PRODUCT : TFT TOUCH MODULE

MODULE NO. : WKS70WSV016-WCT

SUPPLIER: WKS Technology Co.,LTD

DATE: Dec 11, 2018

SPECIFICATION

Revision: 0.0

WKS70WSV016-WCT

This module uses ROHS material

This specification may change without prior notice in order to improve performance or quality. Please contact WKS R&D department for updated specification and product status before design for this product or release of this order.

WRITTEN BY	*CHECKED BY*	*APPROVED BY*
Jason	Eric	Henry

REVISION RECORD

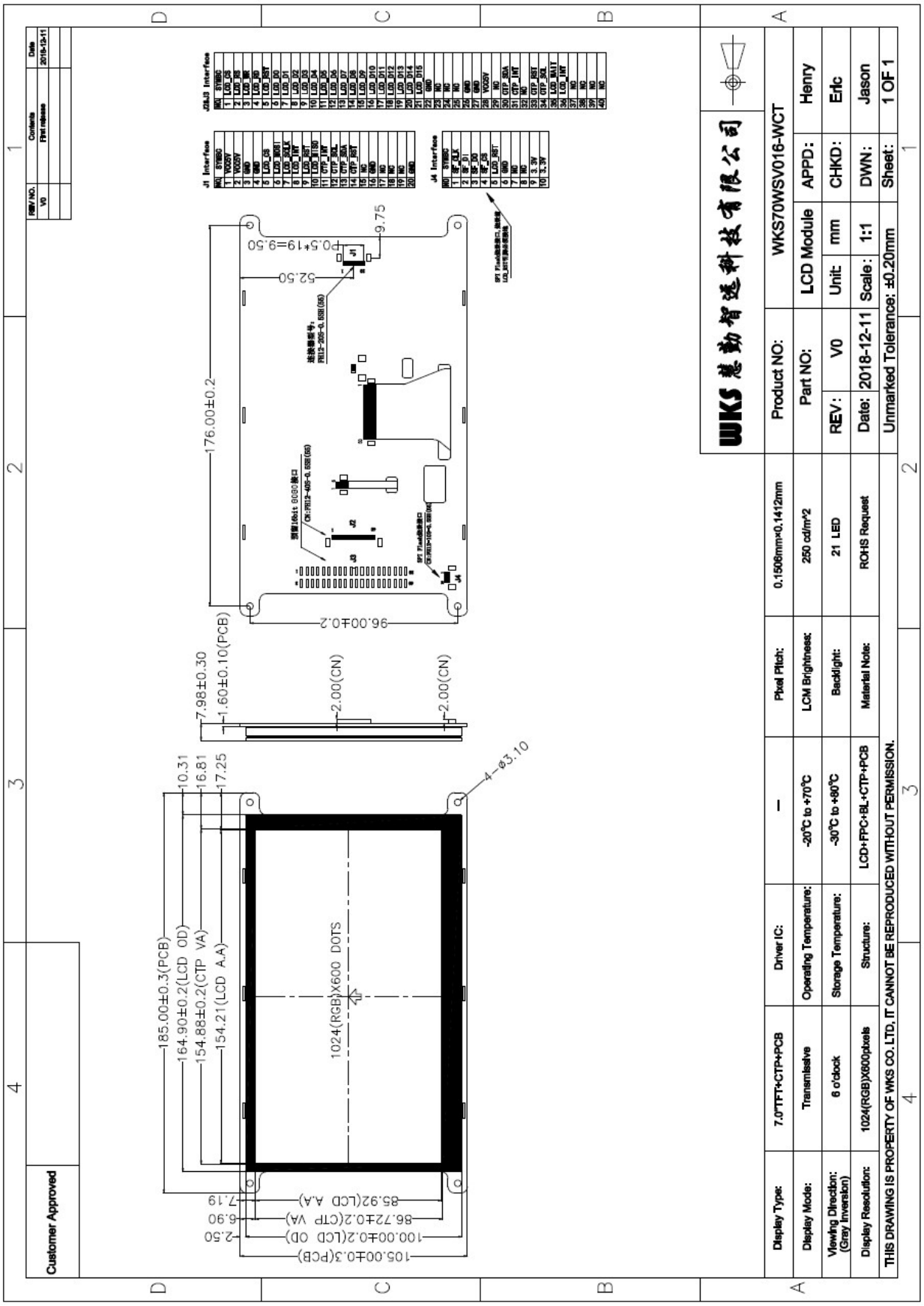
REV NO.	REV DATE	CONTENTS	REMARKS
0.0	2018-12-11	First release	Preliminary

CONTENTS

1、GENERAL INFORMATION

Item of general information	Contents		Unit
LCD Display Size(Diagonal)	7.0		inch
Module Structure	LCD Display + CTP Touch + PCB		-
LCD Display Type	TFT/TRANSMISSIVE		-
LCD Display Mode	Normally White		-
Recommended Viewing Direction	12		o'clock
Gray inversion Direction	6		o'clock
Module size (W×H×T)	185.00×105.00×7.98		mm
Active area (W×H)	154.21×85.92		mm
Number of pixels (Resolution)	1024RGB×600		pixel
Pixel pitch (W×H)	0.1506×0.1432		mm
LCD Driver IC	-		-
Module Interface Type	LCD	SPI or 8080/6800 interface	-
	CTP	I2C interface	-
Module Input voltage	5.0V		V
Module Power consumption	-		mW
Color Numbers	16.7M		-
Backlight Type	White LED		-

2、EXTERNAL DIMENSIONS



3、ABSOLUTE MAXIMUM RATINGS

Parameter of absolute maximum ratings	Symbol	Min	Max	Unit
Operating temperature	Top	-20	70	℃
Storage temperature	Tst	-30	80	℃
Humidity	RH	-	90%(Max 60℃)	RH

Note: Absolute maximum ratings means the product can withstand short-term, not more than 120 hours. If the product is a long time to withstand these conditions, the life time would be shorter.

4、ELECTRICAL CHARACTERISTICS(DC CHARACTERISTICS)

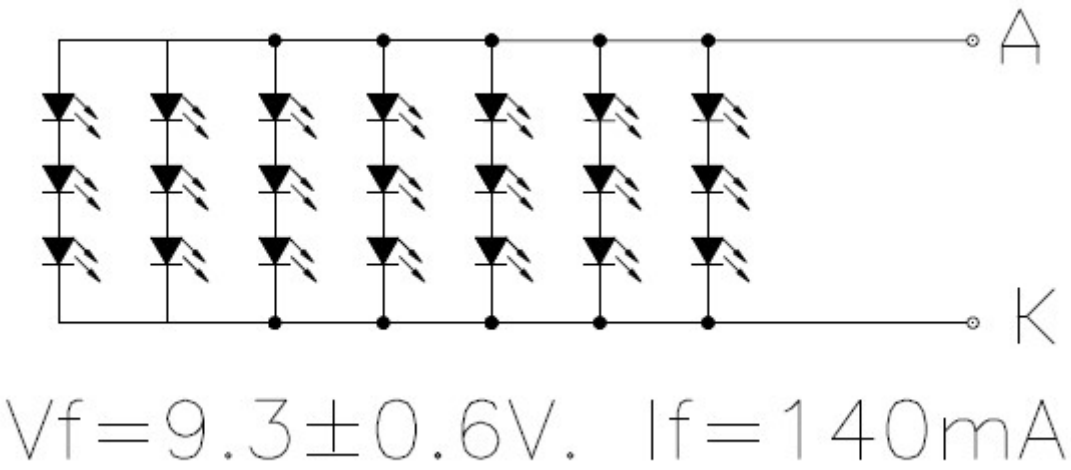
Parameter of DC characteristics	Symbol	Min.	Typ.	Max.	Unit
PCB operating voltage	VCC5V	-	5.0	-	V
LCD I/O operating voltage	VDD	3.0	3.3	3.6	V
Input voltage 'H' level	VIH	2	-	3.6	V
Input voltage 'L' level	VIL	-0.3	-	0.8	V
Output voltage 'H' level	VOH	2.4	-	-	V
Output voltage 'L' level	VOL	-	-	0.4	V

5、BACKLIGHT CHARACTERISTICS

Item of backlight characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Voltage	Vf	8.7	9.3	9.9	V	Note1
Forward Current	If	-	140	-	mA	-
Number of LED	-	-	3*7=21	-	Piece	-
LED Connection mode	P/S	-	Serial/Parallel	-	-	-
Lifetime of LED	-	-	10000	-	hour	Note2

Note:

- Note1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and If=140mA.
- Note2: The LED lifetime define as the estimated time to 50% degradation of initial luminous. The LED lifetime could be decreased if operating If is larger than 140mA.
- Backlight circuit:



6、CTP CHARACTERISTICS

Item of CTP characteristics	Specification	Unit	Remark
Panel Type	Glass Cover + Glass Sensor	-	-
Resolution	1024 × 600	pixel	-
Surface Hardness	≥6H	-	-
Transparency	>82%	-	-
Driver IC	-	-	-
Interface Type	I2C	-	-
Support Points	5	-	-
Sampling Rate	20~100	Hz	-
Supply voltage	3.3	V	-

7、ELECTRO-OPTICAL CHARACTERISTICS

Item of electro-optical characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	Note
Response time		Tr+Tf	θ=0 ∅=0 Ta=25℃	-	25	40	ms	FIG 1.	4
Contrast Ratio		CR		-	400	-	-	FIG 2.	1
Luminance uniformity		δWHITE		-	80	-	%	FIG 2.	3
Surface Luminance		Lv		-	250	-	cd/m2	FIG 2.	2
CIE (x, y) chromaticity	White	White x	θ=0 ∅=0 Ta=25℃	-	0.302	-	-	FIG 2.	5
		White y		-	0.338	-			
	Red	Red x		-	0.606	-			
		Red y		-	0.325	-			
	Green	Green x		-	0.303	-			
		Green y		-	0.567	-			
	Blue	Blue x		-	0.147	-			
		Blue y		-	0.161	-			
Viewing angle range	∅=90(12 o'clock)		CR ≥ 10	-	60	-	deg	FIG 3.	6
	∅=270(6 o'clock)			-	70	-	deg		
	∅=0(3 o'clock)			-	80	-	deg		
	∅=180(9 o'clock)			-	80	-	deg		
NTSC ratio	-		-	-	50	-	%	-	-

Note 1. *Contrast Ratio(CR) is defined mathematically by the following formula. For more information see FIG 2.:*

$$\text{Contrast Ratio(CR)} = \frac{\text{Average Surface Luminance with all white pixels(P1,P2,P3,P4,P5,P6,P7,P8,P9)}}{\text{Average Surface Luminance with all black pixels(P1,P2,P3,P4,P5,P6,P7,P8,P9)}}$$

Note 2. *Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see FIG 2.*

Lv=Average Surface Luminance with all white pixels (P1,P2,P3,P4,P5,P6,P7,P8,P9)

Note 3. *The uniformity in surface luminance（δWHITE）is determined by measuring*

luminance at each test position 1 through 9, and then dividing the maximum luminance of 9points luminance by minimum luminance of 9 points luminance. For more information see FIG 2.

$$\delta WHITE = \frac{Minimum\ Surface\ Luminance\ with\ all\ white\ pixels\ (P1, P2, P3, P4, P5, P6, P7, P8, P9)}{Maximum\ Surface\ Luminance\ with\ all\ white\ pixels\ (P1, P2, P3, P4, P5, P6, P7, P8, P9)}$$

Note 4. *Response time is the time required for the display to transition from White to black(Rise Time, Tr) and from black to white(Decay Time, Tf). For additional information see FIG 1.*

Note 5. *CIE (x, y) chromaticity ,The x,y value is determined by screen active area position 5. For more information see FIG 2.*

Note 6. *Viewing angle is the angle at which the contrast ratio is greater than a specific value. For TFT module, the specific value of contrast ratio is 10.The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.*

Note 7. *For Viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope. Series Instruments. For contrast ratio, Surface Luminance, Luminance uniformity and CIE， the testing data is base on BM-7 photo detector.*

Note 8. *For TN type TFT transmissive module, Gray scale reverse occurs in the direction of panel viewing angle.*

FIG.1. The definition of Response Time

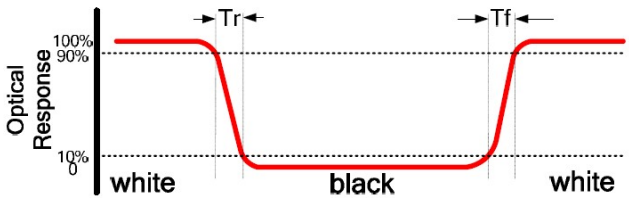


FIG.2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x , y) chromaticity

A : H/6 ;
B : V/6 ;
H,V : Active Area(AA) size
Measurement instrument: BM-7; Light spot size=5mm, 350mm distance from the LCD surface to detector lens.

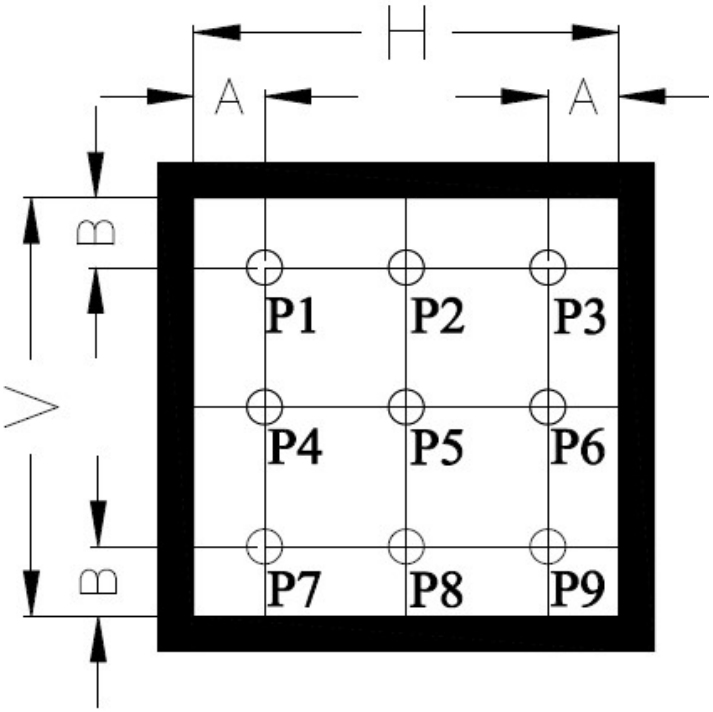
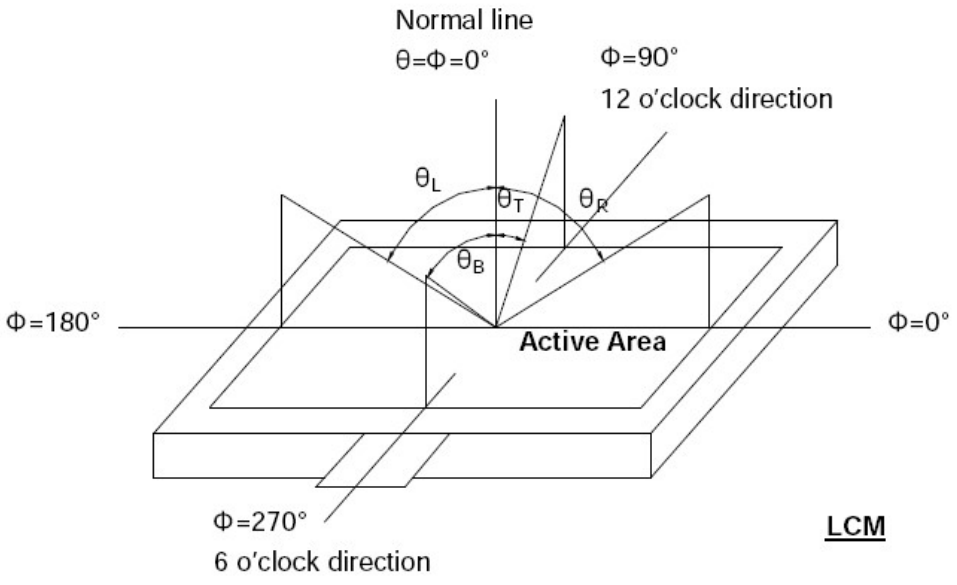


FIG.3. The definition of viewing angle



8、INTERFACE DESCRIPTION

8.1、J1 Interface Description (SPI interface)

NO.	Symbol	I/O	DESCRIPTION
1~2	VCC5V	Power supply	Module Power supply (5V Typ.)
3~4	GND	Power supply	Power ground
5	LCD_CS	I	Chip Select pin for 3-wire or 4-wire serial I/F.
6	LCD_MOSI	I	Data input pin of 4-wire SPI I/F.
7	LCD_SCLK	I	Clock of 3-wire or 4-wire serial I/F.
8	LCD_INT	O	The interrupt output for host to indicate the status.
9	LCD_RST	I	This is an active low Reset pin for LCD.
10	LCD_MISO	O	Data output pin of 4-wire SPI I/F. Bi-direction data pin of 3-wire SPI I/F.
11	CTP_INT	O	CTP External interrupt to the host
12	CTP_SCL	I	CTP I2C clock input
13	CTP_SDA	I/O	CTP I2C data input and output
14	CTP_RST	I	CTP external reset signal, Low is active
15	NC	-	No connection
16	GND	Power supply	Power ground
17	NC	-	No connection
18	NC	-	No connection
19	NC	-	No connection
20	GND	Power supply	Power ground

8.2、J2&J3 Interface Description (8080/6800 interface)

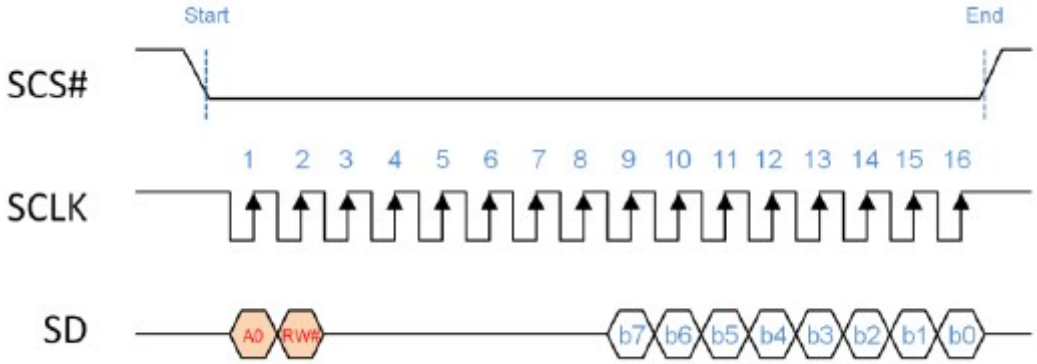
NO.	Symbol	I/O	DESCRIPTION
1	LCD_CS	I	Chip select
2	LCD_RS	I	Data/Command select
3	LCD_WR	I	Write strobe signal
4	LCD_RD	I	Read strobe signal
5	LCD_RST	I	LCD RESET signal, Low is active
6~21	LCD_D0~LCD_D15	I/O	Data bus (D0: LSB; D15: MSB)
22	GND	Power supply	Power ground
23~25	NC	-	No connection
26~27	GND	Power supply	Power ground
28	VCC5V	Power supply	Module Power input (5V Typ.)
29	NC	-	No connection
30	CTP_SDA	I/O	CTP I2C data input and output
31	CTP_INT	I	CTP External interrupt to the host
32	NC	-	No connection
33	CTP_RST	I	CTP external reset signal, Low is active
34	CTP_SCL	I	CTP I2C clock input
35	LCD_WAIT	O	When high, it indicates that the LCD is ready to transfer data; when low, then microprocessor is in wait state.
36	LCD_INT	O	The interrupt output for host to indicate the status.
37	NC	-	No connection
38	NC	-	No connection
39	NC	-	No connection
40	NC	-	No connection

8.3、J4 Interface Description (SPI Flash burning interface)

NO.	Symbol	I/O	DESCRIPTION
1	SF_CLK	I	Serial Clock Input
2	SF_DI	I	Data Input
3	SF_DO	O	Data output
4	SF_CS	I	Chip Select Input
5	LCD_RST	I	LCD RESET signal. This pin must be pull low
6	GND	Power supply	Power ground
7	NC	-	No connection
8	NC	-	No connection
9~10	3.3V	Power supply	Power supply for the SPI Flash (3.3V Typ.)

9、INPUT TIMING

9.1、3-wire SPI Interface



Status Register Read:

1. Host drive SCS#(Low) and SCLK (SPI Clock).

2. Host drive A0(Low), then drive RW#(High).

3. The Driver IC will drive the Data of Status Register (b7 ~ b0) at 9th ~ 16th Clock. Then Host will get the content of Status Register.

Write Register's Address:

1. Host drive SCS#(Low) and SCLK.

2. Host drive A0(Low), then drive RW#(Low).

3. Host drive the Register's Address (b0 ~ b7) at 9th ~ 16th Clock to The Driver IC.

Write Data to Register or Memory:

1. Host drive SCS#(Low) and SCLK.

2. Host drive A0(High), then drive RW#(Low).

3. Host drive the Data at 9th ~ 16th Clock to The Driver IC. i.e. Data will be stored in Register or Memory.

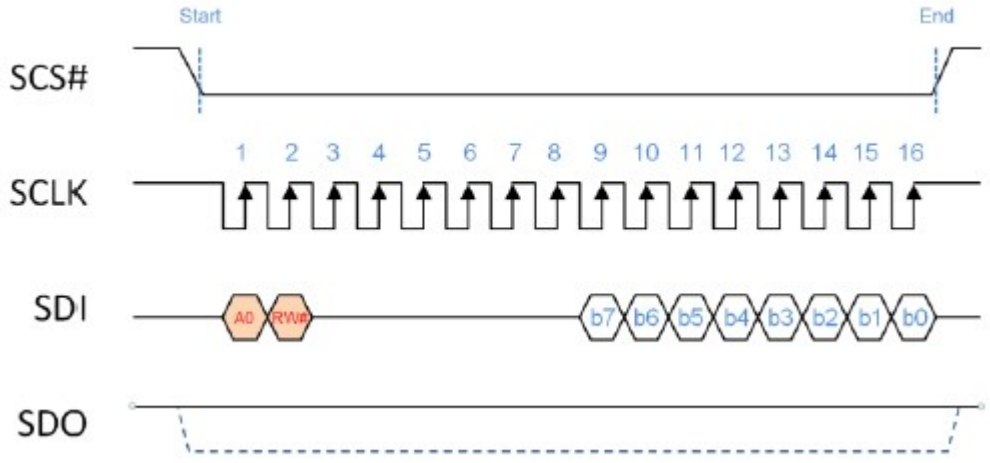
Read Register's Data:

1. Host drive SCS#(Low) and SCLK.

2. Host drive A0(High), then drive RW#(High).

3. The Driver IC will drive the Data of Register at 9th ~ 16th Clock. Then Host will get the content of Register.

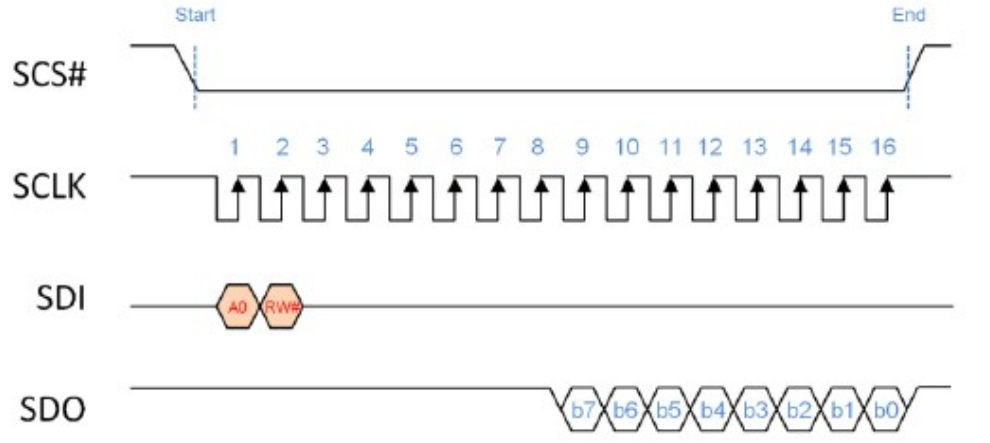
9.2、4-wire SPI Interface



4-Wire SPI Interface Write Timing

When Host drive A0(Low) and RW#(Low), that's means Host write Register's Address. When Host drive A0(High), then RW#(Low) that's means Host write data to Register or Display RAM.

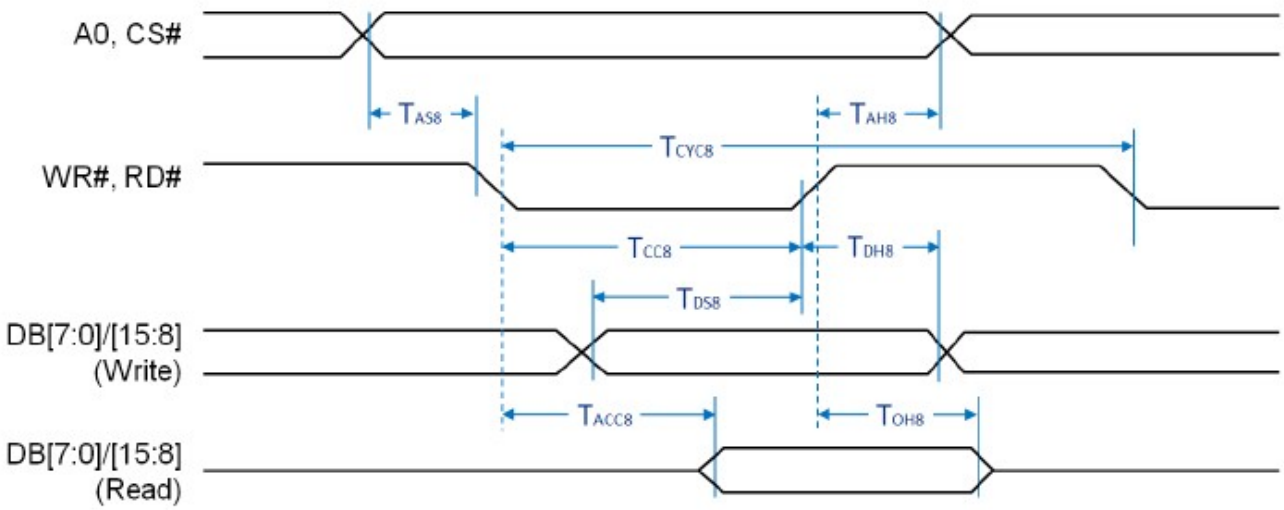
The following Timing diagram is the Read Cycle of 4-Wires SPI. When Host drive A0(Low) and RW#(High), that's means Host want to read the data of Status Register. The Driver IC will drive the Data of Status Register (b7 ~ b0) at 9th ~ 16th Clock. Then Host will get the data of Status Register. When Host drive A0(High), then RW#(High) that's means Host want to read the data of Command Register. The Driver IC will drive the Data of Command Register (b7 ~ b0) at 9th ~ 16th Clock for Host. Of course, Host will get the content of Command Register.



4-Wire SPI Interface Read Timing

9.3、8080/6800 Interface

9.3.1 8080 Parallel Interface



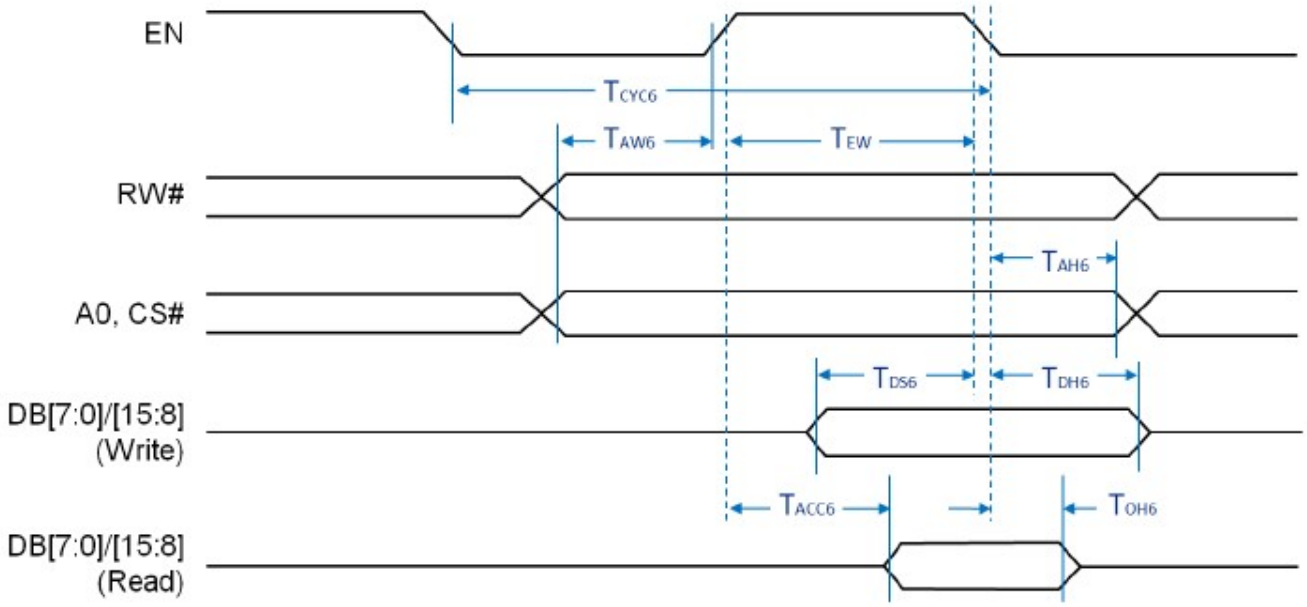
8080 Parallel Mode Interface Timing

The WAIT# signal is used to indicate The Driver IC is ready to transfer data or not. If WAIT# signal did not connect, then the Host access cycle time has to length than five CCLK clocks to avoid access fail. If the Host's Reset signal is active low, then it can connect to RST# of The Driver IC. Of course, the RST# can also control by the I/O pin of host, or connect a RC circuit to generate a low pulse. However, either way to confirm RST#'s active cycle has to keep at least 256 system clock cycle. While using The Driver IC, Host should first confirm the state register bit1, to know whether the The Driver IC in the standard operating state.

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CYC8}	Cycle Time	50	--	ns	tc is one system clock period: tc = 1/SYS_CLK
T_{CC8}	Strobe Pulse Width	20	--	ns	
T_{AS8}	Address Setup Time	0	--	ns	
T_{AH8}	Address Hold Time	10	--	ns	
T_{DS8}	Data Setup Time	20	--	ns	
T_{DH8}	Data Hold Time	10	--	ns	
T_{ACC8}	Data Output Access Time	0	20	ns	
T_{OH8}	Data Output Hold Time	0	20	ns	

8080 Parallel Mode Interface Timing Parameter

9.3.2 6800 Parallel Interface



6800 Parallel Mode Interface Timing

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CYC6}	Cycle Time	50	--	ns	tc is one system clock period: tc = 1/SYS_CLK
T_{EW}	Strobe Pulse Width	20	--	ns	
T_{AW6}	Address Setup Time	0	--	ns	
T_{AH6}	Address Hold Time	10	--	ns	
T_{DS6}	Data Setup Time	20	--	ns	
T_{DH6}	Data Hold Time	10	--	ns	
T_{ACC6}	Data Output Access Time	0	20	ns	
T_{OH6}	Data Output Hold Time	0	20	ns	

6800 Parallel Mode Interface Timing Parameter

10、RELIABILITY TEST CONDITIONS

No.	Test Item	Test Condition
1	High Temperature Storage	80℃/120 hours
2	Low Temperature Storage	-30℃/120 hours
3	High Temperature Operating	70℃/120 hours
4	Low Temperature Operating	-20℃/120 hours
5	Temperature Cycle Storage	-20℃(30min.)~25(5min.)~70℃(30min.)×10cycles

A、Inspection after test:

Inspection after 2~4 hours storage at room temperature, the sample shall be free from defects:

- Air bubble in the LCD;
- Sealleak;
- Non-display;
- Missing segments;
- Glass crack;
- Current is twice higher than initial value.

B、Remark:

- The test samples should be applied to only one test item.
- Sample size for each test item is 5~10pcs.
- Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11、INSPECTION CRITERION

This specification is made to be used as the standard of acceptance/rejection criteria for TFT-LCD/IPS TFT-LCD module product, and this specification is applicable only in the case that the size of module equal to or exceed than 3.5 inch.

11.1 Sample plan

Sampling plan according to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993,normal level 2 and based on:

Major defect: AQL 0.65

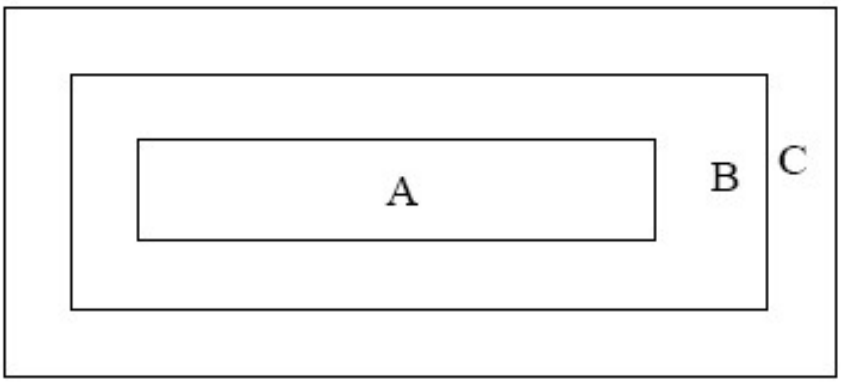
Minor defect: AQL 1.5

11.2 Inspection condition

Viewing distance for cosmetic inspection is about 30cm with bare eyes, and under an environment of 20~40W light intensity, all directions for inspecting the sample should be within 45°against perpendicular line. (Normal temperature 20~25℃and normal humidity 60 ±15%RH)

11.3 Definition of Inspection Item.

A、Definition of inspection zone in LCD.



Zone A: character/Digit area

Zone B: viewing area except Zone A (Zone A + Zone B=minimum Viewing area)

Zone C: Outside viewing area (invisible area after assembly in customer's product)

Fig.1 Inspection zones in an LCD

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

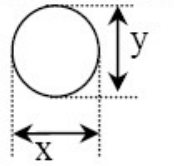
B*、*Definition of some visual defect

Bright dot	*Because of losing all or part function, bad pixel dots appear bright and the size is more than 50% of one dot in which LCD panel is displaying under black pattern.*
Dark dot	*Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture, or pure whiter picture.*

11.4 Major Defect

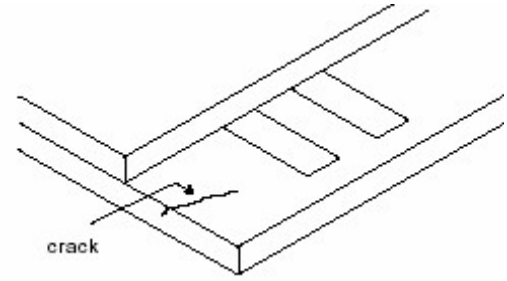
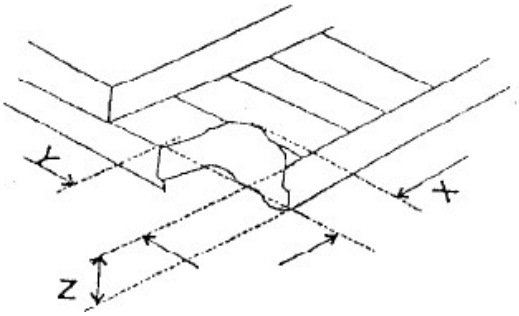
Item No.	***Items to be inspected***	***Inspection standard***	***Classification of defects***
1	*Functional defects*	*1) No display* *2) Display abnormally* *3) Missing vertical, horizontal segment* *4) Short circuit* *5) Excess power consumption* *6)Backlight no lighting, flickering and abnormal lighting*	*major*
2	*Missing*	*Missing component*	
3	*Outline dimension*	*Overall outline dimension beyond the drawing is not allowed*	

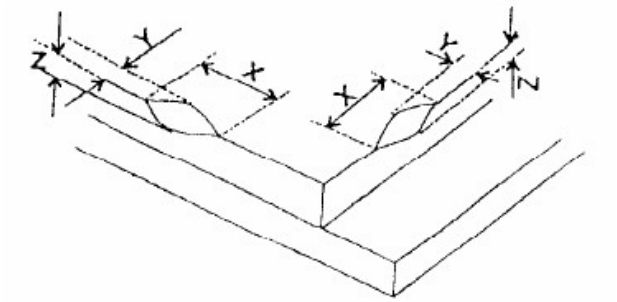
11.5 Minor Defect

<table>
<tr><th>Item No.</th><th>Items to be inspected</th><th>Inspection standard</th><th>Classification of defects</th></tr>
<tr><td>1</td><td>Bright dot /dark dot defect</td><td>
<table>
<tr><td rowspan="2">Zone</td><td colspan="3">Acceptable Qty</td><td rowspan="2"></td></tr>
<tr><td colspan="3">A+B</td></tr>
<tr><td></td><td>3.5” ～ 7”</td><td>7～10.1”</td><td>>10.1”</td><td>C</td></tr>
<tr><td>Bright pixel dot</td><td>1</td><td>2</td><td>3</td><td rowspan="5">Acceptable</td></tr>
<tr><td>Dark pixel dot</td><td>4</td><td>4</td><td>4</td></tr>
<tr><td>2bright dots adjacent</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2dark dots adjacent</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Total bright and dark dots</td><td>5</td><td>6</td><td>7</td></tr>
</table>
Note: Minimum distance between defective dots is more than 5mm; Pixel dots’ function is normal, but bright dots caused by foreign material and other reasons are judged by the dot defect of 5.2.
</td><td>Minor</td></tr>
<tr><td>2</td><td>Dot defect
 

Φ=(x+y) /2</td><td>
<table>
<tr><td rowspan="2">Zone
Size(mm)</td><td colspan="3">Acceptable Qty</td><td rowspan="2"></td></tr>
<tr><td colspan="3">A+B</td></tr>
<tr><td></td><td>3.5”～7”</td><td>7～10.1”</td><td>>10.1”</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td>Acceptable</td><td>Acceptable</td><td>Acceptable</td><td rowspan="3">Acceptable</td></tr>
<tr><td>0.2＜Φ≤0.5</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>Φ＞0.5</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Note:
1. Minimum distance between defective dots is more than 5 mm;
2. The quantity of defect is zero in operating condition.
</td><td>Minor</td></tr>
<tr><td>3</td><td>Linear defect</td><td>
<table>
<tr><td colspan="2" rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td><td rowspan="3"></td></tr>
<tr><td colspan="3">A+B</td></tr>
<tr><td>Length</td><td>Width</td><td>3.5”～7”</td><td>7～10.1”</td><td>>10.1”</td><td>C</td></tr>
<tr><td>Ignore</td><td>W≤0.05</td><td>Acceptable</td><td>Acceptable</td><td>Acceptable</td><td rowspan="3">Acceptable</td></tr>
<tr><td>L≤5.0</td><td>0.05＜W≤0.1</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>L＞5.0</td><td>W＞0.1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
</table>

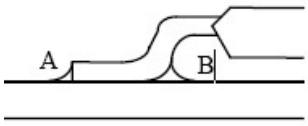
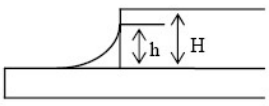
<table>
<tr>
<td>4</td>
<td>Polarizer defect</td>
<td>
5.4.1 Polarizer Position
(i) Shifting in position should not exceed the glass outline dimension.
(ii) Incomplete covering of the viewing area due to shifting is not allowed.
5.4.2 Dirt on polarizer
Dirt which can be wiped easily should be acceptable.
5.4.3 Polarizer Dent & Air bubble
<table>
<tr><td rowspan="2">Zone
Size(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td colspan="2">A+B</td><td>C</td></tr>
<tr><td>Φ≤0.2</td><td>Acceptable</td><td>Acceptable</td><td>Acceptable</td><td rowspan="4">Acceptable</td></tr>
<tr><td>0.2＜Φ≤0.5</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>Φ＞0.5</td><td>0</td><td>0</td><td>0</td></tr>
</table>
5.4.4 Polarizer scratch
(i) If the polarizer scratch can be seen after cover assembling or in the operating condition, judge by the linear defect of 5.3.
(ii)If the polarizer scratch can be seen only in non-operating condition or some special angle, judge by the following:
<table>
<tr><td colspan="2" rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td colspan="2">A+B</td><td>C</td></tr>
<tr><td>Length</td><td>Width</td><td>3.5”～7”</td><td>7～10.1”</td><td>＞10.1”</td><td rowspan="4">Acceptable</td></tr>
<tr><td>Ignore</td><td>W≤0.05</td><td>Acceptable</td><td>Acceptable</td><td>Acceptable</td></tr>
<tr><td>1.0＜L≤5.0</td><td>0.05＜W≤0.20</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>L＞5.0</td><td>W＞0.2</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td>
<td>Minor</td>
</tr>
<tr>
<td rowspan="2">5</td>
<td>MURA</td>
<td>Using 3% ND filter, it’s NG if it can be seen in R,G,B picture.</td>
<td rowspan="2">Minor</td>
</tr>
<tr>
<td>White/Black dot（MURA）</td>
<td>Visible under：ND3%；D≦0.15mm, Acceptable；
0.15mm<D≦0.5mm, N≦4；D>0.5mm, Not allowable.</td>
</tr>
</table>

<table>
<tr><td rowspan="3">6</td><td rowspan="3">Glass defect</td><td>(i) Crack
Cracks are not allowed.
 
</td><td>Minor</td></tr>
<tr><td>(ii) TFT chips on corner
 

<table><tr><th>X</th><th>Y</th><th>Z</th><th>Acceptable</th></tr><tr><td>≤3.0</td><td>≤3.0</td><td>Not more than the thickness of glass</td><td>N≤3</td></tr></table>Chips on the corner of terminal shall not be allowed to extend into the ITO pad or expose perimeter seal.</td><td>Minor</td></tr>
<tr><td>(iii) Usual surface crack
 

<table><tr><th>X</th><th>Y</th><th>Z</th><th>Acceptable</th></tr><tr><td>≤1.5</td><td>≤1.5</td><td>Not more than the thickness of glass</td><td>N≤4</td></tr></table>It is only applicable to the upper glass of LCD.</td><td>Minor</td></tr>
</table>

11.6 Module Cosmetic Criteria

Item No.	Items to be inspected	Inspection Standard	Classification of defects
1	Difference in Spec.	Not allowable	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing	Major
		No soldering bridge	Major
		No cold soldering	Minor
4	Resist flaw on PCB	Visible copper foil (Φ0.5 mm or more) on substrate pattern is not allowed	Minor
5	FPC gold finger	No dirt, breaking, oxidation lead to black	Major
6	Backlight plastic frame	No deformation, crack, breaking, backlight positioning column breaking, obvious nick.	Minor
7	Marking printing effect	No dark marking, incomplete, deformation lead to unable to judge	Minor
8	Accretion of metallic Foreign matter	No accretion of metallic foreign matter (Not exceed Φ0.2mm)	Minor
9	Stain	No stain to spoil cosmetic badly	Minor
10	Plate discoloring	No plate fading, rusting and discoloring	Minor
11	1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly.	Minor
		b. Components side(In case of 'Through Hole PCB') Solder to reach the Components side of PCB.	Minor
	2. Flat packages	Either 'Toe'(A) or 'Seal'(B)of the lead to be covered by "Filet". Lead form to be assume over Solder. 	Minor
	3. Chips	(3/2) H ≥h ≥(1/2) H 	Minor
	4. Solder ball/Solder splash	a. The spacing between solder ball and the conductor or solder pad h ≥0.13 mm. The diameter of solder ball d ≤0.15 mm.	Minor
		b. The quantity of solder balls or solder splashes isn't beyond 5 in 600 mm2.	Minor
		c. Solder balls/Solder splashes do not violate minimum electrical clearance.	Major