Sitronix

ST5623

PRELIMINARY

6-Bit 1200-Channel TFT LCD Source Driver with TCON

Product Description

ST5623 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. ST5623 integrate source driver, timing controller and pin control interface. Input data can support TTL digital 18-bit / 24-bit parallel RGB data format, and source driver support 256 gray scales with dithering features. All functions can be set by relative H/W pin.

ST5623 can be configured as dual-gate operation mode to reduce the FPC amount and save the cost. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

Features

◆ TCON

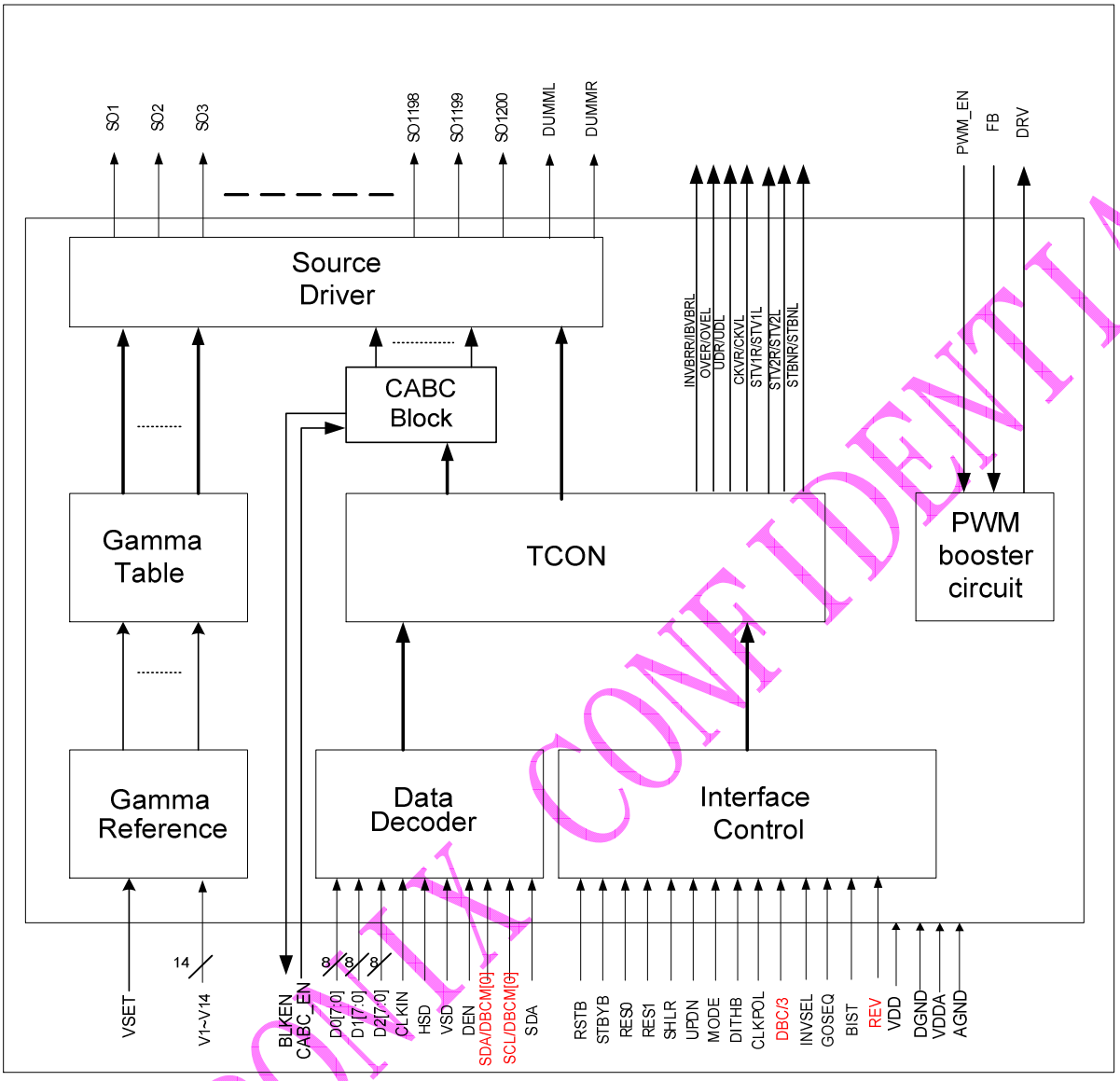
- Supports display resolutions : 800(RGB)x600、800(RGB)x480、640(RGB)x480
- Supports TTL 18-bit or 24-bit parallel (RGB) input timing
- Support LED Backlight Enable Control Signal With CABC Function(CABC_PWM)
- Supports to configure CABC block via 3 line SPI mode
- Output dynamic range : 0.1 ~ VDDA-0.1V
- Power for logic circuit : 3.0V~3.6V
- Operating frequency : 50MHz
- 8-bit resolution with 2-bits dithering
- Support dual-gate operation mode
- Support Stripe color filter configuration
- Hardware Pin Control CABC Mode Selection

◆ PWM booster function

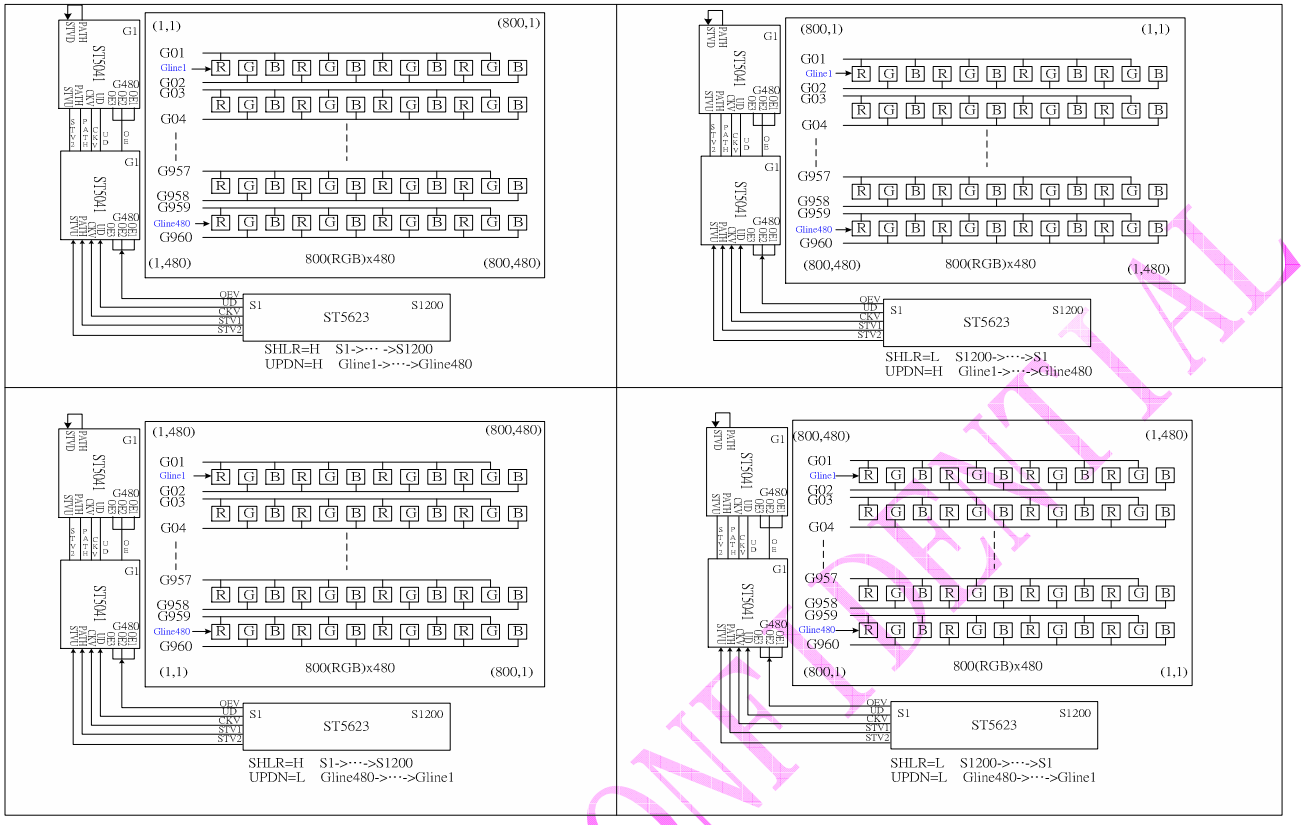
◆ Source Driver

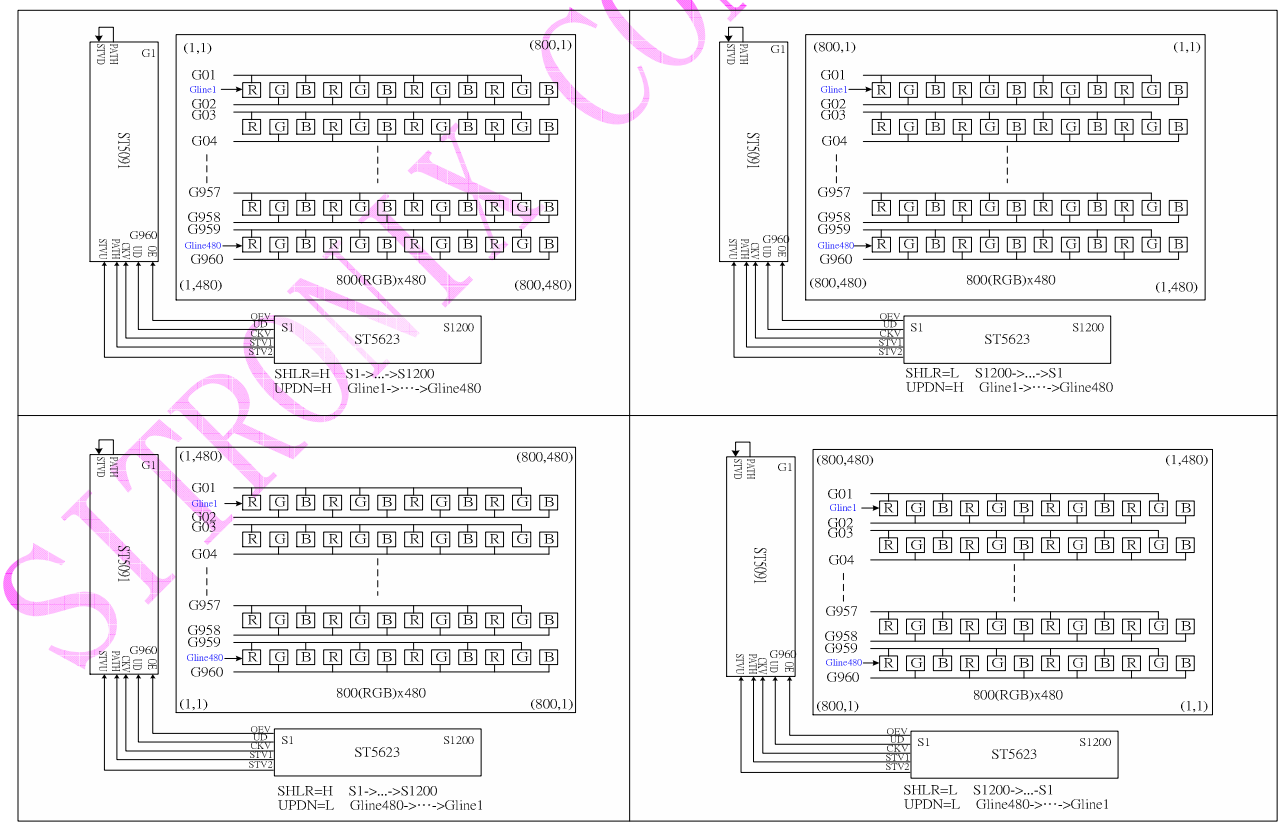
- Output : 1200/960 output channels
- Power of LCD driving voltage : 6.5 ~ 13.5V
- Output deviation : ± 20mV
- Supports external V1~V14 pad for Gamma correction
- Support stand-by mode for low power consumption
- Support 1 dot or 2 dot inversion driving scheme
- Package : COG available

Function Block Diagram

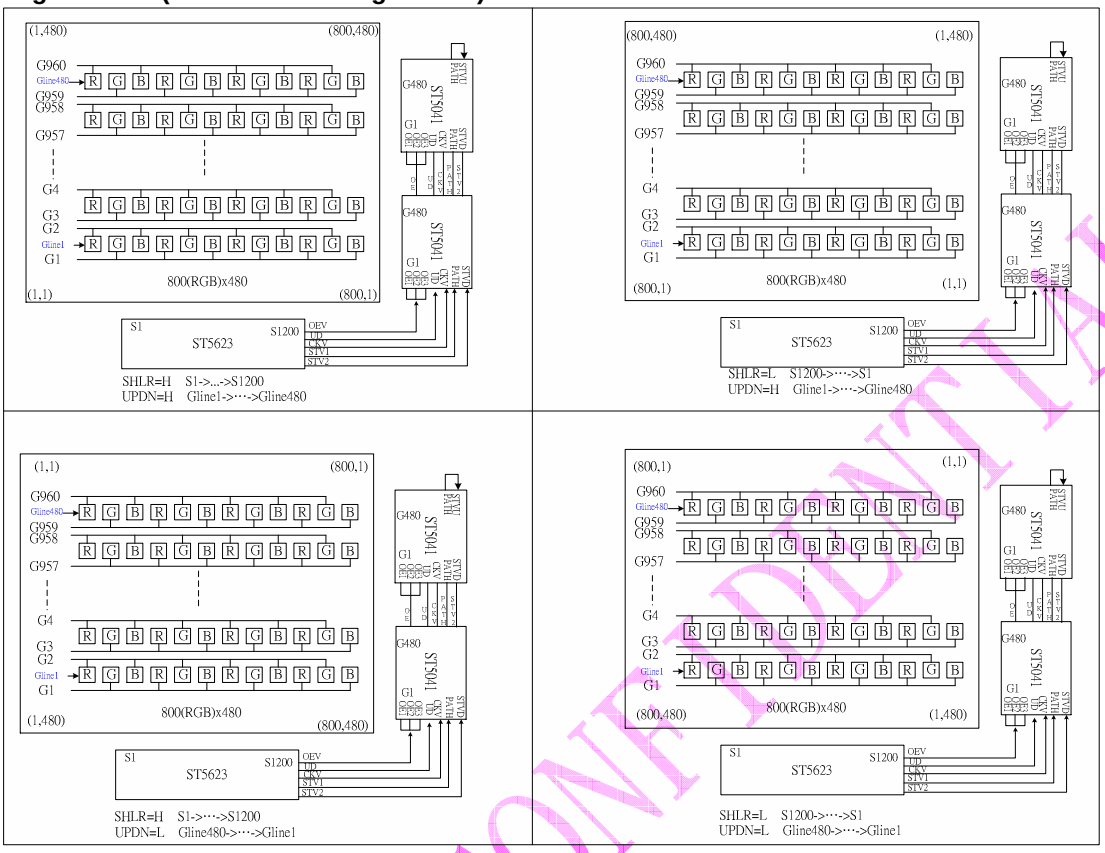


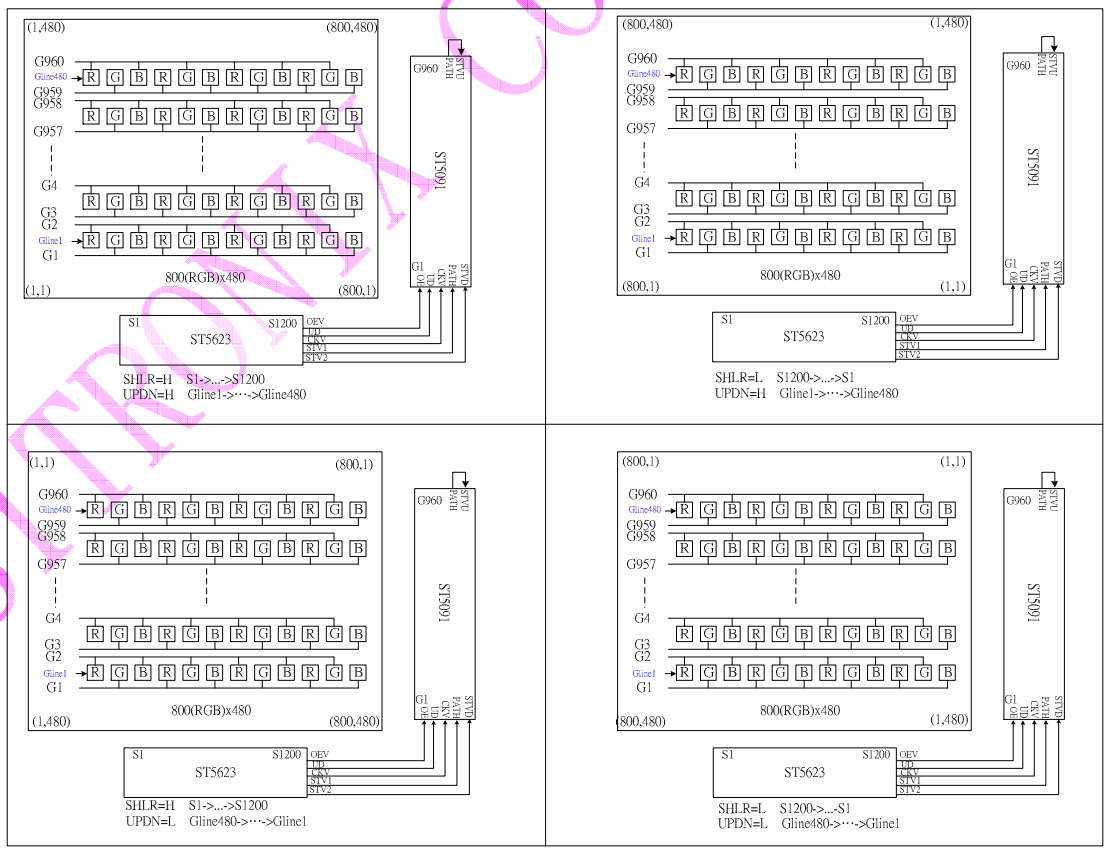
800x480 dual gate mode (Gate driver on left side)



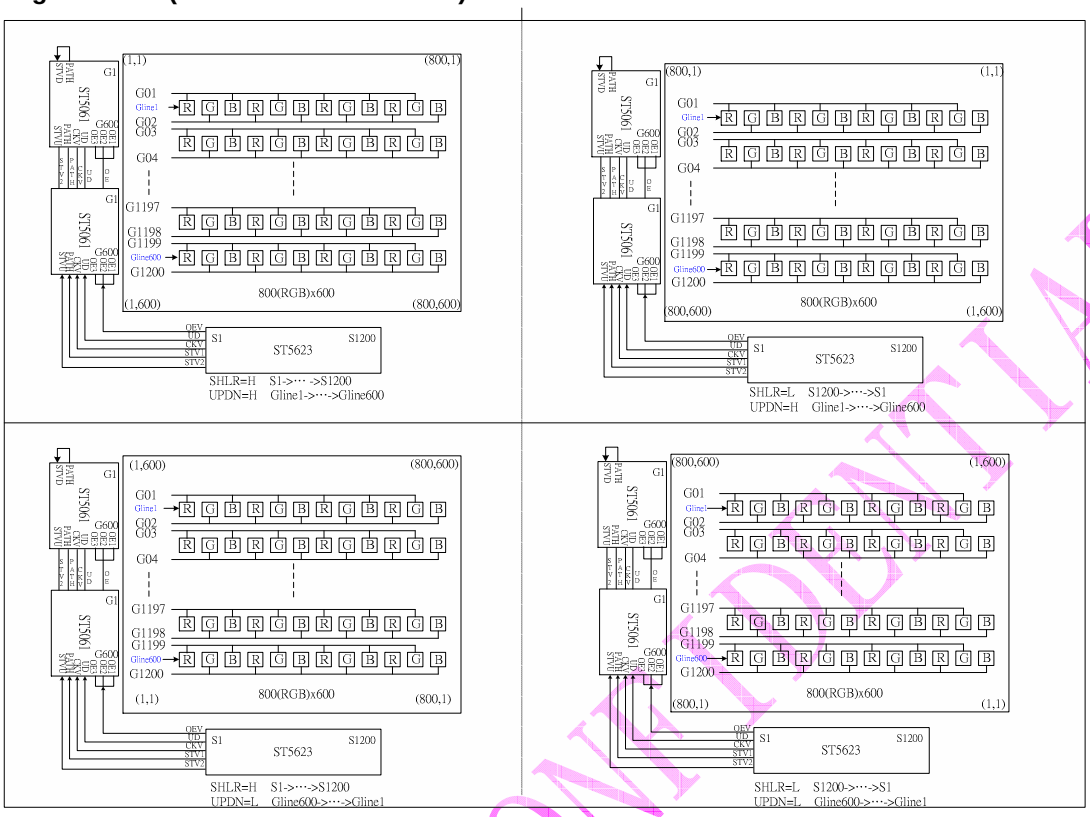


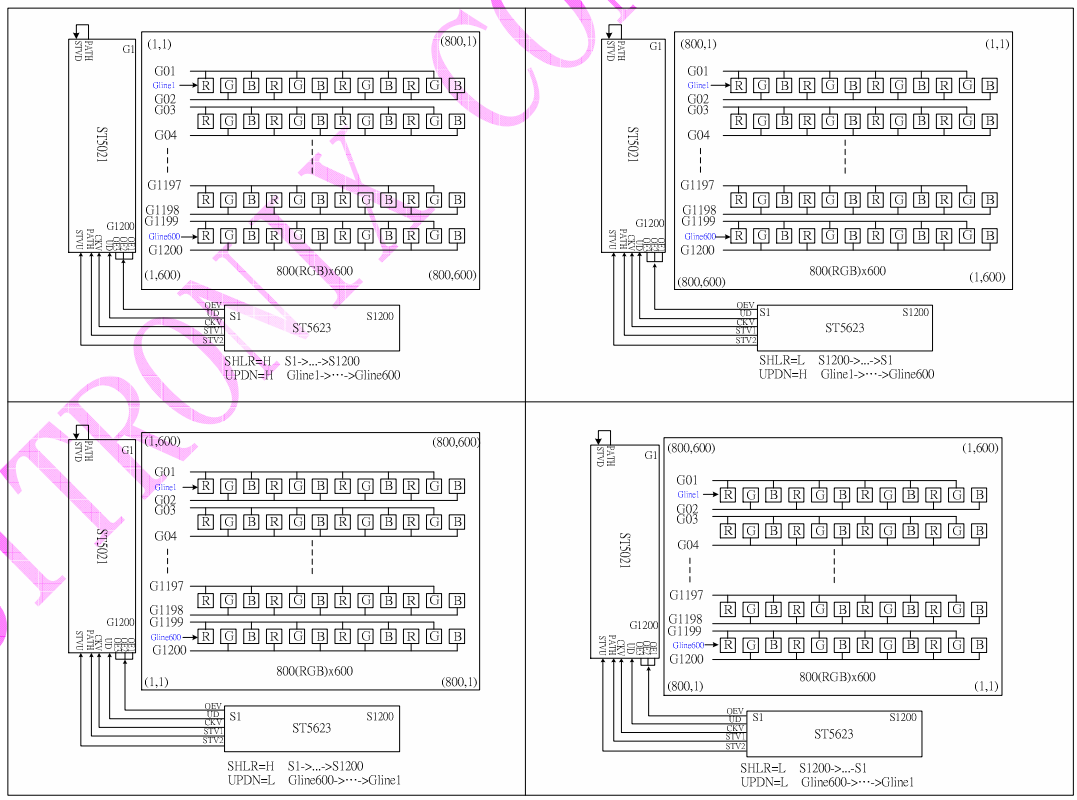
800x480 dual gate mode(Gate driver on right side)



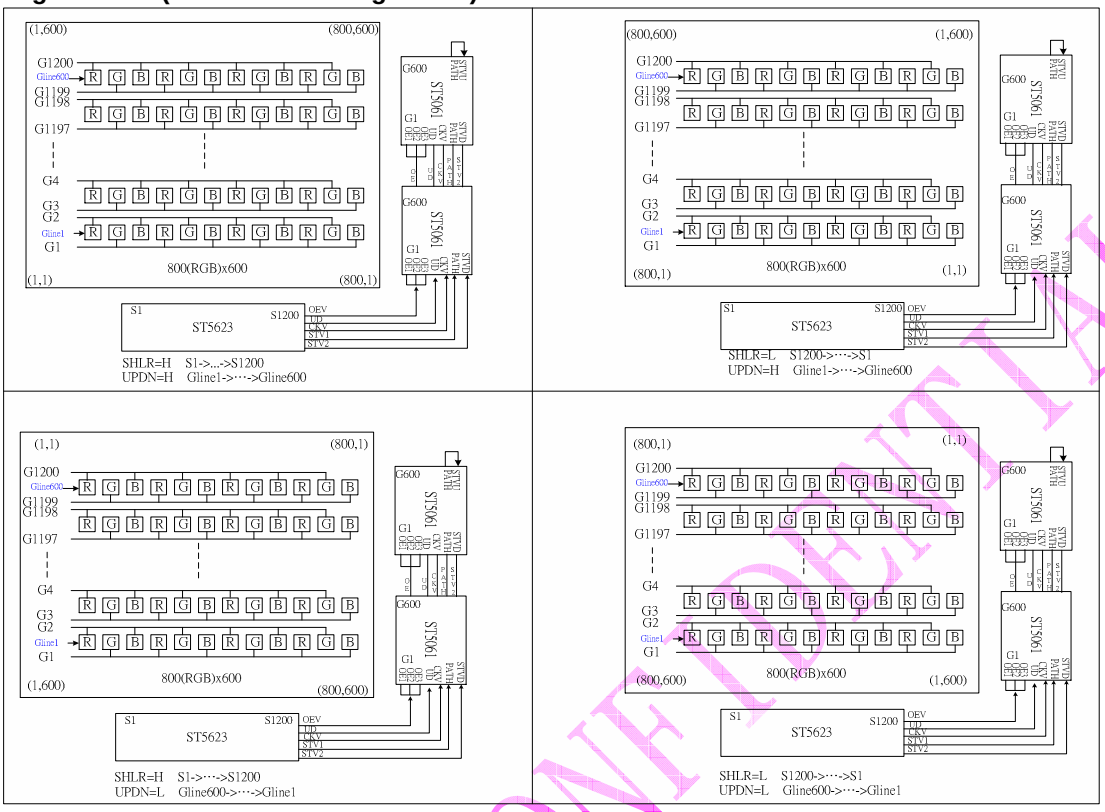


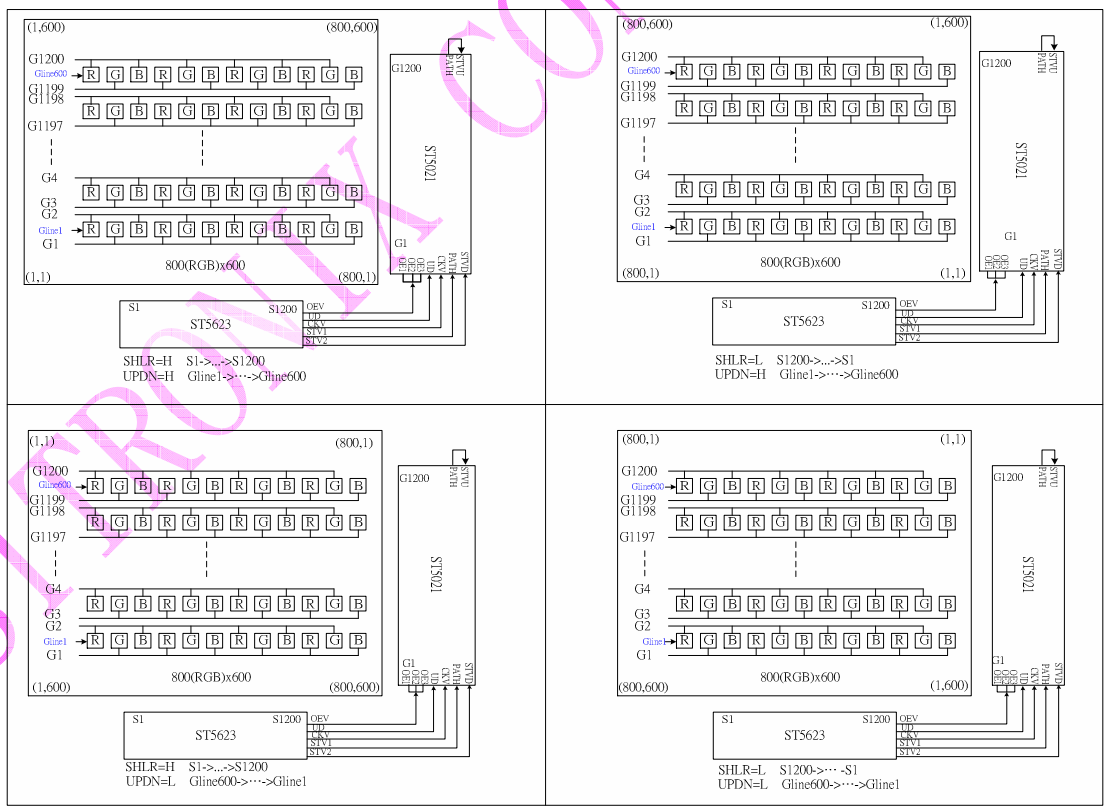
800x600 dual gate mode (Gate driver on left side)



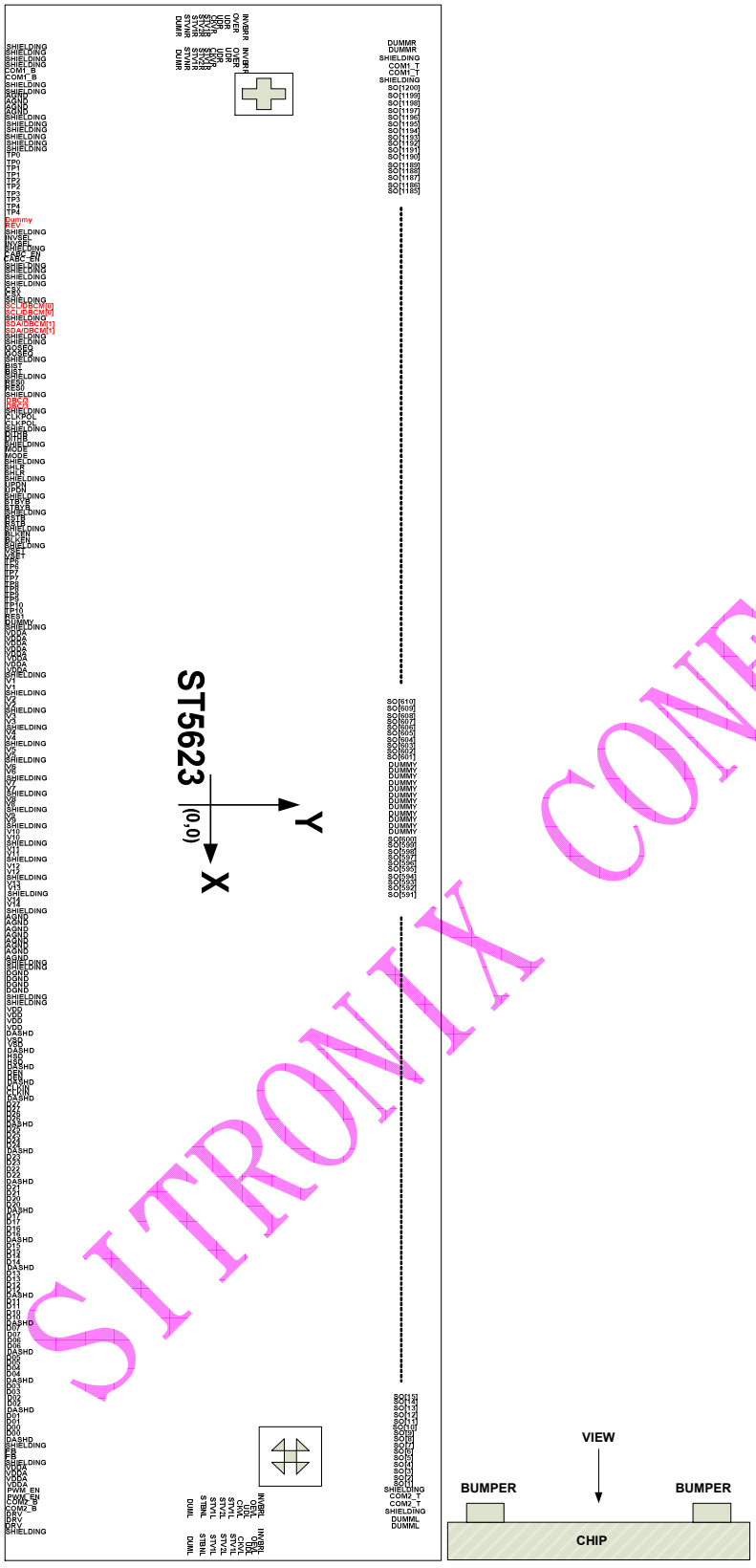


800x600 dual gate mode(Gate driver on right side)





Pin Assignments (Bump View)



Pin Description

<table>
<tr><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>D0[7:0]
D1[7:0]
D2[7:0]</td><td>I</td><td>Parallel data Input. For TTL 24-bit parallel RGB image data input.
D0[7:0] = R[7:0] data; D1[7:0] = G[7:0] data; D2[7:0] = B[7:0] data.
For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to DGND.</td></tr>
<tr><td>CLKIN</td><td>I</td><td>Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.</td></tr>
<tr><td>HSD</td><td>I</td><td>Horizontal Sync input. Negative polarity.</td></tr>
<tr><td>VSD</td><td>I</td><td>Vertical Sync input. Negative polarity.</td></tr>
<tr><td>DEN</td><td>I</td><td>Data Input Enable. Active High to enable the data input bus under “DE Mode”.
(Normally pull low.)</td></tr>
<tr><td>REV</td><td>I</td><td>Data inverted control. Normally pull low
REV=”1”: Data inverted for normally black LCD
REV=”0”: Data not inverted for normally white LCD. (Default)</td></tr>
<tr><td>MODE</td><td>I</td><td>DE / SYNC mode select. (Normally pull high)
H : DE mode.
L : HSD/VSD mode.</td></tr>
<tr><td>RES[1:0]</td><td>I</td><td>Display resolution selection. (default value is 00)
<table>
<tr><th>RES[1:0]</th><th>Resolution</th></tr>
<tr><td>00</td><td>800(RGB)*480</td></tr>
<tr><td>01</td><td>800(RGB)*600</td></tr>
<tr><td>10</td><td>640(RGB)*480(channel 481~720 is disable)</td></tr>
<tr><td>11</td><td>800(RGB)*480</td></tr>
</table></td></tr>
<tr><td>DITHB</td><td>I</td><td>Dithering function enable control. (Normally pull high)
DITHB = “1”, Disable internal dithering function
DITHB = “0”, Enable internal dithering function</td></tr>
<tr><td>CLKPOL</td><td>I</td><td>Input clock edge selection.(Normally pull low)
CLKPOL = “1”, Latch data at CLKIN rising edge.
CLKPOL = “0”, Latch data at CLKIN falling edge.</td></tr>
<tr><td>CSX</td><td>I</td><td>A chip select signal(Normally pull high)
CSX=”L”, the chip is selected and accessible
CSX=”H”, the chip is not selected and not accessible
Note: Fix to the VDD level when not in use.</td></tr>
<tr><td>SCL/DBCM[0]</td><td>I</td><td>Multi-Function Selection:
When DBC/3=”L”, this pin act as 3-wire “SCL” pin.
Serial clock input. This pin is used for CABC command set only.
When DBC/3=”H”, this pin act as DBC mode select pin LSB (DBCM[0])
Note: Normal pull high and Fix to the VDD level when not in use.</td></tr>
<tr><td>SDA/DBCM[1]</td><td>I/O</td><td>Multi-Function Selection:
When DBC/3=”L”, this pin act as 3-wire “SDA” pin.
Serial data input / output. This pin is used for CABC command set only.
When DBC/3=”H”, this pin act as DBC mode select pin MSB (DBCM[1])
Note: Normal pull high and Fix to the VDD level when not in use.</td></tr>
<tr><td>CABC_EN</td><td>I</td><td>CABC Function Enable Control.(Normal pull “L”)
CABC_EN=“L”, BLKEN pin is used to be backlight control signal for external backlight controller.
CABC_EN=“H”, ST5623 will refer the gray scale content of display image to output a PWM frequency to LED driver via BLKEN pin.</td></tr>
<tr><td>BLKEN</td><td>O</td><td>The backlight control signal for external backlight controller.
BLKEN =“L”, turn off the external backlight controller.
BLKEN =“H”, turn on the external backlight controller.
Note: Refer to the Power ON/OFF sequence for the detail information when</td></tr>
</table>

		CABC_EN is set to “L”.
V1 ~ V14	I/O	When VSET=“L”, the internal Gamma table is used and V1~V14 pins are unused. When VSET=“H”, V1~V14 pins are the external adjustment point for Gamma correction. The relationship between V1~V14 must be : AGND<V14<V13<V12<V11<V10<V9<V8<V7<V6<V5<V4<V3<V2<V1<VDDA
GOSEQ	I	Gate on sequence. (Normally pull low) GOSEQ=“L”, INVBRR/INVBRL will output “H” and gate on sequence is “ G1->G2->G3->G4->G5->G6->G7->G8->…….->Gn-3-> Gn-2-> Gn-1-> Gn “ GOSEQ=“H”, INVBRR/INVBRL will output “L” and gate on sequence is “G1->G2->G4->G3->G5->G6->G8->G7->…….-> Gn-3 -> Gn-2-> Gn -> Gn-1” Note : This function is inactive while CFSEL is fixed to “L”.
RSTB	I	Global reset pin. Active Low to enter Reset State. (Normally pull high.) Suggest to connecting with an RC reset circuit for stability.
VSET	I	Gamma correction source select(Normally pull low) VSET=”L” ,to use internal Gamma reference voltage(VDDA) VSET=”H” ,to use external Gamma correction input(V1~V14)
INVSEL	I	The driving polarity inversion select.(Normally pull low) INVSEL=”L”, 2-dot inversion INVSEL=”H”,1-dot inversion
STBYB	I	Standby mode,(normally pulled high.) STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z
SHLR	I	Source Right or Left sequence control.(Normally pull high) SHLR = “L”, shift left : last data = S1←S2←S3.....←S1200 = first data. SHLR = “H”, shift right : first data = S1→S2→S3.....→S1200 = last data.
UPDN	I	Gate Up or Down scan control. (Normally pull high.) UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver. UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.
DBC/3	I	DBC/3-wire selection pin(Normal pull high) DBC/3=”H”, Select DBC hardware control function. DBC/3=”L”, Select 3-wire SPI interface function.
BIST	I	Normal Operation/BIST pattern select. Normally pull low BIST = “H” : BIST(DCLK input is not needed) BIST = “L” : Normal Operation
OVER/OVEL	O	Gate driver control signal
UDR/UDL	O	Gate driver control signal
CKVR/CKVL	O	Gate driver control signal
STV1R/STV1L	O	Gate driver control signal
STV2R/STV2L	O	Gate driver control signal
STBNR/STBNL	O	Gate driver control signal
INVBRR/INVBRL	O	Gate driver control signal(High=Z shape ,Low= 弓 shape)
VDDA	PI	Power supply for analog circuits
AGND	PI	Ground pins for analog circuits

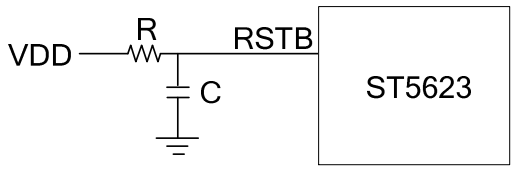
VDD	PI	Power supply for digital circuits
DGND	PI	Ground pins for digital circuits
SO1~SO1200	O	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
ALIGN	M	For assembly alignment.
COM1_B COM1_B	S	Internal link together between input side and output side.
COM1_T COM2_T	S	Internal link together between input side and output side.
TP0~TP4	I	Test pins, not accessible to user, must be left open(Normally pull low)
TP6~TP10	O	Test pins, not accessible to user, must be left open
SHIELDING	SH	IC Shielding pads. Those pins are internally connected to the AGND. DO NOT connect to any WOA on the panel.
DASHD	SH	Data Bus Shielding pad. Those pins are internally connected to the DGND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUMMY DUMMR DUMML	D	Dummy pads. Those pins are floating pads.
PWM_EN	I	PWM_EN="L" ,disable booster circuit(default) PWM_EN="H" ,enable booster circuit
FB	I	feedback voltage from external booster circuit (1.2V)
DRV	O	Driving output for external booster power MOS gate control

Note:
I: Input, O: Output, P: Power, S: Shorted line, M:mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, I / O: Input / Output.

DBC/3 for CABC Function Control description:

<table>
<tr><th rowspan="2">Pin name</th><th colspan="2">DBC/3</th></tr>
<tr><th>L</th><th>H(default)</th></tr>
<tr><td>CSX</td><td rowspan="3">Enable SPI Function</td><td rowspan="3">Disable SPI Function,
CABC Function mode by Hardware Pin control
<table><tr><th>SDA/DBCM[1]</th><th>SCL/DBCM[0]</th><th>MODE</th></tr><tr><td>0</td><td>0</td><td>User Interface image</td></tr><tr><td>0</td><td>1</td><td>CABC off</td></tr><tr><td>1</td><td>0</td><td>Moving image</td></tr><tr><td>1</td><td>1</td><td>Still picture</td></tr><tr><td colspan="3">Remark :Default Still Mode</td></tr></table></td></tr>
<tr><td>SCL/DBCM[0]</td></tr>
<tr><td>SDA/DBCM[1]</td></tr>
</table>

Application Circuit for Reset function



Recommend R =47kΩ,C=0.1uF

Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_B	COM1_T
2	COM2_B	COM2_T

ps: The wiring resistance value from COM1_B(COM2_B) to COM1_T(COM2_T) is less than 10Ω

The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommended as below.

Pin name	Wiring resistance value(Ω)
VDDA	<5
AGND	<5
VDD	<10
DGND	<10
V1~V14	<10
Dx[0:7]	<50
CLKIN	<50
VSD	<50
HSD	<50
DEN	<50
BLK_EN	<200
CSX	<200
SCL/DBCM[0]	<200
SDA/DBCM[1]	<200
RESX	<500
STBYB	<500
DITHB	<500
SHLR	<500
UPDN	<500
BIST	<500
MODE	<500
RES0	<500
RES1	<500
CLKPOL	<500
DBC/3	<500
VSET	<500
INVBRR/INVBRL	<500
OEVR/OEVL	<500
UDR/UDL	<500
CKVR/CKVL	<500
STV1R/STV1L	<500
STV2R/STV2L	<500
STBNR/STBNL	<500
Others	<500

Relationship between the Order of Input Data and Output Channels

GOSEQ= ”H”, Stripe Mode

The relationship between input display data and source output channels is illustrated as below:

(1)、SHLR=”L” , shift left

Output	SO1	SO2	SO3	←	SO1198	SO1199	SO1200
Order	Last data			---	First data		
Odd Line /Gn	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Odd Line /Gn+1	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]
Even Line /Gn	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Even Line /Gn+1	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]

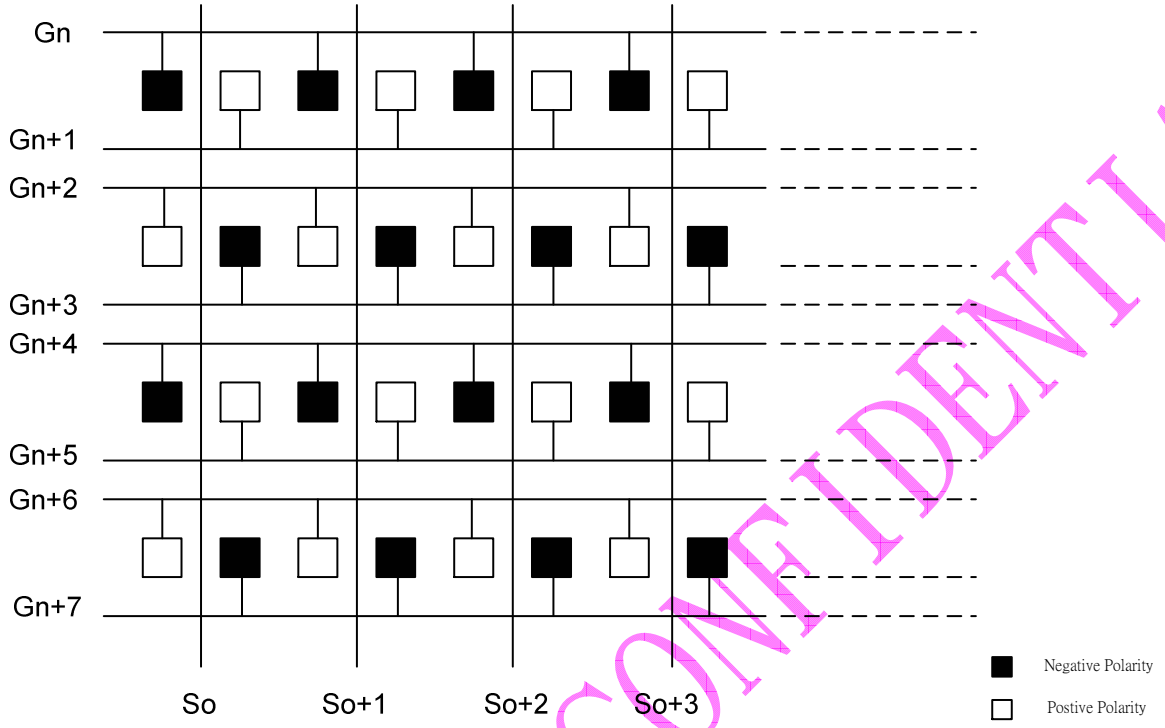
(2)、SHLR=”H” , shift right

Output	SO1	SO2	SO3	→	SO1198	SO1199	SO1200
Order	First data			---	Last data		
Odd Line /Gn	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Odd Line /Gn+1	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]
Even Line /Gn	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Even Line /Gn+1	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]

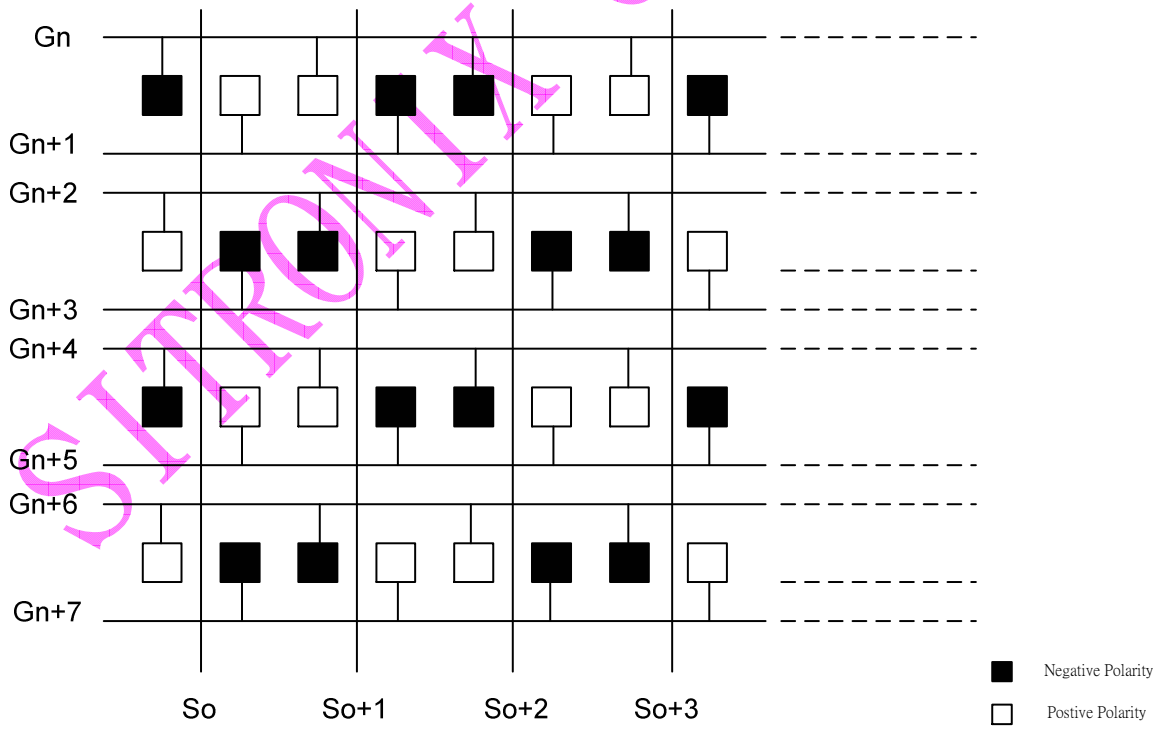
Dot Polarity Inversion

ST5623 supplies both of 1-dot and 2-dot inversion, the pixel polarity inversion was illustrated as below:

1-dot inversion, INVSEL"H" & GOSEQ="L"



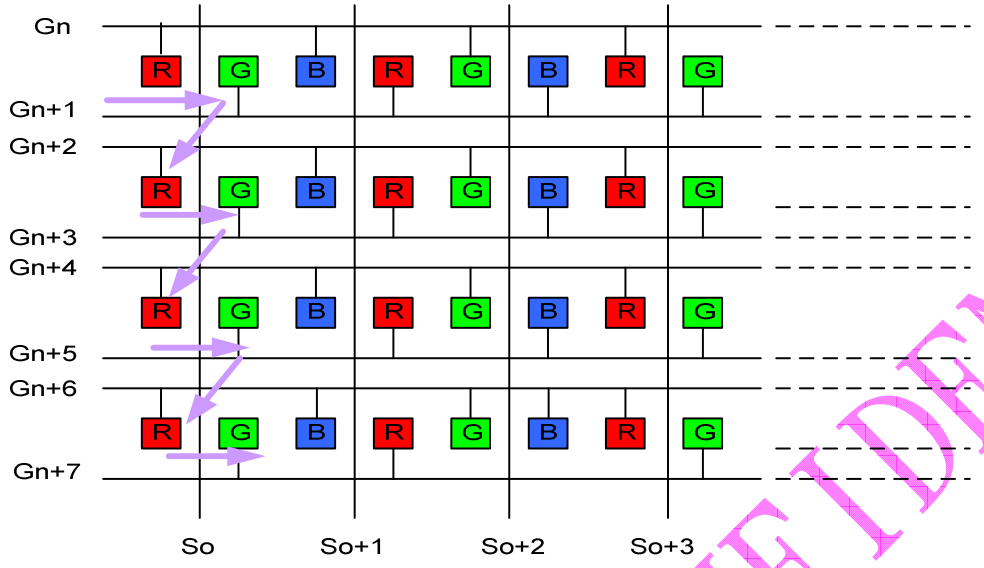
2-dot inversion, INVSEL"L" & GOSEQ="L"



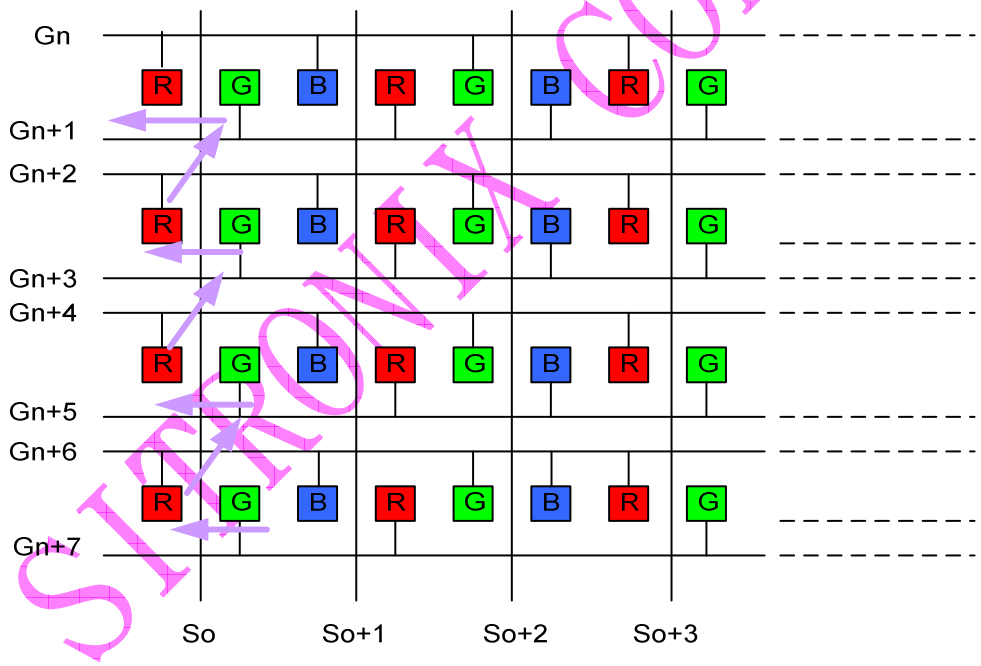
Gate Scan Sequence

Based on special panel request,ST5623 supports two kinds of gate scan sequences and illustrated as below:

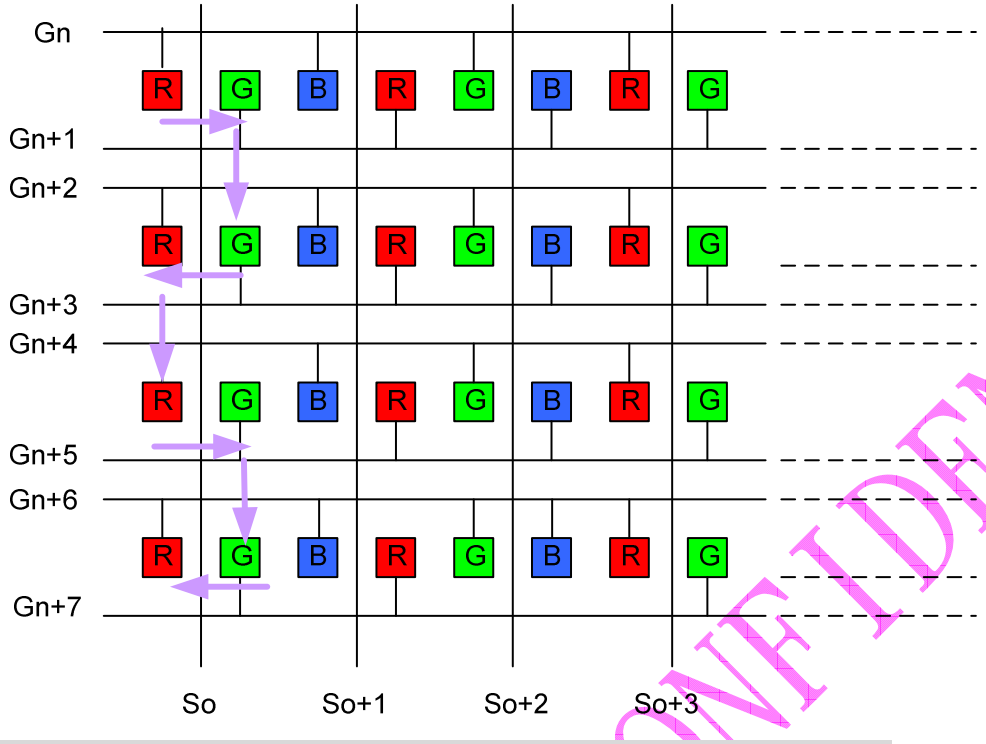
GOSEQ="L" & UPDN="H"=>INVBRR/INVBRL="H" (Z Shape)



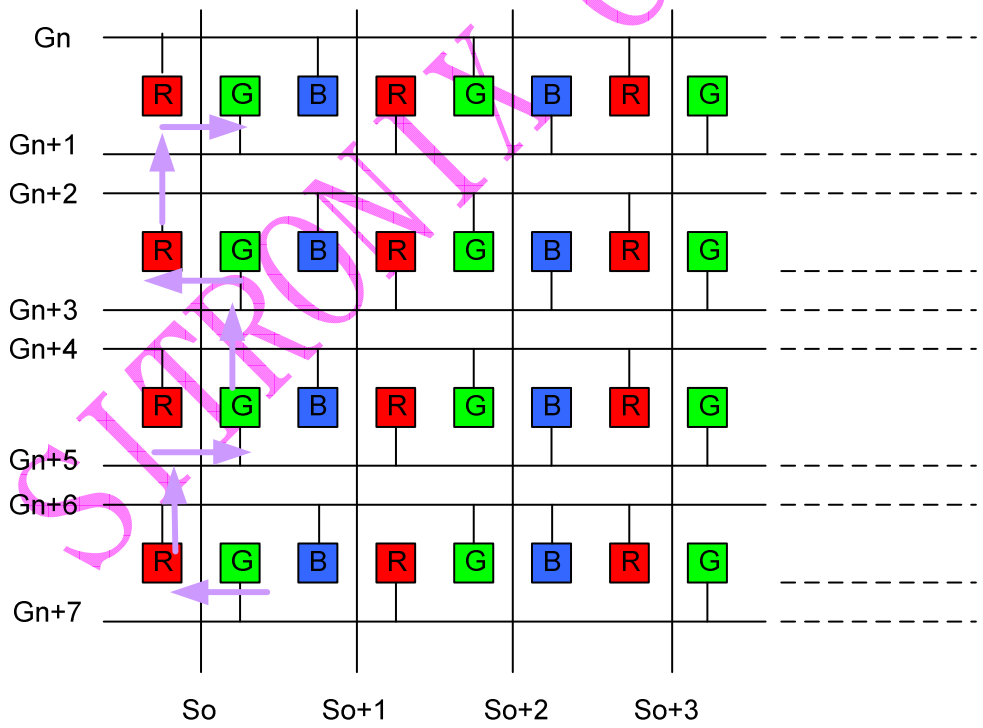
GOSEQ="L" & UPDN="L"=>INVBRR/INVBRL="H" (Z Shape)



GOSEQ="H" & UPDN="H"=>INVBRR/INVBRL="L" (弓 Shape)

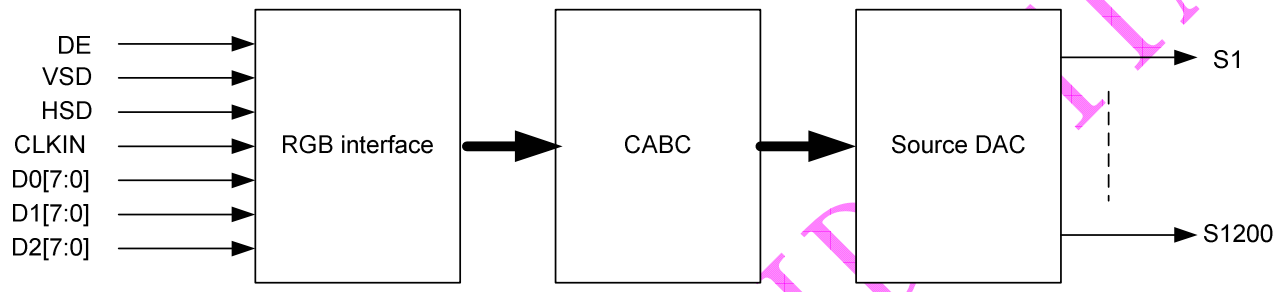


GOSEQ="H" & UPDN="L"=>INVBRR/INVBRL="L" (弓 Shape)

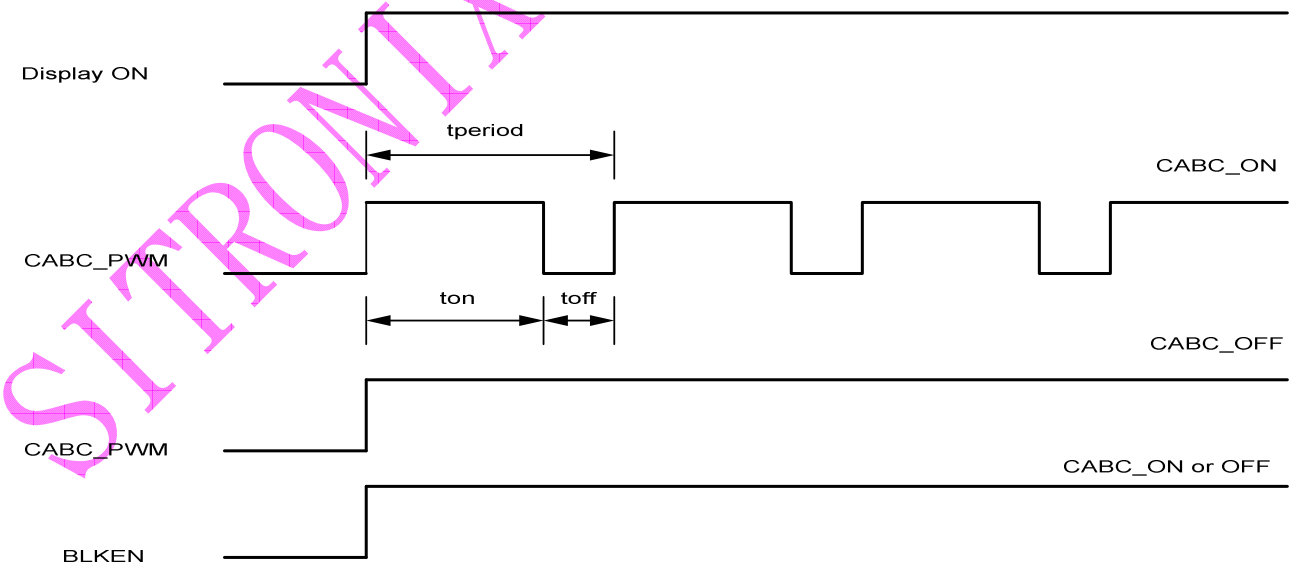


CABC (Content Adaptive Brightness Control)

ST5623 provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. ST5623 will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

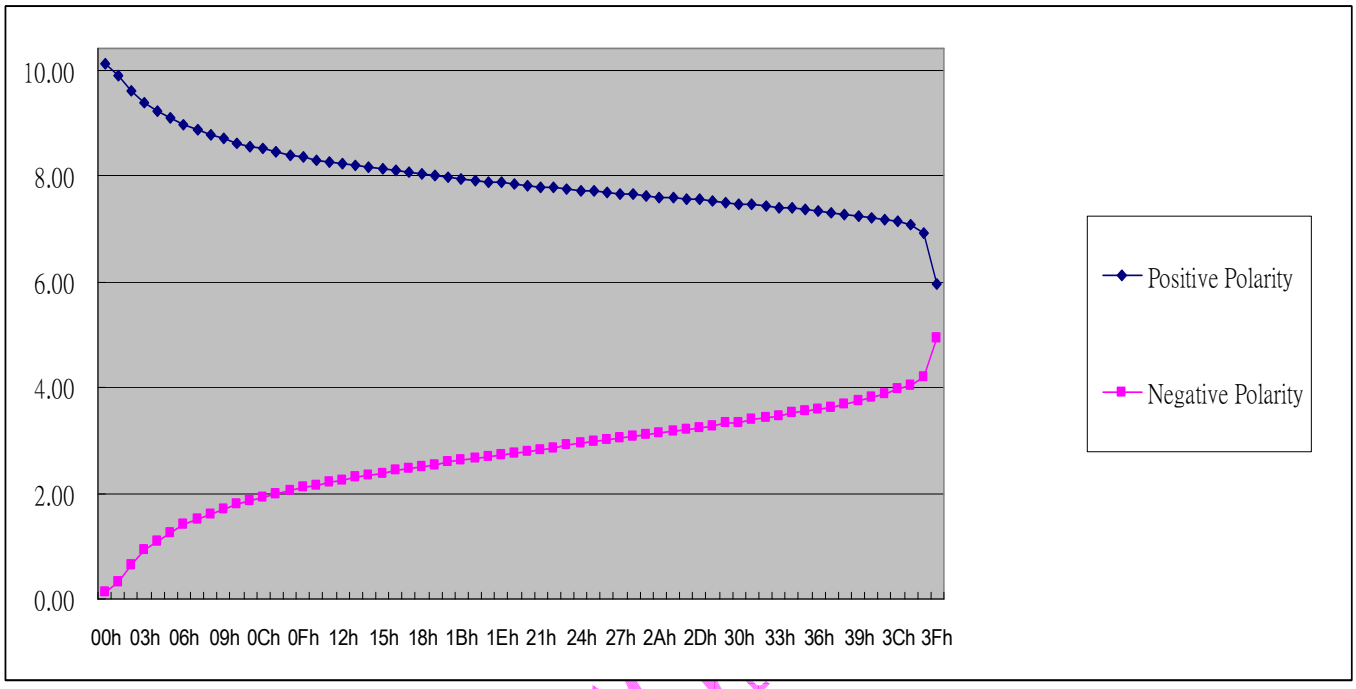


The CABC function can be turned ON/OFF via external pin as CABC_EN and also can be configured by software commands via SPI mode for performance optimization.ST5623 can calculate the backlight brightness level and send a PWM pulse to LED driver via BLKEN pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied ST5623 to control LED driver.



Relationship between Input Data and Output Voltage

The figure below shows the relationship between the input data and the output voltage with the output polarity. The range of V1~V7 is for positive polarity, and V8~V14 for negative polarity. Please refer to the next page to get the R-string resistor value and voltage calculation table.



Note:VDDA-0.1≧V1≧V2≧V3≧V4≧V5≧V6≧V7≧V8≧V9≧V10≧V11≧V12≧V13≧V14≧AGND+0.1

Gamma Correction Resistor Ratio

Display Data(Hex)	Positive Polarity		Negative Polarity	
00h	VDDA X	0.962	VDDA X	0.019598
01h	VDDA X	0.938	VDDA X	0.046119
02h	VDDA X	0.905	VDDA X	0.083529
03h	VDDA X	0.883	VDDA X	0.109285
04h	VDDA X	0.865	VDDA X	0.12996
05h	VDDA X	0.851	VDDA X	0.146395
06h	VDDA X	0.840	VDDA X	0.159756
07h	VDDA X	0.831	VDDA X	0.171244
08h	VDDA X	0.823	VDDA X	0.181228
09h	VDDA X	0.816	VDDA X	0.190248
0Ah	VDDA X	0.810	VDDA X	0.198566
0Bh	VDDA X	0.805	VDDA X	0.205538
0Ch	VDDA X	0.800	VDDA X	0.212346
0Dh	VDDA X	0.795	VDDA X	0.218658
0Eh	VDDA X	0.791	VDDA X	0.224393
0Fh	VDDA X	0.787	VDDA X	0.230035
10h	VDDA X	0.784	VDDA X	0.235175
11h	VDDA X	0.781	VDDA X	0.24012
12h	VDDA X	0.777	VDDA X	0.245052
13h	VDDA X	0.775	VDDA X	0.249372
14h	VDDA X	0.772	VDDA X	0.253994
15h	VDDA X	0.769	VDDA X	0.258138
16h	VDDA X	0.767	VDDA X	0.262134
17h	VDDA X	0.764	VDDA X	0.266387
18h	VDDA X	0.762	VDDA X	0.270174
19h	VDDA X	0.760	VDDA X	0.273866
1Ah	VDDA X	0.758	VDDA X	0.277749
1Bh	VDDA X	0.756	VDDA X	0.281507
1Ch	VDDA X	0.754	VDDA X	0.284932
1Dh	VDDA X	0.753	VDDA X	0.288506
1Eh	VDDA X	0.751	VDDA X	0.292303
1Fh	VDDA X	0.749	VDDA X	0.295628
20h	VDDA X	0.748	VDDA X	0.298992
21h	VDDA X	0.746	VDDA X	0.302483
22h	VDDA X	0.744	VDDA X	0.3059
23h	VDDA X	0.742	VDDA X	0.308842
24h	VDDA X	0.741	VDDA X	0.311887

25h	VDDA X	0.739	VDDA X	0.315036
26h	VDDA X	0.737	VDDA X	0.318369
27h	VDDA X	0.736	VDDA X	0.321407
28h	VDDA X	0.734	VDDA X	0.324539
29h	VDDA X	0.733	VDDA X	0.327767
2Ah	VDDA X	0.731	VDDA X	0.331173
2Bh	VDDA X	0.730	VDDA X	0.334383
2Ch	VDDA X	0.728	VDDA X	0.337684
2Dh	VDDA X	0.727	VDDA X	0.341076
2Eh	VDDA X	0.725	VDDA X	0.344652
2Fh	VDDA X	0.724	VDDA X	0.348236
30h	VDDA X	0.722	VDDA X	0.351912
31h	VDDA X	0.721	VDDA X	0.355689
32h	VDDA X	0.719	VDDA X	0.359704
33h	VDDA X	0.718	VDDA X	0.363864
34h	VDDA X	0.716	VDDA X	0.368123
35h	VDDA X	0.715	VDDA X	0.372563
36h	VDDA X	0.713	VDDA X	0.3776
37h	VDDA X	0.712	VDDA X	0.38275
38h	VDDA X	0.710	VDDA X	0.388237
39h	VDDA X	0.708	VDDA X	0.394664
3Ah	VDDA X	0.706	VDDA X	0.401224
3Bh	VDDA X	0.704	VDDA X	0.40944
3Ch	VDDA X	0.701	VDDA X	0.418345
3Dh	VDDA X	0.697	VDDA X	0.42997
3Eh	VDDA X	0.688	VDDA X	0.446886
3Fh	VDDA X	0.529	VDDA X	0.514095

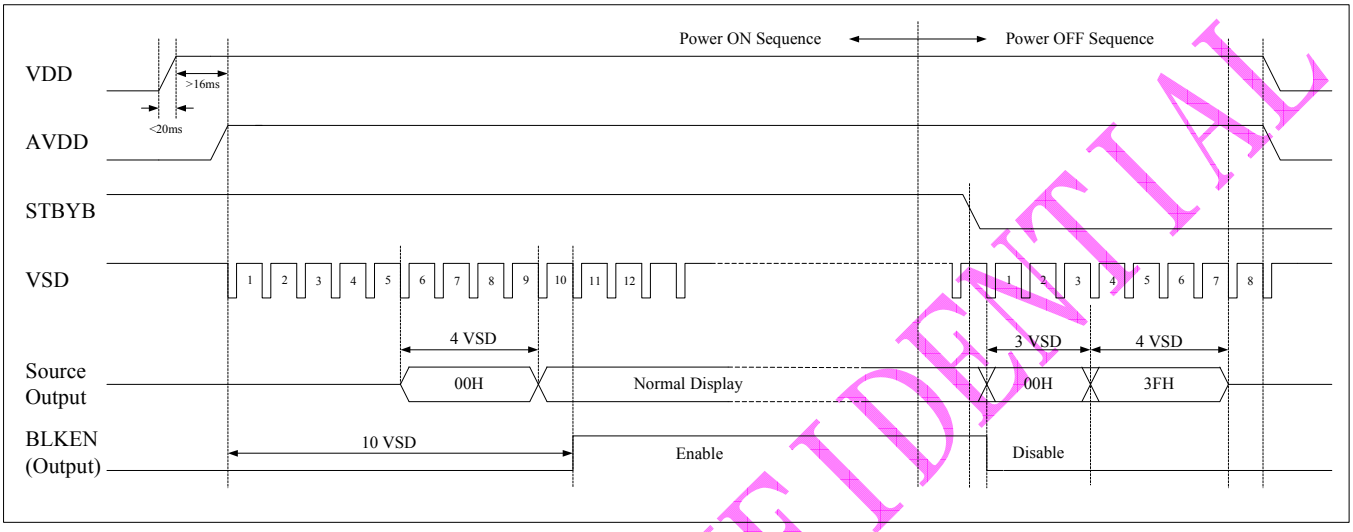
VDDA=10.4

CHIP version	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	**[UNIT]**
	00H	**01H**	**10H**	**20H**	**30H**	**3EH**	**3FH**	**3FH**	**3EH**	**30H**	**20H**	**10H**	**01H**	**00H**	
ST5623	**10.004**	**9.755**	**8.153**	**7.774**	**7.511**	**7.15**	**6.55**	**5.35**	**4.647**	**3.66**	**3.11**	**2.445**	**0.480.**	**0.204**	**V**

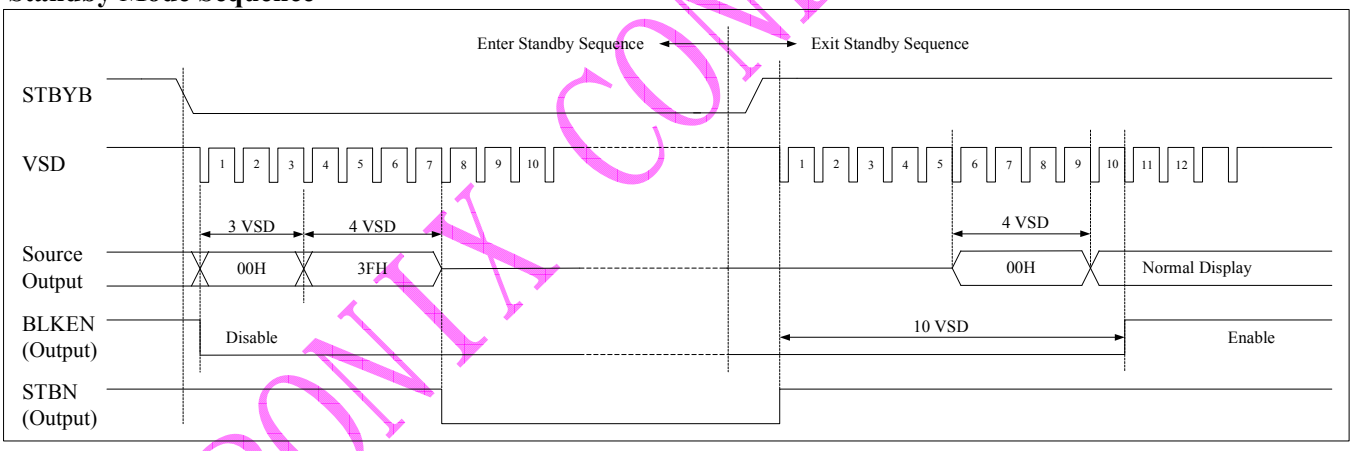
Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

Power-On/Off Timing Sequence

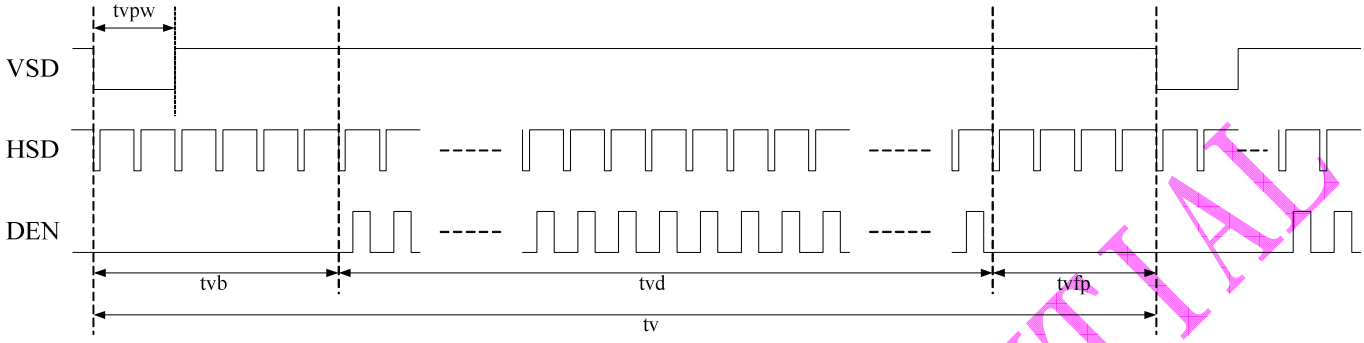


Standby Mode Sequence

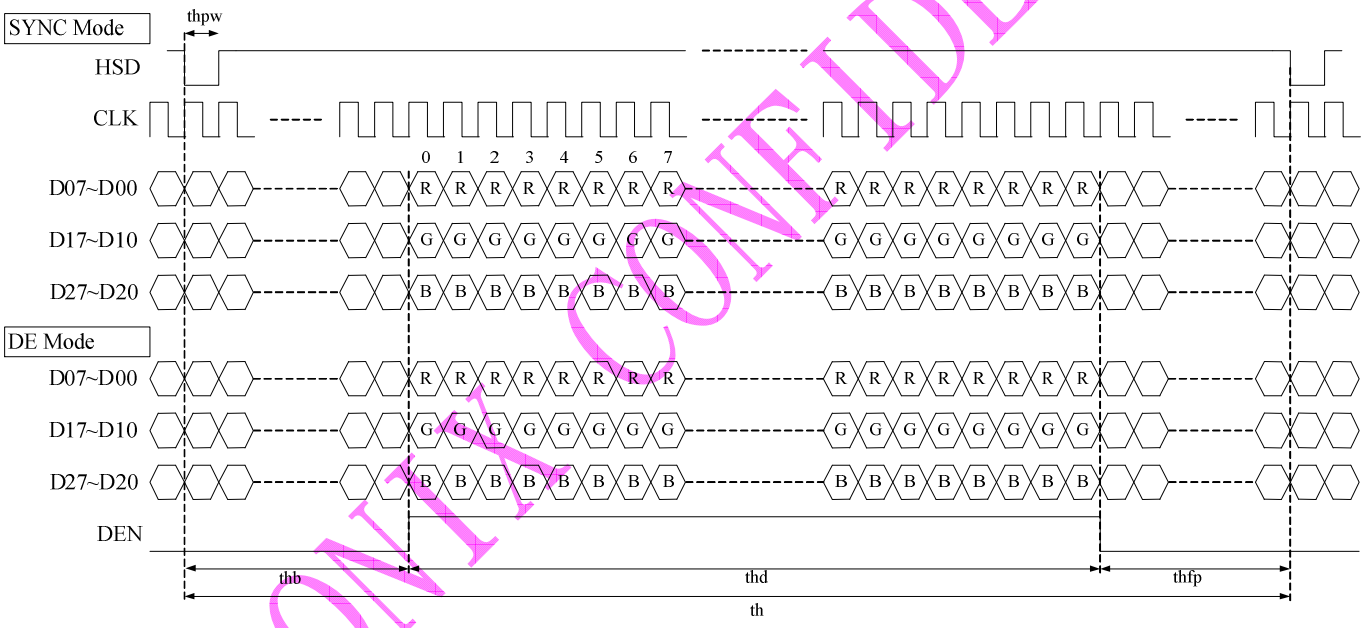


Data Input Format

Vertical input timing



Horizontal input timing



Timing Characteristic

For 800x480 panel

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency		fclk	**Min.**	**Typ.**	**Max.**	
			-	33.3	50	MHz
1 Horizontal Line		th	862	1056	1200	
HSD pulse width	Min.	thpw	1			DCLK
	Typ.		--			
	Max.		40			
HSD Blanking		thb	46	46	46	
HSD Front Porch		thfp	16	210	354	

Vertical input timing

Parameter	Symbol	Value			Uint
		Min.	**Typ.**	**Max.**	
Vertical display area	tvd	480			H
VSD period time	tv	510	525	650	H
VSD pulse width	tvpw	1	-	20	H
VSD Blanking	tvb	23	23	23	H
VSD Front Porch	tvfp	7	22	147	H

For 800x600 panel

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	800			DCLK
DCLK frequency		fclk	**Min.**	**Typ.**	**Max.**	
			-	40	50	MHz
1 Horizontal Line		th	862	1056	1200	DCLK
HSD pulse width	Min.	thpw	1			
	Typ.		--			
	Max.		40			
HSD Blanking		thb	46	46	46	
HSD Front Porch		thfp	16	210	354	

Vertical input timing

Parameter	Symbol	Value			Uint
		Min.	**Typ.**	**Max.**	
Vertical display area	tvd	600			H
VSD period time	tv	624	635	700	H
VSD pulse width	tvpw	1	--	20	H
VSD Blanking	tvb	23	23	23	H
VSD Front Porch	tvfp	1	12	77	H

For 640x480 panel

Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd	640			DCLK
DCLK frequency		fclk	**Min.**	**Typ.**	**Max.**	
			20	24	50	MHz
1 Horizontal Line		th	976	760	1280	DCLK
HSD pulse width	Min.	thpw	1			
	Typ.		--			
	Max.		40			
HSD Blanking		thb	46	46	46	
HSD Front Porch		thfp	290	74	594	

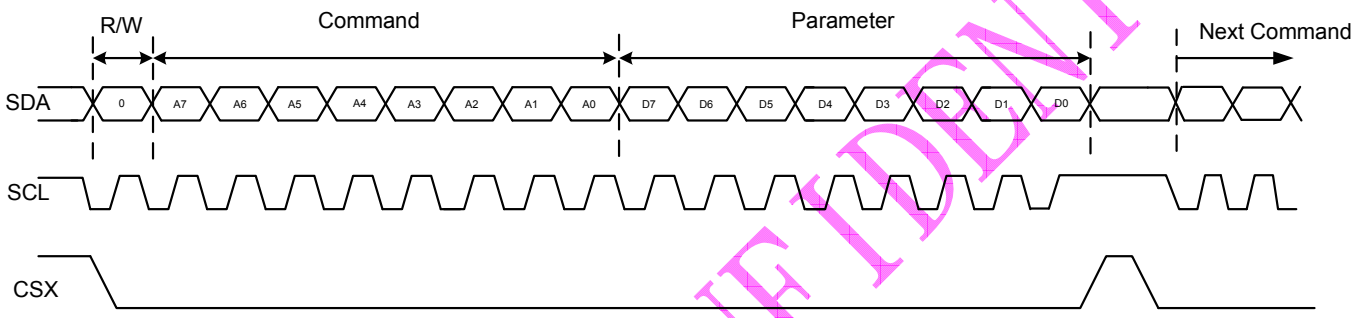
Vertical input timing

Parameter	Symbol	Value			Uint
		Min.	**Typ.**	**Max.**	
Vertical display area	tvd	480			H
VSD period time	tv	510	525	650	H
VSD pulse width	tvpw	1	--	20	H
VSD Blanking	tvb	23	23	23	H
VSD Front Porch	tvfp	7	22	147	H

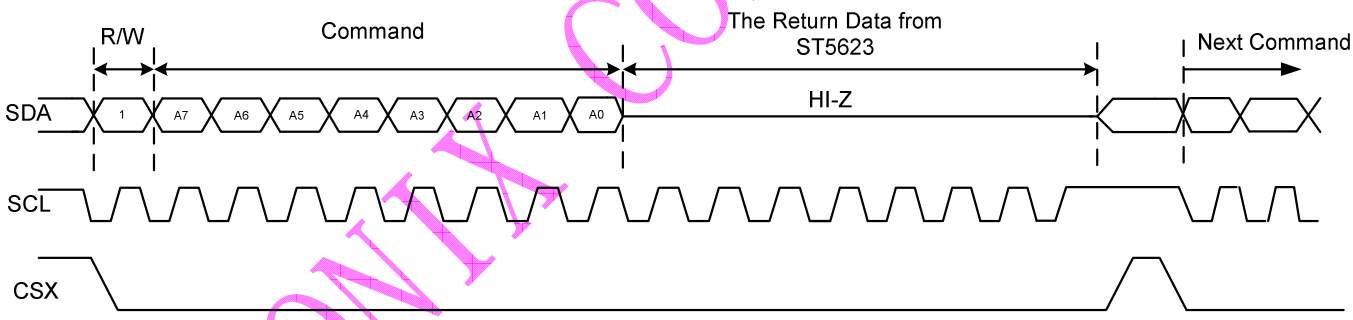
The Command Format for 3-line Serial Interface

ST5623 using the 3-line serial port as communication interface for all the commands and parameters of CABC function. This 3-line serial communication can be bi-directional controlled by the “R/W” bit in address field. Under read mode, the 3-line engine in ST5623 will return the data during “Data phase”. The returned data should be latched at the rising edge of SPCK by external controller. Data in the “Hi-Z phase” will be ignored by 3-line engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under “Hi-Z phase” and “Data phase”.
Each Read/Write operation should be exactly 17 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 17 bit data during a CSX Low period will be ignored by 3-line engine. The timing diagram of read/write operation is illustrated as below:

Write Operation



Read Operation



Command List

Command Function	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Write Display Brightness	0	0	1	0	1	0	0	0	1	51h
	0	DBV[7:0]								XX
Read Display Brightness Value	0	0	1	0	1	0	0	1	0	52h
	1	DBV[7:0]								XX
Write CTRL Display	0	0	1	0	1	0	0	1	1	53h
	0	0	0	0	0	DD	BL	0	0	XX
Read CTRL Display	0	0	1	0	1	0	1	0	0	54h
	1	0	0	0	0	DD	BL	0	0	XX
Write Content Adaptive Brightness Control	0	0	1	0	1	0	1	0	1	55h
	0	0	0	0	0	0	0	C[1:0]		XX
Read Content Adaptive Brightness Control	0	0	1	0	1	0	1	1	0	56h
	1	0	0	0	0	0	0	C[1:0]		XX
Write CABC Minimum Brightness	0	0	1	0	1	1	1	1	0	5Eh
	0	CMB[7:0]								XX
Read CABC Minimum Brightness	0	0	1	0	1	1	1	1	1	5Fh
	1	CMB[7:0]								XX
CABC Control 1	0	0	1	1	0	0	0	0	0	60h
	0	bl_tune_ui		bl_tune_still		bl_tune_movie				XX
CABC Control 2	0	0	1	1	0	0	0	0	1	61h
	0	Dim_still_tune			Dim_movie_tune					XX
CABC Control 3	0	0	1	1	0	0	0	1	0	62h
	0	lut_tune_cabc			pwm_period			force_bl		XX

Note : 1. These commands above can be transmitted from host to driver IC via 3-line SPI mode only.
2. When R/W in the table above is '0', it means the "Write" operation is executed and the "Read" operation is executed when R/W is set to '1'

Command Description

Write Display Brightness Value (51h)

51h	WRDISBV(Write Display Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	0	1	51h
Parameter	DBV[7:0]								XX
Description	This command is used to adjust the brightness value of the display. **DBV[7:0]**: 8 bit, for display brightness of manual brightness setting and CABC in ST5623. There is a PWM output signal, CABC_PWM pin to control the LED driver IC in order to control display brightness.								

Read Display Brightness Value (52h)

52h	RDDISBV(Read Display Brightness Value)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	1	0	52h
Parameter	DBV[7:0]								XX
Description	This command is used to return the brightness value of the display. DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when BL bit is '1'.								

Write CTRL Display Value (53h)

53h	WRCTRLD(Write Control Display)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	0	1	1	53h
Parameter	X	X	X	X	DD	BL	X	X	XX
Description	**DD**: Display Dimming Control. This function is only for manual brightness setting. DD: 0 = Display Dimming OFF; 1 = Display Dimming ON **BL**: Backlight Control On/Off BL: 0 = Backlight Control OFF; 1 = Backlight Control ON When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected X=Don't care								

Read CTRL Display Value (54h)

54h	RDCTRLD(Read Control Display)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	0	0	54h
Parameter	X	X	X	X	DD	BL	X	X	XX
Description	**DD**: Display Dimming Control. This function is only for manual brightness setting. DD: 0 = Display Dimming OFF; 1 = Display Dimming ON **BL**: Backlight Control On/Off BL: 0 = Backlight Control OFF; 1 = Backlight Control ON X=Don't care								

Write Content Adaptive Brightness Control Value (55h)

55h	WRCABC(Write Control Display)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	0	1	55h
Parameter	0	0	0	0	0	0	C[1:0]		XX
Description	This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. C[1:0] 0 0 = CABC OFF; 0 1 = User Interface Image; 1 0 = Still Picture; 1 1 = Moving image X=Don't care								

Read Content Adaptive Brightness Control Value (56h)

56h	RDCABC(Read Control Display)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	0	1	1	0	56h
Parameter	0	0	0	0	0	0	C[1:0]		XX
Description	This command is used to read the settings for image content based adaptive brightness control functionality. There is Possible to use 4 different modes for content adaptive image functionality which are defined on the table below. C[1:0] 0 0 = CABC OFF; 0 1 = User Interface Image; 1 0 = Still Picture; 1 1 = Moving image X=Don't care								

Write CABC Minimum Brightness(5Eh)

5Eh	WRCABCMB(Write CABC Minimum Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	0	5Eh
Parameter	CMB[7:0]								XX
Description	This command is used to set the minimum brightness value of the display for CABC function. **CMB[7:0]**: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.								

Read CABC Minimum Brightness(5Fh)

5Fh	RDCABCMB(Read CABC Minimum Brightness)								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	0	1	1	1	1	1	5Fh
Parameter	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (5Eh)” command.								

60h	Backlight fine tune								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	60h
Parameter	bl_tune_ui		bl_tune_still		bl_tune_movie				XX
Description	bl_tune_ui:back light fine tune for UI bl_tune_still:back light fine tune for still picture bl_tune_movie:back light fine tune for movie bl_tune_ui: 00: Back light control dynamic range from 128~255 01: Back light control dynamic range from 160~255 10: Back light control dynamic range from 192~255 11: Back light control dynamic range from 224~255 bl_tune_still: 00: Back light control dynamic range from 128~255 01: Back light control dynamic range from 160~255 10: Back light control dynamic range from 192~255 11: Back light control dynamic range from 224~255 bl_tune_movie: 00: Back light control dynamic range from 128~255 01: Back light control dynamic range from 160~255 10: Back light control dynamic range from 192~255 11: Back light control dynamic range from 224~255								

61h	Dimming setting								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	1	61h
Parameter	Dim_still_tune			Dim_movie_tune					XX
Description	dim_still_tune: 000: every frame jump to target brightness value 001: brightness change 127/256 * 100% / frame 010: brightness change 64/256 * 100% / frame 011: brightness change 32/256 * 100% / frame 100: brightness change 16/256 * 100% / frame 101: brightness change 8/256 * 100% / frame 110: brightness change 4/256 * 100% / frame 111: brightness change 2/256 * 100% / frame dim_movie_tune: 000: every frame jump to target brightness value 001: brightness change 127/256 * 100% / frame 010: brightness change 64/256 * 100% / frame 011: brightness change 32/256 * 100% / frame 100: brightness change 16/256 * 100% / frame 101: brightness change 8/256 * 100% / frame 110: brightness change 4/256 * 100% / frame 111: brightness change 2/256 * 100% / frame								

62h	Other setting								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	1	0	62h
Parameter	lut_tune_cabc			pwm_period			force_bl		
Description	Lut_tune_cabc:data transfer LUT setting , This function just run in CABC mode. 000: data transfer curve slope rate 0/128 001: data transfer curve slope rate 1/128 010: data transfer curve slope rate 2/128 011: data transfer curve slope rate 3/128 100: data transfer curve slope rate 4/128 101: data transfer curve slope rate 5/128 110: data transfer curve slope rate 6/128 111: data transfer curve slope rate 7/128 Pwm_period: pwm period setting 3'b000:sig_pwm period= osc period*256*1=20ns*256*16*1=82us 3'b001:sig_pwm period= osc period*256*1=20ns*256*16*2=164us 3'b010:sig_pwm period= osc period*256*1=20ns*256*16*4=328us 3'b011:sig_pwm period= osc period*256*1=20ns*256*16*8=656us 3'b100:sig_pwm period= osc period*256*1=20ns*256*16*16=1312us 3'b101:sig_pwm period= osc period*256*1=20ns*256*16*32=2624us 3'b110:sig_pwm period= osc period*256*1=20ns*256*16*64=5248us 3'b111:sig_pwm period= osc period*256*1=20ns*256*16*128=10496us force_bl 0: force_bl = Low , the PWM will be controlled by CABC 1: force_bl = High, the PWM will still keep high								

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Digital supply voltage	VDD	-0.5 to 5.0	V
Analog supply voltage,	VDDA	-0.5 to 13.5	V
Storage temperature	---	-55 to +125	℃
Operating temperature	---	-20 to +85	℃

CAUTIONS：

Stresses beyond "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operations beyond those indicated under " typical operating conditions" is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Recommended Operating Range

(DGND = AGND = 0V, TA = -20 to +85℃)

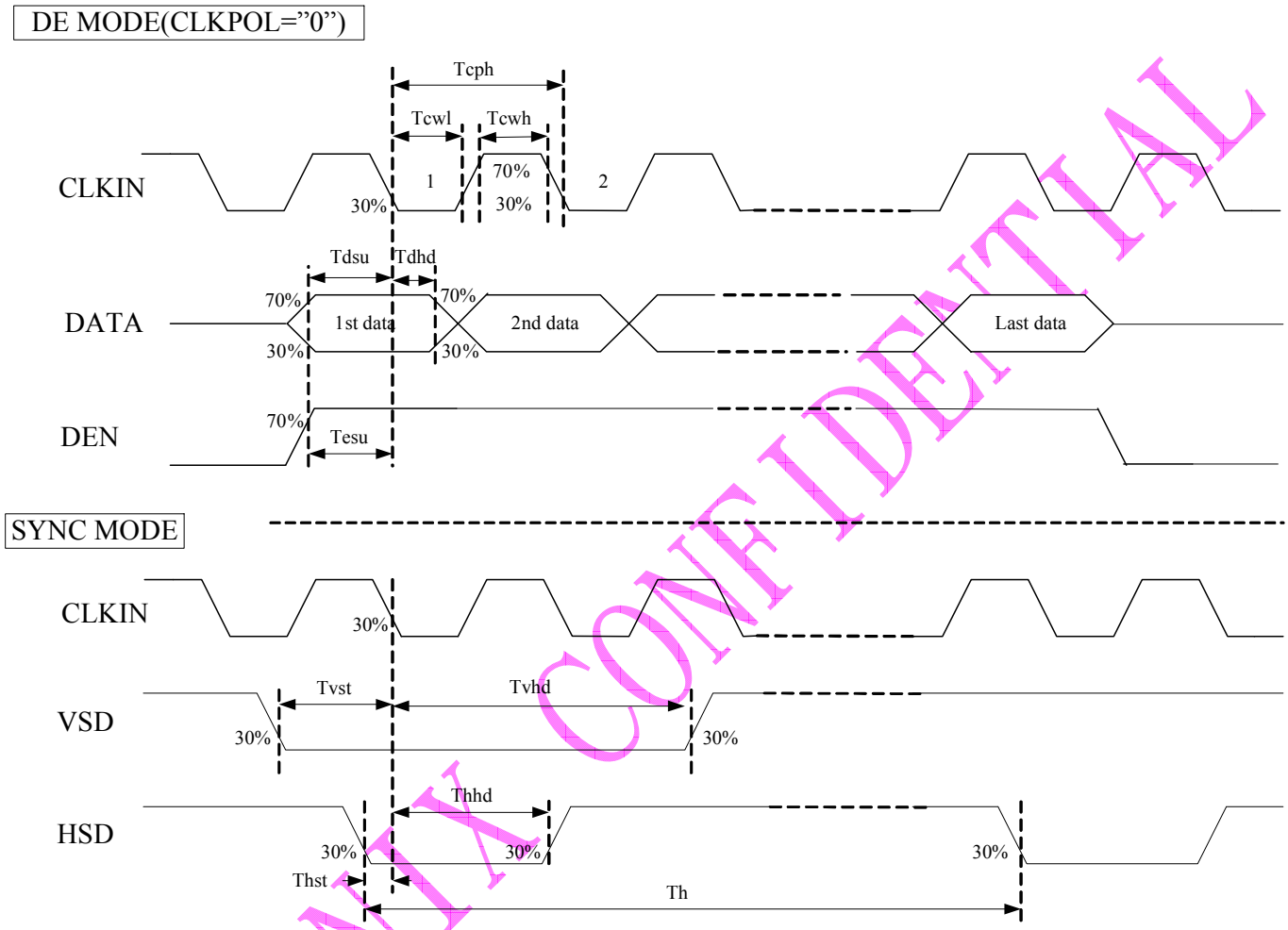
Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	3.0	3.3	3.6	V
Analog supply voltage,	VDDA	6.5	10.4	13.5	V
Digital input voltage	VIN	0	--	VCC	V

DC Electrical Characteristics (VDD=3.0~3.6V, VDDA=6.5~13.5V, DGND=AGND=0V, TA=-20~85℃)

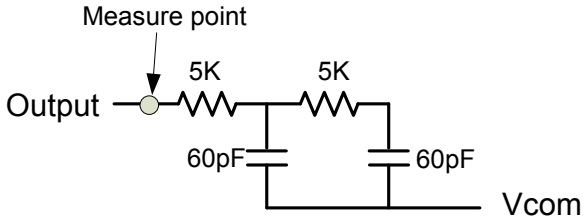
Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
Power supply voltage	**VDD**	3.0	3.3	3.6		
Power supply voltage	**VDDA**	6.5	10.4	13.5		
Low level input voltage	**Vil**	0	-	0.3xVDD	V	For digital circuit
High level input voltage	**Vih**	0.7xVDD	-	VDD	V	For digital circuit
Input leakage current	**Ii**	-	-	+/-1	uA	For digital circuit
High level output voltage	**Voh**	VDD-0.4	-	-	V	Ioh=-400uA
Low level output voltage	**Vol**	-	-	DGND+0.4	V	Iol=+400uA
Pull low/high resistor	**Ri**	200K	250K	300K	Ohm	For the digital input pin@VDD=3.3V
Digital Operation Current	**Idd**	-	8	10	mA	Fclk=50MHz, FLD=48KHz, VDD=3.3V
Digital Stand-by current	**Ist1**	-	10	50	uA	Clock & all functions are stopped
Analog Operation Current	**Idda**	-	10	12	mA	No load Fclk=50Mhz, FLD=48K@VDDA=10V, V1=8V, V14=0.4V
Analog Stand-by Current	**Ist2**	-	10	50	uA	No load. Clock & all functions are stopped
Input Level of V1~V7	**Vref1**	0.4*VDDA	-	VDDA-0.1	V	Gamma correction voltage input
Input Level of V8~V14	**Vref2**	0.1	-	0.6*VDDA	V	Gamma correction voltage input
Output Voltage deviation	**Vod1**	-	+/- 20	+/- 35	mV	Vo=AGND+0.1V~ AGND +0.5V& Vo= VDDA -0.5V~VDDA-0.1V
Output Voltage deviation	**Vod2**	-	+/- 15	+/- 20	mV	Vo=AGND+0.5V~VDDA-0.5V
Output Voltage offset between chips	**Voc**	-	-	+/- 20	mV	Vo=AGND+0.5V~VDDA-0.5V
Dynamic Range of Output	**Vdr**	0.1	-	VDDA-0.1	V	SO1~SO1200
Sinking current of Output	**IOLy**	80	-	-	uA	SO1~SO1200; Vo=0.1V vs. 1.0V, VDDA=13.5V
Driving current of outputs	**IOHy**	80	-	-	uA	SO1~SO1200; Vo=13.4V vs. 12.5V, VDDA=13.5V
Resistance of Gamma Table	**Rg**	0.7*Rn	1.0*Rn	1.3*Rn	ohm	Rn:Internal gamma resistor

Timing Diagram

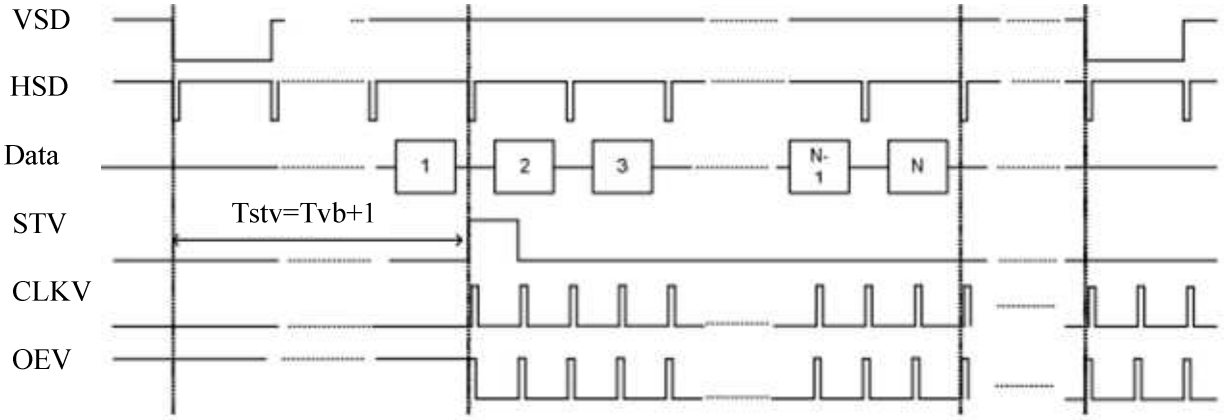
Input Clock and Data Timing Diagram



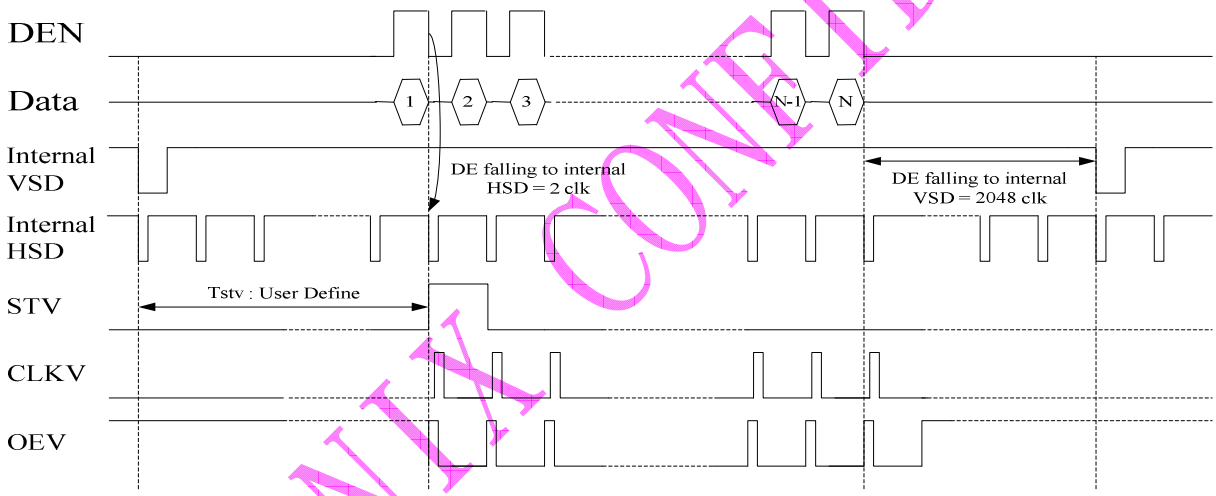
Output Load Condition



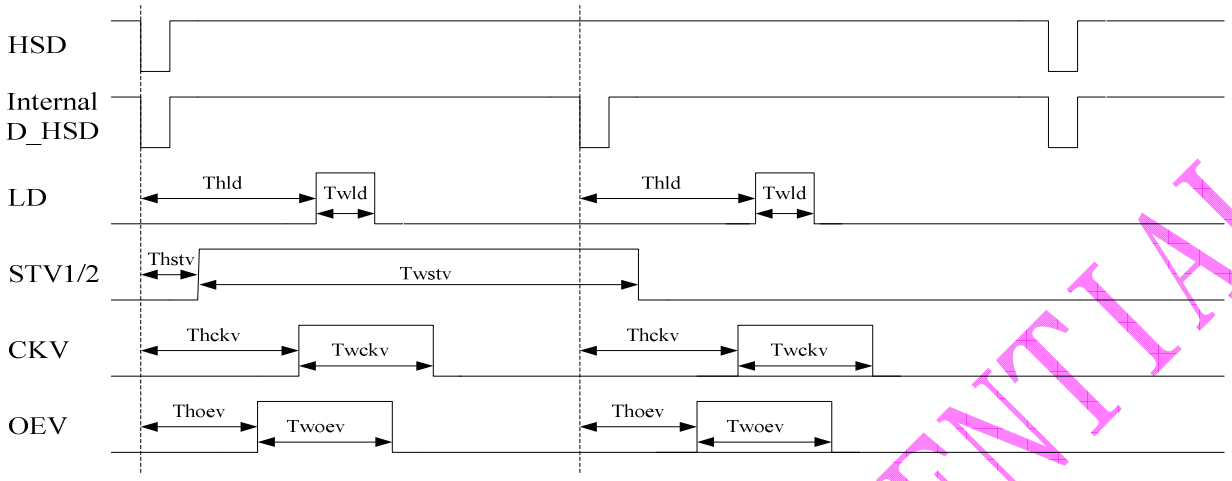
Vertical Timing Diagram SYNC (Dual Gate)



Vertical Timing Diagram DE (Dual Gate)



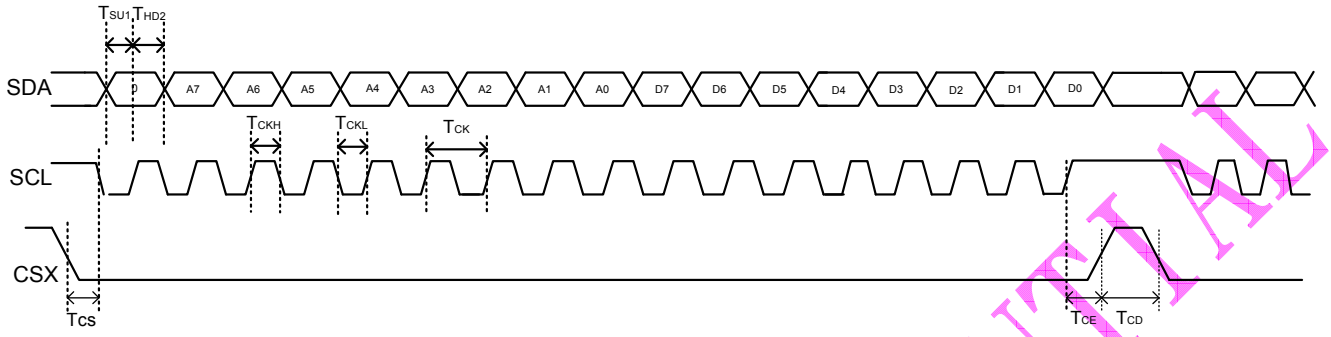
Gate output Timing Diagram (Dual Gate)



AC Electrical Characteristics (VDD =3.0~3.6V, VDDA=6.5~13.5V, AGND=DGND=0V, TA= -20~85℃)

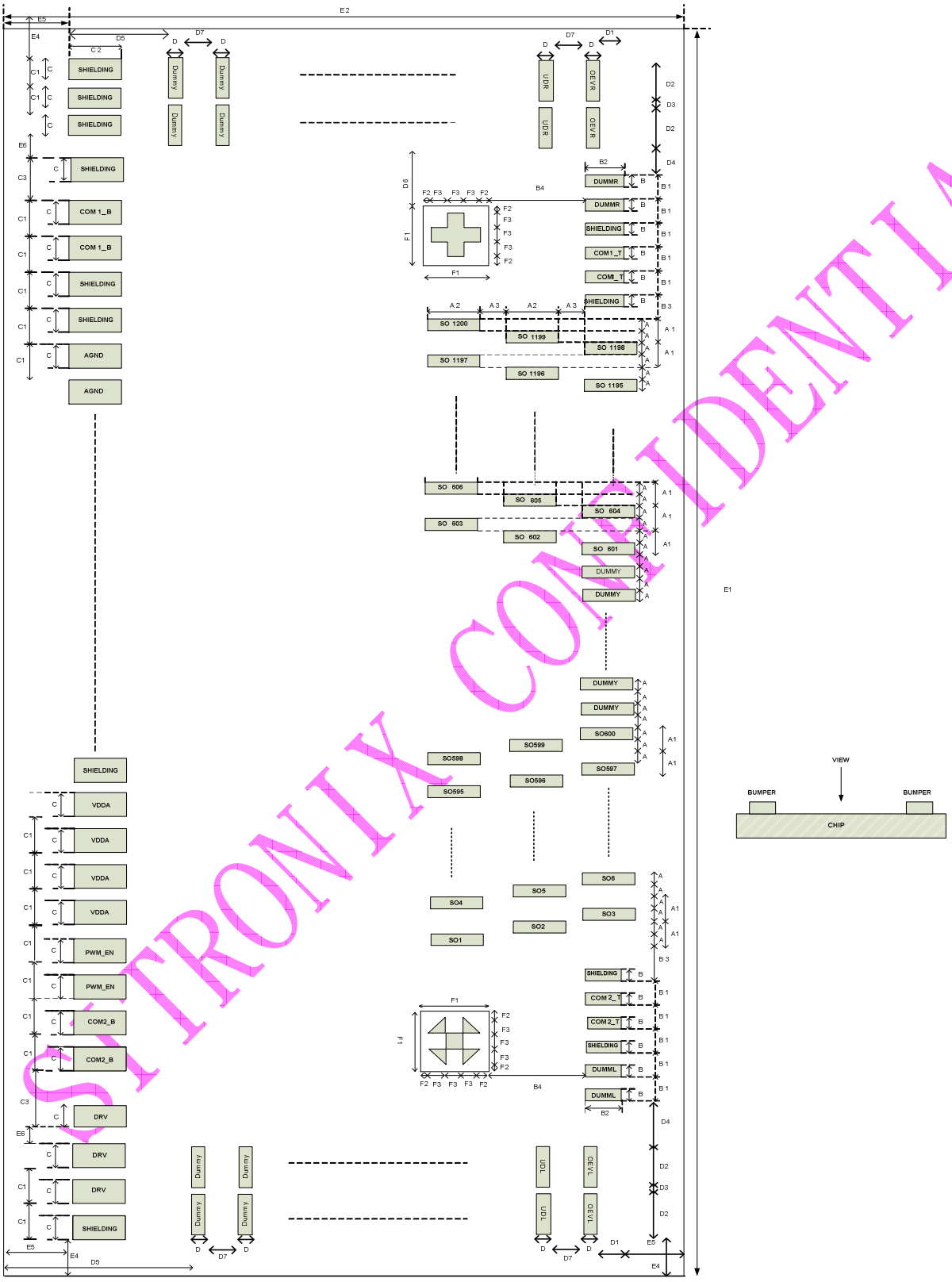
Parameter	Symbol	Min	Typ.	Max.	Unit	Conditions
VDD Power on Slew Rate	T_{POR}	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	T_{RST}	10	-	-	us	Clkin=50MHz
CLKIN cycle time	Tcph	20			ns	
CLKIN pulse duty	Tcwh	40	50	60	%	
VSD setup time	Tvst	8	-	-	ns	
VSD hold time	Tvhd	8	-	-	ns	
HSD setup time	Thst	8	-	-	ns	
HSD hold time	Thhd	8	-	-	ns	
Data setup time	Tdsu	8	-	-	ns	D[7:0], D1[7:0], D2[7:0] to clkin
Date hold time	Tdhd	8	-	-	ns	D[7:0], D1[7:0], D2[7:0] to clkin
DE setup time	Tesu	8	-	-	ns	
DE hold time	Tehd	8	-	-	ns	
Output stable time	Tsst	-	-	6	us	10% to 90% target voltage. CL=120pF, R=10Kohm
CLKIN Frequency	Fclk	-	40	50	MHz	VDD=3.0V~3.6V
CLKIN Cycle Time	Tclk	20	25	-	ns	
CLKIN Pulse Duty	Tcwh	40	50	60	%	Tclk
Time from HSD to Source Output	Thso	-	20	-	CLKIN	
Time from HSD to LD	Thld	-	20	-	CLKIN	
Time from HSD to STV	Thstv	-	2	-	CLKIN	
Time from HSD to CKV	Thckv	-	20	-	CLKIN	
Time from HSD to OEV	Thoev	-	4	-	CLKIN	
LD pulse width	Twld	-	10	-	CLKIN	
CKV pulse width	Twckv	-	66	-	CLKIN	
OEV pulse width	Twoev	-	74	-	CLKIN	

SPI timing



Parameter		Min	Typ.	Max.		
SCL period	T_{ck}	60			ns	
SCL high width	T_{CKH}	30			ns	
SCL low width	T_{CKL}	30			ns	
Data setup time	T_{SU1}	12			ns	
Data hold time	T_{HD1}	12			ns	
CSX to SCL setup time	T_{CS}	20			ns	
CSX to SDA hold time	T_{CE}	20			ns	
CSX high pulse width	T_{CD}	50			ns	

Chip Outline Dimensions and Coordination (Bump Side)



Pad Dimension

Symbol	Dimension(um)	Symbol	Dimension(um)
A	17	D2	100
A1	34	D3	30
A2	110	D4	70
A3	30	D5	266
B	30	D6	168.5
B1	50	D7	50
B2	70	E1	22578
B3	50	E2	1045
B4	191.5	E3	TBD
C	65	E4	57
C1	85	E5	57
C2	110	E6	136.5
C3	115	F1	115
D	30	F2	20
D1	40	F3	25

Pad Coordination

No.	NAME	X	Y
1	INVBRR	-11179	408
2	OEVR	-11179	328
3	UDR	-11179	248
4	UDR	-11049	248
5	CKVR	-11179	168
6	CKVR	-11049	168
7	STV1R	-11179	88
8	STV1R	-11049	88
9	STV2R	-11179	8
10	STV2R	-11049	8
11	STV1R	-11179	-72
12	STV1R	-11049	-72
13	STBNR	-11179	-152
14	STBNR	-11049	-152
15	DUMMR	-11179	-232
16	DUMMR	-11049	-232
17	SHIELDING	-11196.5	-408
18	SHIELDING	-11111.5	-408
19	SHIELDING	-11026.5	-408
20	SHIELDING	-10825	-408
21	COM1_B	-10710	-408
22	COM1_B	-10625	-408
23	SHIELDING	-10540	-408
24	SHIELDING	-10455	-408
25	AGND	-10370	-408
26	AGND	-10285	-408
27	AGND	-10200	-408
28	AGND	-10115	-408
29	SHIELDING	-10030	-408
30	SHIELDING	-9945	-408
31	SHIELDING	-9860	-408
32	SHIELDING	-9775	-408
33	SHIELDING	-9690	-408
34	SHIELDING	-9605	-408
35	TP0	-9520	-408
36	TP0	-9435	-408
37	TP1	-9350	-408
38	TP1	-9265	-408
39	TP2	-9180	-408
40	TP2	-9095	-408
41	TP3	-9010	-408
42	TP3	-8925	-408
43	TP4	-8840	-408
44	TP4	-8755	-408
45	Dummy	-8670	-408
46	REV	-8585	-408
47	SHIELDING	-8500	-408
48	INVSEL	-8415	-408
49	INVSEL	-8330	-408
50	SHIELDING	-8245	-408
51	CABC_EN	-8160	-408
52	CABC_EN	-8075	-408
53	SHIELDING	-7990	-408
54	SHIELDING	-7905	-408
55	SHIELDING	-7820	-408
56	SHIELDING	-7735	-408
57	CSX	-7650	-408
58	CSX	-7565	-408
59	SHIELDING	-7480	-408
60	SCL/DBCM[0]	-7395	-408
61	SCL/DBCM[0]	-7310	-408
62	SHIELDING	-7225	-408
63	SDA/DBCM[1]	-7140	-408
64	SDA/DBCM[1]	-7055	-408
65	SHIELDING	-6970	-408
66	SHIELDING	-6885	-408
67	GOSEQ	-6800	-408
68	GOSEQ	-6715	-408
69	SHIELDING	-6630	-408
70	BIST	-6545	-408
71	BIST	-6460	-408
72	SHIELDING	-6375	-408
73	RES0	-6290	-408
74	RES0	-6205	-408
75	SHIELDING	-6120	-408
76	DBC/3	-6035	-408
77	DBC/3	-5950	-408
78	SHIELDING	-5865	-408
79	CLKPOL	-5780	-408
80	CLKPOL	-5695	-408
81	SHIELDING	-5610	-408
82	DITHB	-5525	-408
83	DITHB	-5440	-408
84	SHIELDING	-5355	-408
85	MODE	-5270	-408
86	MODE	-5185	-408
87	SHIELDING	-5100	-408
88	SHLR	-5015	-408
89	SHLR	-4930	-408
90	SHIELDING	-4845	-408
91	UPDN	-4760	-408
92	UPDN	-4675	-408
93	SHIELDING	-4590	-408
94	STBYB	-4505	-408
95	STBYB	-4420	-408
96	SHIELDING	-4335	-408
97	RSTB	-4250	-408
98	RSTB	-4165	-408
99	SHIELDING	-4080	-408
100	BLKEN	-3995	-408
101	BLKEN	-3910	-408
102	SHIELDING	-3825	-408
103	VSET	-3740	-408
104	VSET	-3655	-408
105	TP6	-3570	-408
106	TP6	-3485	-408
107	TP7	-3400	-408
108	TP7	-3315	-408
109	TP8	-3230	-408
110	TP8	-3145	-408
111	TP9	-3060	-408
112	TP9	-2975	-408
113	TP10	-2890	-408
114	Dummy	-2805	-408
115	RES1	-2720	-408
116	DUMMY	-2635	-408
117	SHIELDING	-2550	-408
118	VDDA	-2465	-408
119	VDDA	-2380	-408
120	VDDA	-2295	-408
121	VDDA	-2210	-408
122	VDDA	-2125	-408
123	VDDA	-2040	-408
124	VDDA	-1955	-408
125	VDDA	-1870	-408
126	SHIELDING	-1785	-408
127	V1	-1700	-408
128	V1	-1615	-408
129	SHIELDING	-1530	-408
130	V2	-1445	-408
131	V2	-1360	-408
132	SHIELDING	-1275	-408
133	V3	-1190	-408
134	V3	-1105	-408
135	SHIELDING	-1020	-408
136	V4	-935	-408
137	V4	-850	-408
138	SHIELDING	-765	-408
139	V5	-680	-408
140	V5	-595	-408
141	SHIELDING	-510	-408
142	V6	-425	-408
143	V6	-340	-408
144	SHIELDING	-255	-408
145	V7	-170	-408
146	V7	-85	-408
147	SHIELDING	0	-408
148	V8	85	-408
149	V8	170	-408
150	SHIELDING	255	-408
151	V9	340	-408
152	V9	425	-408
153	SHIELDING	510	-408
154	V10	595	-408
155	V10	680	-408
156	SHIELDING	765	-408
157	V11	850	-408
158	V11	935	-408
159	SHIELDING	1020	-408
160	V12	1105	-408
161	V12	1190	-408
162	SHIELDING	1275	-408
163	V13	1360	-408
164	V13	1445	-408
165	SHIELDING	1530	-408
166	V14	1615	-408
167	V14	1700	-408
168	SHIELDING	1785	-408
169	AGND	1870	-408
170	AGND	1955	-408
171	AGND	2040	-408
172	AGND	2125	-408
173	AGND	2210	-408
174	AGND	2295	-408
175	AGND	2380	-408
176	AGND	2465	-408
177	SHIELDING	2550	-408
178	SHIELDING	2635	-408
179	DGND	2720	-408
180	DGND	2805	-408
181	DGND	2890	-408
182	DGND	2975	-408
183	SHIELDING	3060	-408
184	SHIELDING	3145	-408
185	VDD	3230	-408
186	VDD	3315	-408
187	VDD	3400	-408
188	VDD	3485	-408
189	DASHD	3570	-408
190	VSD	3655	-408
191	VSD	3740	-408
192	DASHD	3825	-408
193	HSD	3910	-408
194	HSD	3995	-408
195	DASHD	4080	-408
196	DEN	4165	-408
197	DEN	4250	-408
198	DASHD	4335	-408
199	CLKIN	4420	-408
200	CLKIN	4505	-408
201	DASHD	4590	-408
202	D2[7]	4675	-408
203	D2[7]	4760	-408
204	D2[6]	4845	-408
205	D2[6]	4930	-408
206	DASHD	5015	-408
207	D2[5]	5100	-408
208	D2[5]	5185	-408
209	D2[4]	5270	-408
210	D2[4]	5355	-408
211	DASHD	5440	-408
212	D2[3]	5525	-408
213	D2[3]	5610	-408
214	D2[2]	5695	-408
215	D2[2]	5780	-408
216	DASHD	5865	-408
217	D2[1]	5950	-408
218	D2[1]	6035	-408
219	D2[0]	6120	-408
220	D2[0]	6205	-408
221	DASHD	6290	-408
222	D1[7]	6375	-408
223	D1[7]	6460	-408
224	D1[6]	6545	-408
225	D1[6]	6630	-408
226	DASHD	6715	-408
227	D1[5]	6800	-408
228	D1[5]	6885	-408
229	D1[4]	6970	-408
230	D1[4]	7055	-408
231	DASHD	7140	-408
232	D1[3]	7225	-408
233	D1[3]	7310	-408
234	D1[2]	7395	-408
235	D1[2]	7480	-408
236	DASHD	7565	-408
237	D1[1]	7650	-408
238	D1[1]	7735	-408
239	D1[0]	7820	-408
240	D1[0]	7905	-408

No.	NAME	X	Y
241	DASHD	7990	-408
242	D0[7]	8075	-408
243	D0[7]	8160	-408
244	D0[6]	8245	-408
245	D0[6]	8330	-408
246	DASHD	8415	-408
247	D0[5]	8500	-408
248	D0[5]	8585	-408
249	D0[4]	8670	-408
250	D0[4]	8755	-408
251	DASHD	8840	-408
252	D0[3]	8925	-408
253	D0[3]	9010	-408
254	D0[2]	9095	-408
255	D0[2]	9180	-408
256	DASHD	9265	-408
257	D0[1]	9350	-408
258	D0[1]	9435	-408
259	D0[0]	9520	-408
260	D0[0]	9605	-408
261	DASHD	9690	-408
262	SHIELDING	9775	-408
263	FB	9860	-408
264	FB	9945	-408
265	SHIELDING	10030	-408
266	VDDA	10115	-408
267	VDDA	10200	-408
268	VDDA	10285	-408
269	VDDA	10370	-408
270	PWM_EN	10455	-408
271	PWM_EN	10540	-408
272	COM2_B	10625	-408
273	COM2_B	10710	-408
274	DRV	10825	-408
275	DRV	11026.5	-408
276	DRV	11111.5	-408
277	SHIELDING	11196.5	-408
278	DUMML	11049	-232
279	DUMML	11179	-232
280	STBNL	11049	-152
281	STBNL	11179	-152
282	STV1L	11049	-72
283	STV1L	11179	-72
284	STV2L	11049	8
285	STV2L	11179	8
286	STV1L	11049	88
287	STV1L	11179	88
288	CKVL	11049	168
289	CKVL	11179	168
290	UDL	11049	248
291	UDL	11179	248
292	OEVL	11179	328
293	INVBRL	11179	408
294	INVBRL	11049	408
295	OEVL	11049	328
296	DUMML	10914	428
297	DUMML	10864	428
298	SHIELDING	10814	428
299	COM2_T	10764	428
300	COM2_T	10714	428

No.	NAME	X	Y
301	SHIELDING	10664	428
302	SO[1]	10620.5	128
303	SO[2]	10603.5	268
304	SO[3]	10586.5	408
305	SO[4]	10569.5	128
306	SO[5]	10552.5	268
307	SO[6]	10535.5	408
308	SO[7]	10518.5	128
309	SO[8]	10501.5	268
310	SO[9]	10484.5	408
311	SO[10]	10467.5	128
312	SO[11]	10450.5	268
313	SO[12]	10433.5	408
314	SO[13]	10416.5	128
315	SO[14]	10399.5	268
316	SO[15]	10382.5	408
317	SO[16]	10365.5	128
318	SO[17]	10348.5	268
319	SO[18]	10331.5	408
320	SO[19]	10314.5	128
321	SO[20]	10297.5	268
322	SO[21]	10280.5	408
323	SO[22]	10263.5	128
324	SO[23]	10246.5	268
325	SO[24]	10229.5	408
326	SO[25]	10212.5	128
327	SO[26]	10195.5	268
328	SO[27]	10178.5	408
329	SO[28]	10161.5	128
330	SO[29]	10144.5	268
331	SO[30]	10127.5	408
332	SO[31]	10110.5	128
333	SO[32]	10093.5	268
334	SO[33]	10076.5	408
335	SO[34]	10059.5	128
336	SO[35]	10042.5	268
337	SO[36]	10025.5	408
338	SO[37]	10008.5	128
339	SO[38]	9991.5	268
340	SO[39]	9974.5	408
341	SO[40]	9957.5	128
342	SO[41]	9940.5	268
343	SO[42]	9923.5	408
344	SO[43]	9906.5	128
345	SO[44]	9889.5	268
346	SO[45]	9872.5	408
347	SO[46]	9855.5	128
348	SO[47]	9838.5	268
349	SO[48]	9821.5	408
350	SO[49]	9804.5	128
351	SO[50]	9787.5	268
352	SO[51]	9770.5	408
353	SO[52]	9753.5	128
354	SO[53]	9736.5	268
355	SO[54]	9719.5	408
356	SO[55]	9702.5	128
357	SO[56]	9685.5	268
358	SO[57]	9668.5	408
359	SO[58]	9651.5	128
360	SO[59]	9634.5	268

No.	NAME	X	Y
361	SO[60]	9617.5	408
362	SO[61]	9600.5	128
363	SO[62]	9583.5	268
364	SO[63]	9566.5	408
365	SO[64]	9549.5	128
366	SO[65]	9532.5	268
367	SO[66]	9515.5	408
368	SO[67]	9498.5	128
369	SO[68]	9481.5	268
370	SO[69]	9464.5	408
371	SO[70]	9447.5	128
372	SO[71]	9430.5	268
373	SO[72]	9413.5	408
374	SO[73]	9396.5	128
375	SO[74]	9379.5	268
376	SO[75]	9362.5	408
377	SO[76]	9345.5	128
378	SO[77]	9328.5	268
379	SO[78]	9311.5	408
380	SO[79]	9294.5	128
381	SO[80]	9277.5	268
382	SO[81]	9260.5	408
383	SO[82]	9243.5	128
384	SO[83]	9226.5	268
385	SO[84]	9209.5	408
386	SO[85]	9192.5	128
387	SO[86]	9175.5	268
388	SO[87]	9158.5	408
389	SO[88]	9141.5	128
390	SO[89]	9124.5	268
391	SO[90]	9107.5	408
392	SO[91]	9090.5	128
393	SO[92]	9073.5	268
394	SO[93]	9056.5	408
395	SO[94]	9039.5	128
396	SO[95]	9022.5	268
397	SO[96]	9005.5	408
398	SO[97]	8988.5	128
399	SO[98]	8971.5	268
400	SO[99]	8954.5	408
401	SO[100]	8937.5	128
402	SO[101]	8920.5	268
403	SO[102]	8903.5	408
404	SO[103]	8886.5	128
405	SO[104]	8869.5	268
406	SO[105]	8852.5	408
407	SO[106]	8835.5	128
408	SO[107]	8818.5	268
409	SO[108]	8801.5	408
410	SO[109]	8784.5	128
411	SO[110]	8767.5	268
412	SO[111]	8750.5	408
413	SO[112]	8733.5	128
414	SO[113]	8716.5	268
415	SO[114]	8699.5	408
416	SO[115]	8682.5	128
417	SO[116]	8665.5	268
418	SO[117]	8648.5	408
419	SO[118]	8631.5	128
420	SO[119]	8614.5	268

No.	NAME	X	Y
421	SO[120]	8597.5	408
422	SO[121]	8580.5	128
423	SO[122]	8563.5	268
424	SO[123]	8546.5	408
425	SO[124]	8529.5	128
426	SO[125]	8512.5	268
427	SO[126]	8495.5	408
428	SO[127]	8478.5	128
429	SO[128]	8461.5	268
430	SO[129]	8444.5	408
431	SO[130]	8427.5	128
432	SO[131]	8410.5	268
433	SO[132]	8393.5	408
434	SO[133]	8376.5	128
435	SO[134]	8359.5	268
436	SO[135]	8342.5	408
437	SO[136]	8325.5	128
438	SO[137]	8308.5	268
439	SO[138]	8291.5	408
440	SO[139]	8274.5	128
441	SO[140]	8257.5	268
442	SO[141]	8240.5	408
443	SO[142]	8223.5	128
444	SO[143]	8206.5	268
445	SO[144]	8189.5	408
446	SO[145]	8172.5	128
447	SO[146]	8155.5	268
448	SO[147]	8138.5	408
449	SO[148]	8121.5	128
450	SO[149]	8104.5	268
451	SO[150]	8087.5	408
452	SO[151]	8070.5	128
453	SO[152]	8053.5	268
454	SO[153]	8036.5	408
455	SO[154]	8019.5	128
456	SO[155]	8002.5	268
457	SO[156]	7985.5	408
458	SO[157]	7968.5	128
459	SO[158]	7951.5	268
460	SO[159]	7934.5	408
461	SO[160]	7917.5	128
462	SO[161]	7900.5	268
463	SO[162]	7883.5	408
464	SO[163]	7866.5	128
465	SO[164]	7849.5	268
466	SO[165]	7832.5	408
467	SO[166]	7815.5	128
468	SO[167]	7798.5	268
469	SO[168]	7781.5	408
470	SO[169]	7764.5	128
471	SO[170]	7747.5	268
472	SO[171]	7730.5	408
473	SO[172]	7713.5	128
474	SO[173]	7696.5	268
475	SO[174]	7679.5	408
476	SO[175]	7662.5	128
477	SO[176]	7645.5	268
478	SO[177]	7628.5	408
479	SO[178]	7611.5	128
480	SO[179]	7594.5	268

No.	NAME	X	Y
481	SO[180]	7577.5	408
482	SO[181]	7560.5	128
483	SO[182]	7543.5	268
484	SO[183]	7526.5	408
485	SO[184]	7509.5	128
486	SO[185]	7492.5	268
487	SO[186]	7475.5	408
488	SO[187]	7458.5	128
489	SO[188]	7441.5	268
490	SO[189]	7424.5	408
491	SO[190]	7407.5	128
492	SO[191]	7390.5	268
493	SO[192]	7373.5	408
494	SO[193]	7356.5	128
495	SO[194]	7339.5	268
496	SO[195]	7322.5	408
497	SO[196]	7305.5	128
498	SO[197]	7288.5	268
499	SO[198]	7271.5	408
500	SO[199]	7254.5	128
501	SO[200]	7237.5	268
502	SO[201]	7220.5	408
503	SO[202]	7203.5	128
504	SO[203]	7186.5	268
505	SO[204]	7169.5	408
506	SO[205]	7152.5	128
507	SO[206]	7135.5	268
508	SO[207]	7118.5	408
509	SO[208]	7101.5	128
510	SO[209]	7084.5	268
511	SO[210]	7067.5	408
512	SO[211]	7050.5	128
513	SO[212]	7033.5	268
514	SO[213]	7016.5	408
515	SO[214]	6999.5	128
516	SO[215]	6982.5	268
517	SO[216]	6965.5	408
518	SO[217]	6948.5	128
519	SO[218]	6931.5	268
520	SO[219]	6914.5	408
521	SO[220]	6897.5	128
522	SO[221]	6880.5	268
523	SO[222]	6863.5	408
524	SO[223]	6846.5	128
525	SO[224]	6829.5	268
526	SO[225]	6812.5	408
527	SO[226]	6795.5	128
528	SO[227]	6778.5	268
529	SO[228]	6761.5	408
530	SO[229]	6744.5	128
531	SO[230]	6727.5	268
532	SO[231]	6710.5	408
533	SO[232]	6693.5	128
534	SO[233]	6676.5	268
535	SO[234]	6659.5	408
536	SO[235]	6642.5	128
537	SO[236]	6625.5	268
538	SO[237]	6608.5	408
539	SO[238]	6591.5	128
540	SO[239]	6574.5	268

No.	NAME	X	Y
541	SO[240]	6557.5	408
542	SO[241]	6540.5	128
543	SO[242]	6523.5	268
544	SO[243]	6506.5	408
545	SO[244]	6489.5	128
546	SO[245]	6472.5	268
547	SO[246]	6455.5	408
548	SO[247]	6438.5	128
549	SO[248]	6421.5	268
550	SO[249]	6404.5	408
551	SO[250]	6387.5	128
552	SO[251]	6370.5	268
553	SO[252]	6353.5	408
554	SO[253]	6336.5	128
555	SO[254]	6319.5	268
556	SO[255]	6302.5	408
557	SO[256]	6285.5	128
558	SO[257]	6268.5	268
559	SO[258]	6251.5	408
560	SO[259]	6234.5	128
561	SO[260]	6217.5	268
562	SO[261]	6200.5	408
563	SO[262]	6183.5	128
564	SO[263]	6166.5	268
565	SO[264]	6149.5	408
566	SO[265]	6132.5	128
567	SO[266]	6115.5	268
568	SO[267]	6098.5	408
569	SO[268]	6081.5	128
570	SO[269]	6064.5	268
571	SO[270]	6047.5	408
572	SO[271]	6030.5	128
573	SO[272]	6013.5	268
574	SO[273]	5996.5	408
575	SO[274]	5979.5	128
576	SO[275]	5962.5	268
577	SO[276]	5945.5	408
578	SO[277]	5928.5	128
579	SO[278]	5911.5	268
580	SO[279]	5894.5	408
581	SO[280]	5877.5	128
582	SO[281]	5860.5	268
583	SO[282]	5843.5	408
584	SO[283]	5826.5	128
585	SO[284]	5809.5	268
586	SO[285]	5792.5	408
587	SO[286]	5775.5	128
588	SO[287]	5758.5	268
589	SO[288]	5741.5	408
590	SO[289]	5724.5	128
591	SO[290]	5707.5	268
592	SO[291]	5690.5	408
593	SO[292]	5673.5	128
594	SO[293]	5656.5	268
595	SO[294]	5639.5	408
596	SO[295]	5622.5	128
597	SO[296]	5605.5	268
598	SO[297]	5588.5	408
599	SO[298]	5571.5	128
600	SO[299]	5554.5	268

No.	NAME	X	Y
601	SO[300]	5537.5	408
602	SO[301]	5520.5	128
603	SO[302]	5503.5	268
604	SO[303]	5486.5	408
605	SO[304]	5469.5	128
606	SO[305]	5452.5	268
607	SO[306]	5435.5	408
608	SO[307]	5418.5	128
609	SO[308]	5401.5	268
610	SO[309]	5384.5	408
611	SO[310]	5367.5	128
612	SO[311]	5350.5	268
613	SO[312]	5333.5	408
614	SO[313]	5316.5	128
615	SO[314]	5299.5	268
616	SO[315]	5282.5	408
617	SO[316]	5265.5	128
618	SO[317]	5248.5	268
619	SO[318]	5231.5	408
620	SO[319]	5214.5	128
621	SO[320]	5197.5	268
622	SO[321]	5180.5	408
623	SO[322]	5163.5	128
624	SO[323]	5146.5	268
625	SO[324]	5129.5	408
626	SO[325]	5112.5	128
627	SO[326]	5095.5	268
628	SO[327]	5078.5	408
629	SO[328]	5061.5	128
630	SO[329]	5044.5	268
631	SO[330]	5027.5	408
632	SO[331]	5010.5	128
633	SO[332]	4993.5	268
634	SO[333]	4976.5	408
635	SO[334]	4959.5	128
636	SO[335]	4942.5	268
637	SO[336]	4925.5	408
638	SO[337]	4908.5	128
639	SO[338]	4891.5	268
640	SO[339]	4874.5	408
641	SO[340]	4857.5	128
642	SO[341]	4840.5	268
643	SO[342]	4823.5	408
644	SO[343]	4806.5	128
645	SO[344]	4789.5	268
646	SO[345]	4772.5	408
647	SO[346]	4755.5	128
648	SO[347]	4738.5	268
649	SO[348]	4721.5	408
650	SO[349]	4704.5	128
651	SO[350]	4687.5	268
652	SO[351]	4670.5	408
653	SO[352]	4653.5	128
654	SO[353]	4636.5	268
655	SO[354]	4619.5	408
656	SO[355]	4602.5	128
657	SO[356]	4585.5	268
658	SO[357]	4568.5	408
659	SO[358]	4551.5	128
660	SO[359]	4534.5	268

No.	NAME	X	Y
661	SO[360]	4517.5	408
662	SO[361]	4500.5	128
663	SO[362]	4483.5	268
664	SO[363]	4466.5	408
665	SO[364]	4449.5	128
666	SO[365]	4432.5	268
667	SO[366]	4415.5	408
668	SO[367]	4398.5	128
669	SO[368]	4381.5	268
670	SO[369]	4364.5	408
671	SO[370]	4347.5	128
672	SO[371]	4330.5	268
673	SO[372]	4313.5	408
674	SO[373]	4296.5	128
675	SO[374]	4279.5	268
676	SO[375]	4262.5	408
677	SO[376]	4245.5	128
678	SO[377]	4228.5	268
679	SO[378]	4211.5	408
680	SO[379]	4194.5	128
681	SO[380]	4177.5	268
682	SO[381]	4160.5	408
683	SO[382]	4143.5	128
684	SO[383]	4126.5	268
685	SO[384]	4109.5	408
686	SO[385]	4092.5	128
687	SO[386]	4075.5	268
688	SO[387]	4058.5	408
689	SO[388]	4041.5	128
690	SO[389]	4024.5	268
691	SO[390]	4007.5	408
692	SO[391]	3990.5	128
693	SO[392]	3973.5	268
694	SO[393]	3956.5	408
695	SO[394]	3939.5	128
696	SO[395]	3922.5	268
697	SO[396]	3905.5	408
698	SO[397]	3888.5	128
699	SO[398]	3871.5	268
700	SO[399]	3854.5	408
701	SO[400]	3837.5	128
702	SO[401]	3820.5	268
703	SO[402]	3803.5	408
704	SO[403]	3786.5	128
705	SO[404]	3769.5	268
706	SO[405]	3752.5	408
707	SO[406]	3735.5	128
708	SO[407]	3718.5	268
709	SO[408]	3701.5	408
710	SO[409]	3684.5	128
711	SO[410]	3667.5	268
712	SO[411]	3650.5	408
713	SO[412]	3633.5	128
714	SO[413]	3616.5	268
715	SO[414]	3599.5	408
716	SO[415]	3582.5	128
717	SO[416]	3565.5	268
718	SO[417]	3548.5	408
719	SO[418]	3531.5	128
720	SO[419]	3514.5	268

No.	NAME	X	Y
721	SO[420]	3497.5	408
722	SO[421]	3480.5	128
723	SO[422]	3463.5	268
724	SO[423]	3446.5	408
725	SO[424]	3429.5	128
726	SO[425]	3412.5	268
727	SO[426]	3395.5	408
728	SO[427]	3378.5	128
729	SO[428]	3361.5	268
730	SO[429]	3344.5	408
731	SO[430]	3327.5	128
732	SO[431]	3310.5	268
733	SO[432]	3293.5	408
734	SO[433]	3276.5	128
735	SO[434]	3259.5	268
736	SO[435]	3242.5	408
737	SO[436]	3225.5	128
738	SO[437]	3208.5	268
739	SO[438]	3191.5	408
740	SO[439]	3174.5	128
741	SO[440]	3157.5	268
742	SO[441]	3140.5	408
743	SO[442]	3123.5	128
744	SO[443]	3106.5	268
745	SO[444]	3089.5	408
746	SO[445]	3072.5	128
747	SO[446]	3055.5	268
748	SO[447]	3038.5	408
749	SO[448]	3021.5	128
750	SO[449]	3004.5	268
751	SO[450]	2987.5	408
752	SO[451]	2970.5	128
753	SO[452]	2953.5	268
754	SO[453]	2936.5	408
755	SO[454]	2919.5	128
756	SO[455]	2902.5	268
757	SO[456]	2885.5	408
758	SO[457]	2868.5	128
759	SO[458]	2851.5	268
760	SO[459]	2834.5	408
761	SO[460]	2817.5	128
762	SO[461]	2800.5	268
763	SO[462]	2783.5	408
764	SO[463]	2766.5	128
765	SO[464]	2749.5	268
766	SO[465]	2732.5	408
767	SO[466]	2715.5	128
768	SO[467]	2698.5	268
769	SO[468]	2681.5	408
770	SO[469]	2664.5	128
771	SO[470]	2647.5	268
772	SO[471]	2630.5	408
773	SO[472]	2613.5	128
774	SO[473]	2596.5	268
775	SO[474]	2579.5	408
776	SO[475]	2562.5	128
777	SO[476]	2545.5	268
778	SO[477]	2528.5	408
779	SO[478]	2511.5	128
780	SO[479]	2494.5	268

No.	NAME	X	Y
781	SO[480]	2477.5	408
782	SO[481]	2460.5	128
783	SO[482]	2443.5	268
784	SO[483]	2426.5	408
785	SO[484]	2409.5	128
786	SO[485]	2392.5	268
787	SO[486]	2375.5	408
788	SO[487]	2358.5	128
789	SO[488]	2341.5	268
790	SO[489]	2324.5	408
791	SO[490]	2307.5	128
792	SO[491]	2290.5	268
793	SO[492]	2273.5	408
794	SO[493]	2256.5	128
795	SO[494]	2239.5	268
796	SO[495]	2222.5	408
797	SO[496]	2205.5	128
798	SO[497]	2188.5	268
799	SO[498]	2171.5	408
800	SO[499]	2154.5	128
801	SO[500]	2137.5	268
802	SO[501]	2120.5	408
803	SO[502]	2103.5	128
804	SO[503]	2086.5	268
805	SO[504]	2069.5	408
806	SO[505]	2052.5	128
807	SO[506]	2035.5	268
808	SO[507]	2018.5	408
809	SO[508]	2001.5	128
810	SO[509]	1984.5	268
811	SO[510]	1967.5	408
812	SO[511]	1950.5	128
813	SO[512]	1933.5	268
814	SO[513]	1916.5	408
815	SO[514]	1899.5	128
816	SO[515]	1882.5	268
817	SO[516]	1865.5	408
818	SO[517]	1848.5	128
819	SO[518]	1831.5	268
820	SO[519]	1814.5	408
821	SO[520]	1797.5	128
822	SO[521]	1780.5	268
823	SO[522]	1763.5	408
824	SO[523]	1746.5	128
825	SO[524]	1729.5	268
826	SO[525]	1712.5	408
827	SO[526]	1695.5	128
828	SO[527]	1678.5	268
829	SO[528]	1661.5	408
830	SO[529]	1644.5	128
831	SO[530]	1627.5	268
832	SO[531]	1610.5	408
833	SO[532]	1593.5	128
834	SO[533]	1576.5	268
835	SO[534]	1559.5	408
836	SO[535]	1542.5	128
837	SO[536]	1525.5	268
838	SO[537]	1508.5	408
839	SO[538]	1491.5	128
840	SO[539]	1474.5	268

No.	NAME	X	Y
841	SO[540]	1457.5	408
842	SO[541]	1440.5	128
843	SO[542]	1423.5	268
844	SO[543]	1406.5	408
845	SO[544]	1389.5	128
846	SO[545]	1372.5	268
847	SO[546]	1355.5	408
848	SO[547]	1338.5	128
849	SO[548]	1321.5	268
850	SO[549]	1304.5	408
851	SO[550]	1287.5	128
852	SO[551]	1270.5	268
853	SO[552]	1253.5	408
854	SO[553]	1236.5	128
855	SO[554]	1219.5	268
856	SO[555]	1202.5	408
857	SO[556]	1185.5	128
858	SO[557]	1168.5	268
859	SO[558]	1151.5	408
860	SO[559]	1134.5	128
861	SO[560]	1117.5	268
862	SO[561]	1100.5	408
863	SO[562]	1083.5	128
864	SO[563]	1066.5	268
865	SO[564]	1049.5	408
866	SO[565]	1032.5	128
867	SO[566]	1015.5	268
868	SO[567]	998.5	408
869	SO[568]	981.5	128
870	SO[569]	964.5	268
871	SO[570]	947.5	408
872	SO[571]	930.5	128
873	SO[572]	913.5	268
874	SO[573]	896.5	408
875	SO[574]	879.5	128
876	SO[575]	862.5	268
877	SO[576]	845.5	408
878	SO[577]	828.5	128
879	SO[578]	811.5	268
880	SO[579]	794.5	408
881	SO[580]	777.5	128
882	SO[581]	760.5	268
883	SO[582]	743.5	408
884	SO[583]	726.5	128
885	SO[584]	709.5	268
886	SO[585]	692.5	408
887	SO[586]	675.5	128
888	SO[587]	658.5	268
889	SO[588]	641.5	408
890	SO[589]	624.5	128
891	SO[590]	607.5	268
892	SO[591]	590.5	408
893	SO[592]	573.5	128
894	SO[593]	556.5	268
895	SO[594]	539.5	408
896	SO[595]	522.5	128
897	SO[596]	505.5	268
898	SO[597]	488.5	408
899	SO[598]	471.5	128
900	SO[599]	454.5	268

No.	NAME	X	Y
901	SO[600]	437.5	408
902	DUMMY	403.5	408
903	DUMMY	369.5	408
904	DUMMY	335.5	408
905	DUMMY	301.5	408
906	DUMMY	267.5	408
907	DUMMY	233.5	408
908	DUMMY	-233.5	408
909	DUMMY	-267.5	408
910	DUMMY	-301.5	408
911	DUMMY	-335.5	408
912	DUMMY	-369.5	408
913	DUMMY	-403.5	408
914	SO[601]	-437.5	408
915	SO[602]	-454.5	268
916	SO[603]	-471.5	128
917	SO[604]	-488.5	408
918	SO[605]	-505.5	268
919	SO[606]	-522.5	128
920	SO[607]	-539.5	408
921	SO[608]	-556.5	268
922	SO[609]	-573.5	128
923	SO[610]	-590.5	408
924	SO[611]	-607.5	268
925	SO[612]	-624.5	128
926	SO[613]	-641.5	408
927	SO[614]	-658.5	268
928	SO[615]	-675.5	128
929	SO[616]	-692.5	408
930	SO[617]	-709.5	268
931	SO[618]	-726.5	128
932	SO[619]	-743.5	408
933	SO[620]	-760.5	268
934	SO[621]	-777.5	128
935	SO[622]	-794.5	408
936	SO[623]	-811.5	268
937	SO[624]	-828.5	128
938	SO[625]	-845.5	408
939	SO[626]	-862.5	268
940	SO[627]	-879.5	128
941	SO[628]	-896.5	408
942	SO[629]	-913.5	268
943	SO[630]	-930.5	128
944	SO[631]	-947.5	408
945	SO[632]	-964.5	268
946	SO[633]	-981.5	128
947	SO[634]	-998.5	408
948	SO[635]	-1015.5	268
949	SO[636]	-1032.5	128
950	SO[637]	-1049.5	408
951	SO[638]	-1066.5	268
952	SO[639]	-1083.5	128
953	SO[640]	-1100.5	408
954	SO[641]	-1117.5	268
955	SO[642]	-1134.5	128
956	SO[643]	-1151.5	408
957	SO[644]	-1168.5	268
958	SO[645]	-1185.5	128
959	SO[646]	-1202.5	408
960	SO[647]	-1219.5	268

No.	NAME	X	Y
961	SO[648]	-1236.5	128
962	SO[649]	-1253.5	408
963	SO[650]	-1270.5	268
964	SO[651]	-1287.5	128
965	SO[652]	-1304.5	408
966	SO[653]	-1321.5	268
967	SO[654]	-1338.5	128
968	SO[655]	-1355.5	408
969	SO[656]	-1372.5	268
970	SO[657]	-1389.5	128
971	SO[658]	-1406.5	408
972	SO[659]	-1423.5	268
973	SO[660]	-1440.5	128
974	SO[661]	-1457.5	408
975	SO[662]	-1474.5	268
976	SO[663]	-1491.5	128
977	SO[664]	-1508.5	408
978	SO[665]	-1525.5	268
979	SO[666]	-1542.5	128
980	SO[667]	-1559.5	408
981	SO[668]	-1576.5	268
982	SO[669]	-1593.5	128
983	SO[670]	-1610.5	408
984	SO[671]	-1627.5	268
985	SO[672]	-1644.5	128
986	SO[673]	-1661.5	408
987	SO[674]	-1678.5	268
988	SO[675]	-1695.5	128
989	SO[676]	-1712.5	408
990	SO[677]	-1729.5	268
991	SO[678]	-1746.5	128
992	SO[679]	-1763.5	408
993	SO[680]	-1780.5	268
994	SO[681]	-1797.5	128
995	SO[682]	-1814.5	408
996	SO[683]	-1831.5	268
997	SO[684]	-1848.5	128
998	SO[685]	-1865.5	408
999	SO[686]	-1882.5	268
1000	SO[687]	-1899.5	128
1001	SO[688]	-1916.5	408
1002	SO[689]	-1933.5	268
1003	SO[690]	-1950.5	128
1004	SO[691]	-1967.5	408
1005	SO[692]	-1984.5	268
1006	SO[693]	-2001.5	128
1007	SO[694]	-2018.5	408
1008	SO[695]	-2035.5	268
1009	SO[696]	-2052.5	128
1010	SO[697]	-2069.5	408
1011	SO[698]	-2086.5	268
1012	SO[699]	-2103.5	128
1013	SO[700]	-2120.5	408
1014	SO[701]	-2137.5	268
1015	SO[702]	-2154.5	128
1016	SO[703]	-2171.5	408
1017	SO[704]	-2188.5	268
1018	SO[705]	-2205.5	128
1019	SO[706]	-2222.5	408
1020	SO[707]	-2239.5	268

No.	NAME	X	Y
1021	SO[708]	-2256.5	128
1022	SO[709]	-2273.5	408
1023	SO[710]	-2290.5	268
1024	SO[711]	-2307.5	128
1025	SO[712]	-2324.5	408
1026	SO[713]	-2341.5	268
1027	SO[714]	-2358.5	128
1028	SO[715]	-2375.5	408
1029	SO[716]	-2392.5	268
1030	SO[717]	-2409.5	128
1031	SO[718]	-2426.5	408
1032	SO[719]	-2443.5	268
1033	SO[720]	-2460.5	128
1034	SO[721]	-2477.5	408
1035	SO[722]	-2494.5	268
1036	SO[723]	-2511.5	128
1037	SO[724]	-2528.5	408
1038	SO[725]	-2545.5	268
1039	SO[726]	-2562.5	128
1040	SO[727]	-2579.5	408
1041	SO[728]	-2596.5	268
1042	SO[729]	-2613.5	128
1043	SO[730]	-2630.5	408
1044	SO[731]	-2647.5	268
1045	SO[732]	-2664.5	128
1046	SO[733]	-2681.5	408
1047	SO[734]	-2698.5	268
1048	SO[735]	-2715.5	128
1049	SO[736]	-2732.5	408
1050	SO[737]	-2749.5	268
1051	SO[738]	-2766.5	128
1052	SO[739]	-2783.5	408
1053	SO[740]	-2800.5	268
1054	SO[741]	-2817.5	128
1055	SO[742]	-2834.5	408
1056	SO[743]	-2851.5	268
1057	SO[744]	-2868.5	128
1058	SO[745]	-2885.5	408
1059	SO[746]	-2902.5	268
1060	SO[747]	-2919.5	128
1061	SO[748]	-2936.5	408
1062	SO[749]	-2953.5	268
1063	SO[750]	-2970.5	128
1064	SO[751]	-2987.5	408
1065	SO[752]	-3004.5	268
1066	SO[753]	-3021.5	128
1067	SO[754]	-3038.5	408
1068	SO[755]	-3055.5	268
1069	SO[756]	-3072.5	128
1070	SO[757]	-3089.5	408
1071	SO[758]	-3106.5	268
1072	SO[759]	-3123.5	128
1073	SO[760]	-3140.5	408
1074	SO[761]	-3157.5	268
1075	SO[762]	-3174.5	128
1076	SO[763]	-3191.5	408
1077	SO[764]	-3208.5	268
1078	SO[765]	-3225.5	128
1079	SO[766]	-3242.5	408
1080	SO[767]	-3259.5	268

No.	NAME	X	Y
1081	SO[768]	-3276.5	128
1082	SO[769]	-3293.5	408
1083	SO[770]	-3310.5	268
1084	SO[771]	-3327.5	128
1085	SO[772]	-3344.5	408
1086	SO[773]	-3361.5	268
1087	SO[774]	-3378.5	128
1088	SO[775]	-3395.5	408
1089	SO[776]	-3412.5	268
1090	SO[777]	-3429.5	128
1091	SO[778]	-3446.5	408
1092	SO[779]	-3463.5	268
1093	SO[780]	-3480.5	128
1094	SO[781]	-3497.5	408
1095	SO[782]	-3514.5	268
1096	SO[783]	-3531.5	128
1097	SO[784]	-3548.5	408
1098	SO[785]	-3565.5	268
1099	SO[786]	-3582.5	128
1100	SO[787]	-3599.5	408
1101	SO[788]	-3616.5	268
1102	SO[789]	-3633.5	128
1103	SO[790]	-3650.5	408
1104	SO[791]	-3667.5	268
1105	SO[792]	-3684.5	128
1106	SO[793]	-3701.5	408
1107	SO[794]	-3718.5	268
1108	SO[795]	-3735.5	128
1109	SO[796]	-3752.5	408
1110	SO[797]	-3769.5	268
1111	SO[798]	-3786.5	128
1112	SO[799]	-3803.5	408
1113	SO[800]	-3820.5	268
1114	SO[801]	-3837.5	128
1115	SO[802]	-3854.5	408
1116	SO[803]	-3871.5	268
1117	SO[804]	-3888.5	128
1118	SO[805]	-3905.5	408
1119	SO[806]	-3922.5	268
1120	SO[807]	-3939.5	128
1121	SO[808]	-3956.5	408
1122	SO[809]	-3973.5	268
1123	SO[810]	-3990.5	128
1124	SO[811]	-4007.5	408
1125	SO[812]	-4024.5	268
1126	SO[813]	-4041.5	128
1127	SO[814]	-4058.5	408
1128	SO[815]	-4075.5	268
1129	SO[816]	-4092.5	128
1130	SO[817]	-4109.5	408
1131	SO[818]	-4126.5	268
1132	SO[819]	-4143.5	128
1133	SO[820]	-4160.5	408
1134	SO[821]	-4177.5	268
1135	SO[822]	-4194.5	128
1136	SO[823]	-4211.5	408
1137	SO[824]	-4228.5	268
1138	SO[825]	-4245.5	128
1139	SO[826]	-4262.5	408
1140	SO[827]	-4279.5	268

No.	NAME	X	Y
1141	SO[828]	-4296.5	128
1142	SO[829]	-4313.5	408
1143	SO[830]	-4330.5	268
1144	SO[831]	-4347.5	128
1145	SO[832]	-4364.5	408
1146	SO[833]	-4381.5	268
1147	SO[834]	-4398.5	128
1148	SO[835]	-4415.5	408
1149	SO[836]	-4432.5	268
1150	SO[837]	-4449.5	128
1151	SO[838]	-4466.5	408
1152	SO[839]	-4483.5	268
1153	SO[840]	-4500.5	128
1154	SO[841]	-4517.5	408
1155	SO[842]	-4534.5	268
1156	SO[843]	-4551.5	128
1157	SO[844]	-4568.5	408
1158	SO[845]	-4585.5	268
1159	SO[846]	-4602.5	128
1160	SO[847]	-4619.5	408
1161	SO[848]	-4636.5	268
1162	SO[849]	-4653.5	128
1163	SO[850]	-4670.5	408
1164	SO[851]	-4687.5	268
1165	SO[852]	-4704.5	128
1166	SO[853]	-4721.5	408
1167	SO[854]	-4738.5	268
1168	SO[855]	-4755.5	128
1169	SO[856]	-4772.5	408
1170	SO[857]	-4789.5	268
1171	SO[858]	-4806.5	128
1172	SO[859]	-4823.5	408
1173	SO[860]	-4840.5	268
1174	SO[861]	-4857.5	128
1175	SO[862]	-4874.5	408
1176	SO[863]	-4891.5	268
1177	SO[864]	-4908.5	128
1178	SO[865]	-4925.5	408
1179	SO[866]	-4942.5	268
1180	SO[867]	-4959.5	128
1181	SO[868]	-4976.5	408
1182	SO[869]	-4993.5	268
1183	SO[870]	-5010.5	128
1184	SO[871]	-5027.5	408
1185	SO[872]	-5044.5	268
1186	SO[873]	-5061.5	128
1187	SO[874]	-5078.5	408
1188	SO[875]	-5095.5	268
1189	SO[876]	-5112.5	128
1190	SO[877]	-5129.5	408
1191	SO[878]	-5146.5	268
1192	SO[879]	-5163.5	128
1193	SO[880]	-5180.5	408
1194	SO[881]	-5197.5	268
1195	SO[882]	-5214.5	128
1196	SO[883]	-5231.5	408
1197	SO[884]	-5248.5	268
1198	SO[885]	-5265.5	128
1199	SO[886]	-5282.5	408
1200	SO[887]	-5299.5	268

No.	NAME	X	Y
1201	SO[888]	-5316.5	128
1202	SO[889]	-5333.5	408
1203	SO[890]	-5350.5	268
1204	SO[891]	-5367.5	128
1205	SO[892]	-5384.5	408
1206	SO[893]	-5401.5	268
1207	SO[894]	-5418.5	128
1208	SO[895]	-5435.5	408
1209	SO[896]	-5452.5	268
1210	SO[897]	-5469.5	128
1211	SO[898]	-5486.5	408
1212	SO[899]	-5503.5	268
1213	SO[900]	-5520.5	128
1214	SO[901]	-5537.5	408
1215	SO[902]	-5554.5	268
1216	SO[903]	-5571.5	128
1217	SO[904]	-5588.5	408
1218	SO[905]	-5605.5	268
1219	SO[906]	-5622.5	128
1220	SO[907]	-5639.5	408
1221	SO[908]	-5656.5	268
1222	SO[909]	-5673.5	128
1223	SO[910]	-5690.5	408
1224	SO[911]	-5707.5	268
1225	SO[912]	-5724.5	128
1226	SO[913]	-5741.5	408
1227	SO[914]	-5758.5	268
1228	SO[915]	-5775.5	128
1229	SO[916]	-5792.5	408
1230	SO[917]	-5809.5	268
1231	SO[918]	-5826.5	128
1232	SO[919]	-5843.5	408
1233	SO[920]	-5860.5	268
1234	SO[921]	-5877.5	128
1235	SO[922]	-5894.5	408
1236	SO[923]	-5911.5	268
1237	SO[924]	-5928.5	128
1238	SO[925]	-5945.5	408
1239	SO[926]	-5962.5	268
1240	SO[927]	-5979.5	128
1241	SO[928]	-5996.5	408
1242	SO[929]	-6013.5	268
1243	SO[930]	-6030.5	128
1244	SO[931]	-6047.5	408
1245	SO[932]	-6064.5	268
1246	SO[933]	-6081.5	128
1247	SO[934]	-6098.5	408
1248	SO[935]	-6115.5	268
1249	SO[936]	-6132.5	128
1250	SO[937]	-6149.5	408
1251	SO[938]	-6166.5	268
1252	SO[939]	-6183.5	128
1253	SO[940]	-6200.5	408
1254	SO[941]	-6217.5	268
1255	SO[942]	-6234.5	128
1256	SO[943]	-6251.5	408
1257	SO[944]	-6268.5	268
1258	SO[945]	-6285.5	128
1259	SO[946]	-6302.5	408
1260	SO[947]	-6319.5	268
1261	SO[948]	-6336.5	128
1262	SO[949]	-6353.5	408
1263	SO[950]	-6370.5	268
1264	SO[951]	-6387.5	128
1265	SO[952]	-6404.5	408
1266	SO[953]	-6421.5	268
1267	SO[954]	-6438.5	128
1268	SO[955]	-6455.5	408
1269	SO[956]	-6472.5	268
1270	SO[957]	-6489.5	128
1271	SO[958]	-6506.5	408
1272	SO[959]	-6523.5	268
1273	SO[960]	-6540.5	128
1274	SO[961]	-6557.5	408
1275	SO[962]	-6574.5	268
1276	SO[963]	-6591.5	128
1277	SO[964]	-6608.5	408
1278	SO[965]	-6625.5	268
1279	SO[966]	-6642.5	128
1280	SO[967]	-6659.5	408
1281	SO[968]	-6676.5	268
1282	SO[969]	-6693.5	128
1283	SO[970]	-6710.5	408
1284	SO[971]	-6727.5	268
1285	SO[972]	-6744.5	128
1286	SO[973]	-6761.5	408
1287	SO[974]	-6778.5	268
1288	SO[975]	-6795.5	128
1289	SO[976]	-6812.5	408
1290	SO[977]	-6829.5	268
1291	SO[978]	-6846.5	128
1292	SO[979]	-6863.5	408
1293	SO[980]	-6880.5	268
1294	SO[981]	-6897.5	128
1295	SO[982]	-6914.5	408
1296	SO[983]	-6931.5	268
1297	SO[984]	-6948.5	128
1298	SO[985]	-6965.5	408
1299	SO[986]	-6982.5	268
1300	SO[987]	-6999.5	128
1301	SO[988]	-7016.5	408
1302	SO[989]	-7033.5	268
1303	SO[990]	-7050.5	128
1304	SO[991]	-7067.5	408
1305	SO[992]	-7084.5	268
1306	SO[993]	-7101.5	128
1307	SO[994]	-7118.5	408
1308	SO[995]	-7135.5	268
1309	SO[996]	-7152.5	128
1310	SO[997]	-7169.5	408
1311	SO[998]	-7186.5	268
1312	SO[999]	-7203.5	128
1313	SO[1000]	-7220.5	408
1314	SO[1001]	-7237.5	268
1315	SO[1002]	-7254.5	128
1316	SO[1003]	-7271.5	408
1317	SO[1004]	-7288.5	268
1318	SO[1005]	-7305.5	128
1319	SO[1006]	-7322.5	408
1320	SO[1007]	-7339.5	268
1321	SO[1008]	-7356.5	128
1322	SO[1009]	-7373.5	408
1323	SO[1010]	-7390.5	268
1324	SO[1011]	-7407.5	128
1325	SO[1012]	-7424.5	408
1326	SO[1013]	-7441.5	268
1327	SO[1014]	-7458.5	128
1328	SO[1015]	-7475.5	408
1329	SO[1016]	-7492.5	268
1330	SO[1017]	-7509.5	128
1331	SO[1018]	-7526.5	408
1332	SO[1019]	-7543.5	268
1333	SO[1020]	-7560.5	128
1334	SO[1021]	-7577.5	408
1335	SO[1022]	-7594.5	268
1336	SO[1023]	-7611.5	128
1337	SO[1024]	-7628.5	408
1338	SO[1025]	-7645.5	268
1339	SO[1026]	-7662.5	128
1340	SO[1027]	-7679.5	408
1341	SO[1028]	-7696.5	268
1342	SO[1029]	-7713.5	128
1343	SO[1030]	-7730.5	408
1344	SO[1031]	-7747.5	268
1345	SO[1032]	-7764.5	128
1346	SO[1033]	-7781.5	408
1347	SO[1034]	-7798.5	268
1348	SO[1035]	-7815.5	128
1349	SO[1036]	-7832.5	408
1350	SO[1037]	-7849.5	268
1351	SO[1038]	-7866.5	128
1352	SO[1039]	-7883.5	408
1353	SO[1040]	-7900.5	268
1354	SO[1041]	-7917.5	128
1355	SO[1042]	-7934.5	408
1356	SO[1043]	-7951.5	268
1357	SO[1044]	-7968.5	128
1358	SO[1045]	-7985.5	408
1359	SO[1046]	-8002.5	268
1360	SO[1047]	-8019.5	128
1361	SO[1048]	-8036.5	408
1362	SO[1049]	-8053.5	268
1363	SO[1050]	-8070.5	128
1364	SO[1051]	-8087.5	408
1365	SO[1052]	-8104.5	268
1366	SO[1053]	-8121.5	128
1367	SO[1054]	-8138.5	408
1368	SO[1055]	-8155.5	268
1369	SO[1056]	-8172.5	128
1370	SO[1057]	-8189.5	408
1371	SO[1058]	-8206.5	268
1372	SO[1059]	-8223.5	128
1373	SO[1060]	-8240.5	408
1374	SO[1061]	-8257.5	268
1375	SO[1062]	-8274.5	128
1376	SO[1063]	-8291.5	408
1377	SO[1064]	-8308.5	268
1378	SO[1065]	-8325.5	128
1379	SO[1066]	-8342.5	408
1380	SO[1067]	-8359.5	268
1381	SO[1068]	-8376.5	128
1382	SO[1069]	-8393.5	408
1383	SO[1070]	-8410.5	268
1384	SO[1071]	-8427.5	128
1385	SO[1072]	-8444.5	408
1386	SO[1073]	-8461.5	268
1387	SO[1074]	-8478.5	128
1388	SO[1075]	-8495.5	408
1389	SO[1076]	-8512.5	268
1390	SO[1077]	-8529.5	128
1391	SO[1078]	-8546.5	408
1392	SO[1079]	-8563.5	268
1393	SO[1080]	-8580.5	128
1394	SO[1081]	-8597.5	408
1395	SO[1082]	-8614.5	268
1396	SO[1083]	-8631.5	128
1397	SO[1084]	-8648.5	408
1398	SO[1085]	-8665.5	268
1399	SO[1086]	-8682.5	128
1400	SO[1087]	-8699.5	408
1401	SO[1088]	-8716.5	268
1402	SO[1089]	-8733.5	128
1403	SO[1090]	-8750.5	408
1404	SO[1091]	-8767.5	268
1405	SO[1092]	-8784.5	128
1406	SO[1093]	-8801.5	408
1407	SO[1094]	-8818.5	268
1408	SO[1095]	-8835.5	128
1409	SO[1096]	-8852.5	408
1410	SO[1097]	-8869.5	268
1411	SO[1098]	-8886.5	128
1412	SO[1099]	-8903.5	408
1413	SO[1100]	-8920.5	268
1414	SO[1101]	-8937.5	128
1415	SO[1102]	-8954.5	408
1416	SO[1103]	-8971.5	268
1417	SO[1104]	-8988.5	128
1418	SO[1105]	-9005.5	408
1419	SO[1106]	-9022.5	268
1420	SO[1107]	-9039.5	128
1421	SO[1108]	-9056.5	408
1422	SO[1109]	-9073.5	268
1423	SO[1110]	-9090.5	128
1424	SO[1111]	-9107.5	408
1425	SO[1112]	-9124.5	268
1426	SO[1113]	-9141.5	128
1427	SO[1114]	-9158.5	408
1428	SO[1115]	-9175.5	268
1429	SO[1116]	-9192.5	128
1430	SO[1117]	-9209.5	408
1431	SO[1118]	-9226.5	268
1432	SO[1119]	-9243.5	128
1433	SO[1120]	-9260.5	408
1434	SO[1121]	-9277.5	268
1435	SO[1122]	-9294.5	128
1436	SO[1123]	-9311.5	408
1437	SO[1124]	-9328.5	268
1438	SO[1125]	-9345.5	128
1439	SO[1126]	-9362.5	408
1440	SO[1127]	-9379.5	268

No.	NAME	X	Y
1444	SO[1131]	-9447.5	128
1445	SO[1132]	-9464.5	408
1446	SO[1133]	-9481.5	268
1447	SO[1134]	-9498.5	128
1448	SO[1135]	-9515.5	408
1449	SO[1136]	-9532.5	268
1450	SO[1137]	-9549.5	128
1451	SO[1138]	-9566.5	408
1452	SO[1139]	-9583.5	268
1453	SO[1140]	-9600.5	128
1454	SO[1141]	-9617.5	408
1455	SO[1142]	-9634.5	268
1456	SO[1143]	-9651.5	128
1457	SO[1144]	-9668.5	408
1458	SO[1145]	-9685.5	268
1459	SO[1146]	-9702.5	128
1460	SO[1147]	-9719.5	408
1461	SO[1148]	-9736.5	268
1462	SO[1149]	-9753.5	128
1463	SO[1150]	-9770.5	408
1464	SO[1151]	-9787.5	268
1465	SO[1152]	-9804.5	128
1466	SO[1153]	-9821.5	408
1467	SO[1154]	-9838.5	268
1468	SO[1155]	-9855.5	128
1469	SO[1156]	-9872.5	408
1470	SO[1157]	-9889.5	268
1471	SO[1158]	-9906.5	128
1472	SO[1159]	-9923.5	408
1473	SO[1160]	-9940.5	268
1474	SO[1161]	-9957.5	128
1475	SO[1162]	-9974.5	408
1476	SO[1163]	-9991.5	268
1477	SO[1164]	-10008.5	128
1478	SO[1165]	-10025.5	408
1479	SO[1166]	-10042.5	268
1480	SO[1167]	-10059.5	128
1481	SO[1168]	-10076.5	408
1482	SO[1169]	-10093.5	268
1483	SO[1170]	-10110.5	128
1484	SO[1171]	-10127.5	408
1485	SO[1172]	-10144.5	268
1486	SO[1173]	-10161.5	128
1487	SO[1174]	-10178.5	408
1488	SO[1175]	-10195.5	268
1489	SO[1176]	-10212.5	128
1490	SO[1177]	-10229.5	408
1491	SO[1178]	-10246.5	268
1492	SO[1179]	-10263.5	128
1493	SO[1180]	-10280.5	408
1494	SO[1181]	-10297.5	268
1495	SO[1182]	-10314.5	128
1496	SO[1183]	-10331.5	408
1497	SO[1184]	-10348.5	268
1498	SO[1185]	-10365.5	128
1499	SO[1186]	-10382.5	408
1500	SO[1187]	-10399.5	268

No.	NAME	X	Y
1504	SO[1191]	-10467.5	128
1505	SO[1192]	-10484.5	408
1506	SO[1193]	-10501.5	268
1507	SO[1194]	-10518.5	128
1508	SO[1195]	-10535.5	408
1509	SO[1196]	-10552.5	268
1510	SO[1197]	-10569.5	128
1511	SO[1198]	-10586.5	408
1512	SO[1199]	-10603.5	268
1513	SO[1200]	-10620.5	128
1514	SHIELDING	-10664	428
1515	COM1_T	-10714	428
1516	COM1_T	-10764	428
1517	SHIELDING	-10814	428
1518	DCMPR	-10864	428
1519	DCMPR	-10914	428
1520	OEVR	-11049	328
1521	INVBRR	-11049	408

Application Circuit Diagram

1. Dual Gate Mode

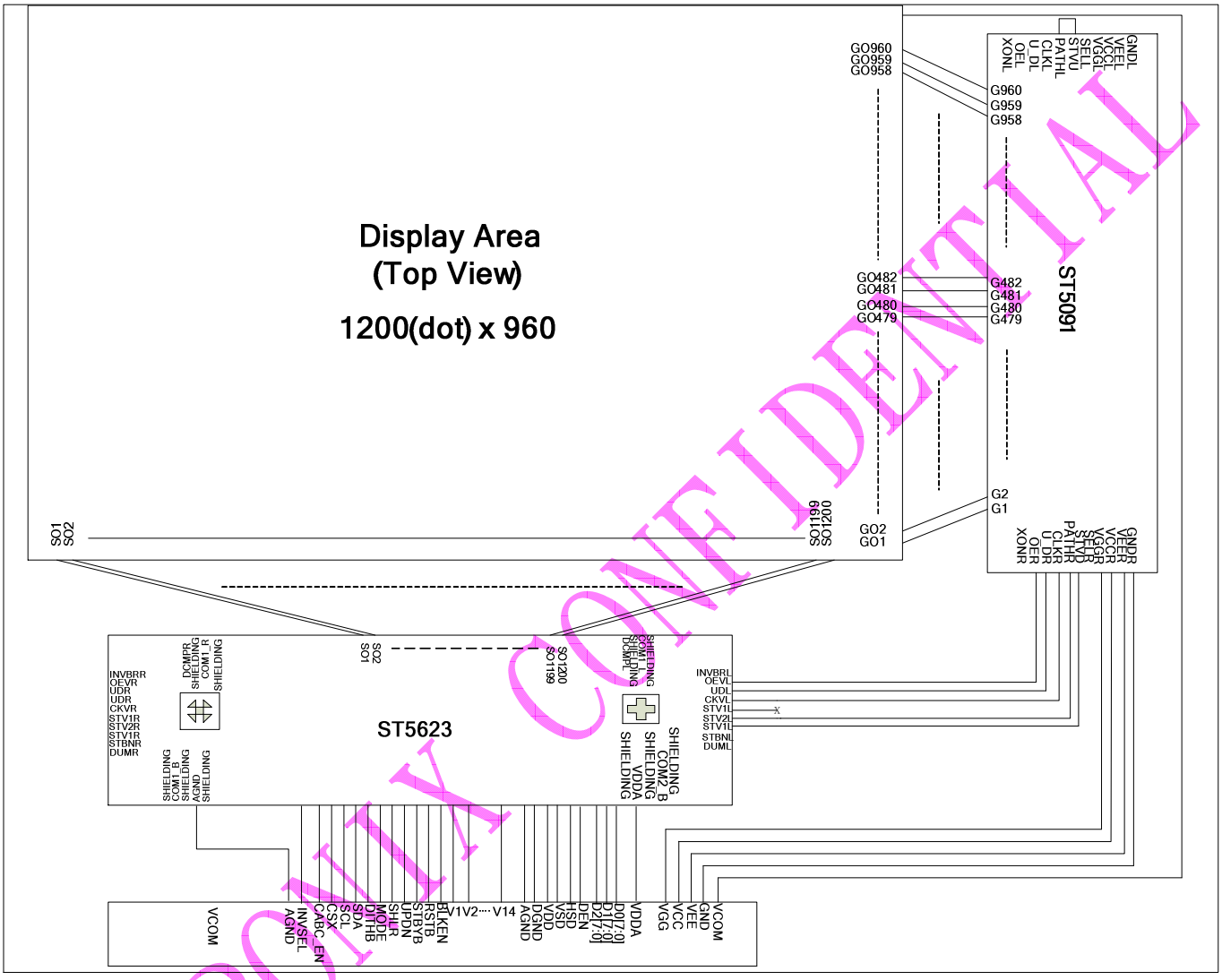
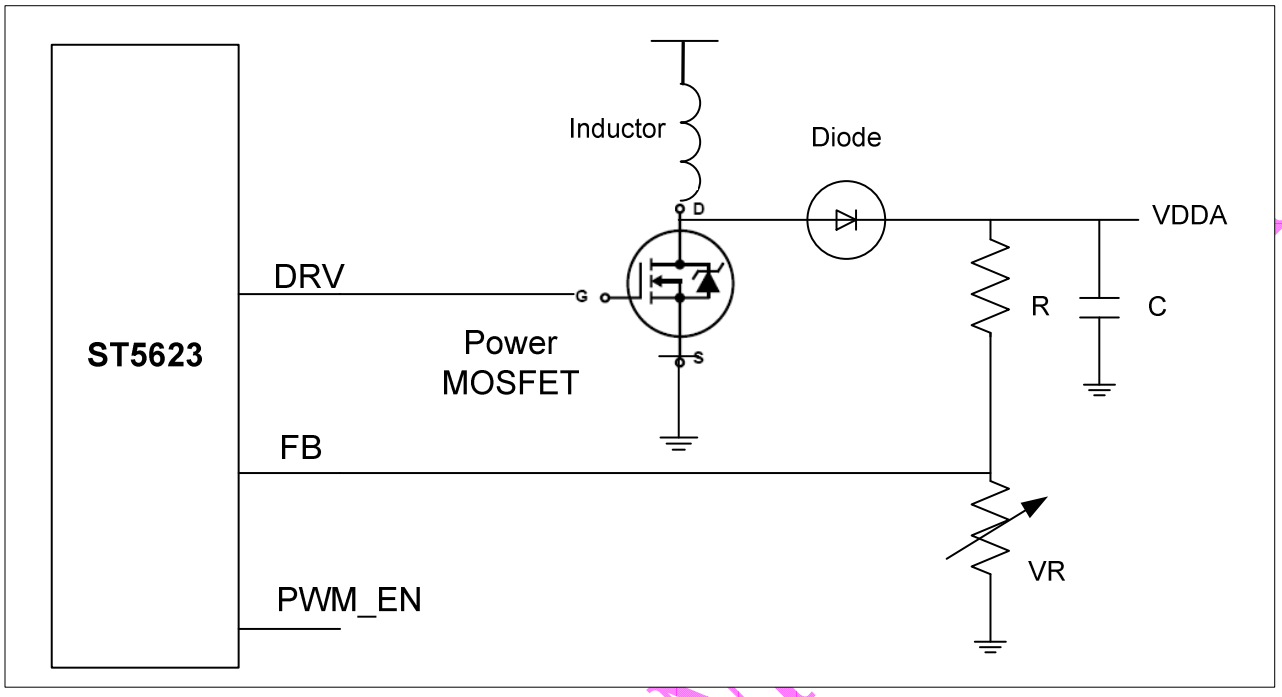
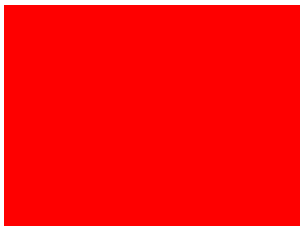
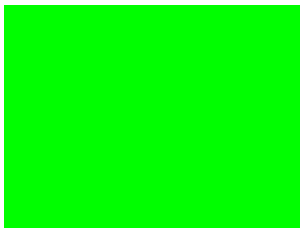
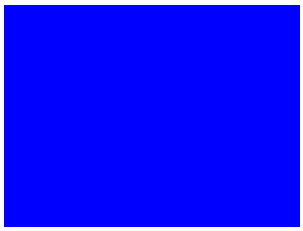
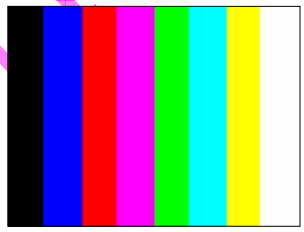


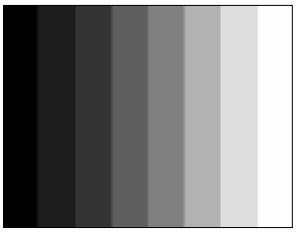
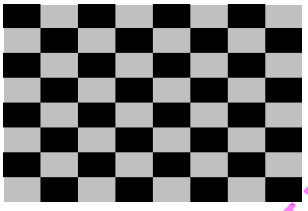
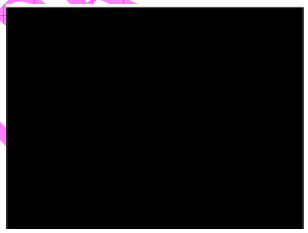
Figure 2 ST5623 used for Dual Gate Mode

2.PWM Booster



BIST Pattern

No.	Pattern	Test Function Description	Notice
1		Color R alignment with color filter.	
2		Color G alignment with color filter.	
3		Color B alignment with color filter.	
4		Black Pattern.	
5		White Pattern.	
6		1. Customer standard test pattern. 2. Color alignment with color filter. 3. Driver scan direction.	

7		Customer standard test pattern.	
8		Customer standard test pattern.	
9		Crosstalk Pattern (Vertical cross talk: Belong to Panel issue, Horizontal cross talk: Inversion structure issue(Line inversion)).	
10		Chessboard Pattern.	
11		Black-Gray(128) Flicker Pattern	
12		Black background and White frame	

Ordering information

Part.No	Package
ST5623 – Gx	G : means COG x: means chip thick ness 3 = 400um 4 = 300um

Revision History

Version	Description of Changes	Page	Date
V0.0	First Version Release.		2010/6/3
V0.3	Modify Pin Assignments (Bump View) Modify Pad Coordination 14,15,17,18 ,38,39 and 121~180 Modify Pad Arrangement	4 34 32	2010/6/28
V0.4	1.Modify dual gate structrure for dot polarity 2.Modify gamma table	9 13~15	2010/7/12
V0.5	1.Add RES[1:0]:11=>800*480 resolution 2.Add wiring resistance value from COM1_B(COM2_B) to COM1_T(COM2_T) 3.Add SPI AC timing 4.Modify application circuit for ST5091 5.Modify bist mode pattern 7	4 6 32 42 44	2010/7/20
V0.6	Add PWM booster function	1,2,3,6,33	2010/8/18
V0.7	1.ADD DBC/3, SCL/DBCM[0] ,SDA/DBCM[1] function 2.ADD REV function 3.modify Gamma table,pad Coordination 4.remove BCTRL of Write CTRL Display Value(53h) for CABC 5.ADD 800x480,800x600 dual gate mode for gate driver on left and right side) 6.Modify bist pattern Black background and White frame 7.remove colore enhance function	5,8.11,39 45 18,19 26,27 3~6 49 2	2010/12/27
V0.8	1.When VSET="H", V1~V14 pins are the external adjustment point for Gamma correction. The relationship between V1~V14 must be : AGND<V14<V13<V12<V11<V10<V9<V8<V7<V6<V5<V4<V3<V2<V1<VDDA	9	2011/3/1
V0.9	Add reset application circuit	11	2011/3/10
V1.0	Modify AC voltage 2.7V~3.6V to 3.0V~3.6V	35	
	Modify 640*480 Horizontal input timing	24	2011/4/27
V1.1	Modify Sync mode timing diagram	34	2011/6/2