PRODUCT SPECIFICATION

Product Name	**S76G** **LoRa and GNSS Wireless Communication Module**
Version	**E**
Doc No	**901-10601**
Date	**Nov 5th, 2019**

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Document History

Date	Revised Contents	Revised By	Version
Nov 01th ,2017	Draft Version	Kenny	A
Mar 26th ,2018	Modify GNSS features description and Package Information	Kenny	B
Jun 27th ,2018	Electrical Characteristics and pin definitions update and modify product marking to add 2D barcode	Kenny	C
July 27th ,2018	1. Correct the function description content, 2. Update Block Diagram,	Kenny	D
Nov 5th ,2019	GNSS add BEIDOU, Correct GNSS current consumption	Jack	E

INDEX

1. Feature

Platform Features

- ST micro controller: STM32L073Z
- High performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency
- 192 Kbytes of Flash memory
- 20 Kbytes of SRAM
- Serial wire debug (SWD) & JTAG
- USB 2.0 full-speed device/host

LORA Features

- LORA chip: Semtech SX1276
- LoRa Modem
- +20 dBm constant RF output vs. V supply
- Programmable bit rate up to 37500 bps
- High sensitivity: down to -137 dBm
- Excellent blocking immunity
- Preamble detection
- Automatic RF Sense and CAD with ultra-fast AFC
- Payload up to 128 bytes with CRC

GNSS Features

- GNSS chip: SONY CXD5603GF
- GPS/GLONASS/BEIDOU receiver
- Ultra-low power consumption
- Supports SBAS/QZSS

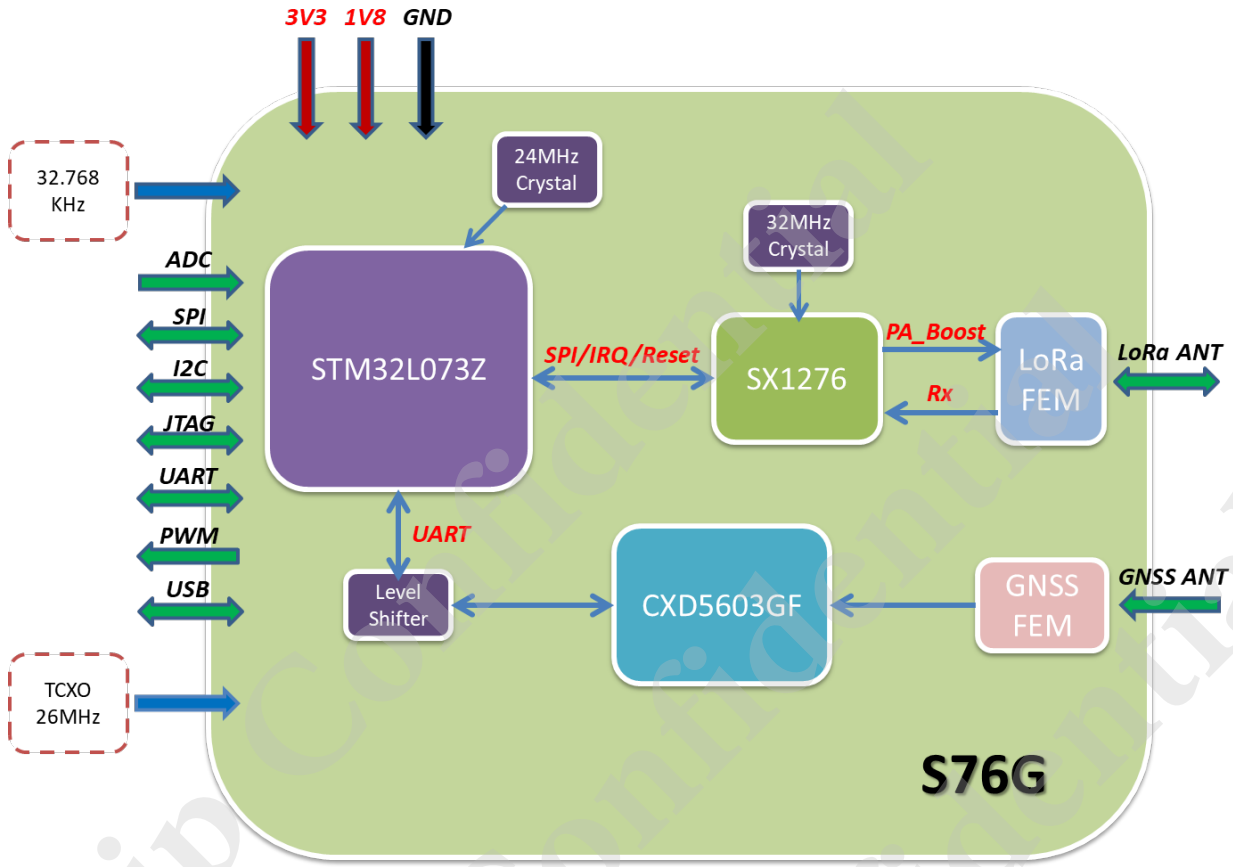
Other Features

- Periphery components inside S76G:
  1. 24MHz crystal for STM32L073Z and 32MHz TCXO for SX1276
  2. 16Mbits Flash for CXD5603GF
  3. Level shifter for communication between STM32L073Z and CXD5603GF
  4. LoRa FEM/matching circuit and GNSS FEM/matching circuit
- Additional components needed for S76G operation:
  1. 32.768KHz crystal for STM32L073Z
  2. 26MHz TCXO for CXD5603GF
  3. Please see section 2-4 and 2-5 for more details
- Epoxy molding finished module in LGA type
- Small size : 13mm X 11mm X 1.55 mm

RoHS & Halogen free compliant / Lead free

1-1. Block Diagram

A simplified block diagram of the S76G module is depicted in the figure below.



1-2. Product Version

The features of S76G is detailed in the following table

Part Number	Frequency Range	Spreading Factor	Bandwidth (K Hz)	Effective Bitrate (bps)	Est. Sensitivity (dBm)
S76G	902-928 MHz 863-870 MHz**	6 - 12	62.5 - 500	146 - 37500	-109 to -137*

Note: * LORA setting SF=12, BW=62.5k, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1.

**Optional FW Support for European band 868 MHz

1-3. Specification

Technical Specifications	
Model Name	S76G
Product Description	LoRa and GNSS Wireless Communication Module
Host Interface	UART
Dimension	13 mm x 11 mm x 1.55mm
Package	LGA type
Electrical Specifications	
Frequency	■ LoRa frequency band: EU868 / US915 / AS923 ■ GNSS frequency band: GPS (L1 C/A) / GLONASS (L1OF)/ BEIDOU
Operation Conditions	
Operating Voltage	■ 3.3V for MCU / LoRa function ■ 1.8V for GNSS function
Temperature	■ Storage：-50℃ ~ +105℃ ■ Operating：-25℃ ~ +85℃
Humidity	■ Operating：10 ~ 95% (Non-Condensing) ■ Storage：5 ~ 95% (Non-Condensing)

2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_3V3	Supply Voltage	-0.3		3.9	V
VDD_1V8	Supply Voltage	-0.3		2.2	V
V_{IN}	Input voltage on digital pins	-0.3		3.9	V
Pmr	LoRa RF Input Level			+10	dBm

2-2. Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_3V3	Supply Voltage	2.4	3.3	3.6	V
VDD_1V8	Supply Voltage	1.65	1.8	1.95	V
ML	LoRa RF Input Level			+10	dBm

2-3. Power Consumption Characteristics

2-3.1. 3.3V for LoRa function

Symbol	Parameter	Conditions	Typ.	Max.	Unit
IDDSL	Supply current in Sleep mode	Sleep Stop Mode	4.2	5	uA
IDDST	Supply current in Standby mode	TCXO oscillator enabled	11.2	12.8	mA
IDDR	Supply current in Receive mode		22.5		mA
IDDT	Supply current in Transmit mode with impedance matching	RF SetPW = +20 dBm RF SetPW = +17 dBm RF SetPW = +13 dBm RF SetPW = + 7 dBm	132 112 89 63	134	mA

2-3.2. 1.8V for GNSS function

Symbol	Item	State	Typ.	Unit
GNS_{ACQ}	Satellite acquisition(Hybrid)	S0: Exec	21	mA
GNS_{TRK}	Satellite tracking (Hybrid) 8-ch tracking		14.2	mA
IDLE	Idle	S1: Idle	3.6	mA
SLP_0	Sleep0	S2: Sleep0	0.39	mA
SLP_1	Sleep1	S3: Sleep1	0.15	mA

State	CXD5603GF				
	GNSS	CPU	Always-on block	Backup RAM	Main RAM
S0: Exec	Operation	Operation	Operation	Hold	Hold
S1: Idle	Standby	Operation	Operation	Hold	Hold
S2: Sleep0	Power-off	Power-off	Operation	Hold	Hold
S3: Sleep1	Power-off	Power-off	Operation	Hold	Power-off

State Description

S0: Exec

GNSS positioning can be performed.

S1: Idle

This is a command waiting state. The system can accept commands but power consumption is managed to be low.

S2: Sleep0

The CXD5603GF holds program code, data and satellite date but other logic circuit is powered off. The CXD5603GF can wake up from this state without loading the data from an external FLASH memory or the system MCU.

S3: Sleep1

Because the CXD5603GF holds satellite data only in this state, it must load program data from an external FLASH memory or the system MCU for wake-up but it can get a position with hot start.

2-4. GPS TCXO CLK_IN(in buffer mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}	0.8	-	1.4	Vpp
Input Frequency	F_{IN}	-	26.0	-	MHz
Input frequency characteristics	F_{IN_C}	-0.5	-	0.5	ppm
Duty Cycle	D_C	40	-	60	%

Recommended Parts List

- Nihon Dempa Kogyo Co., Ltd. / NT2016SA
- KYOCERA Crystal Device Corporation / KT2016

2-5. MCU RTC Low-speed external clock

Symbol	Parameter	Conditions*	Min	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal trans conductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$**	Startup time	V_{DD} is stabilized	-	2	-	s

* Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.

**Guaranteed by characterization results. tSU(LSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

2-6. RF Characteristics

2-6.1. RF characteristics for LoRa

The table below gives the electrical specifications for the transceiver operating with LoRa™ modulation.

Following conditions apply unless otherwise specified:

- Supply voltage = 3.3 V.
- Temperature = 25° C.
- Frequency bands: 915 MHz
- Bandwidth (BW) = 125 kHz.
- Spreading Factor (SF) = 12.
- Error Correction Code (EC) = 4/6.
- Packet Error Rate (PER)= 1%
- CRC on payload enabled.
- Payload length = 64 bytes.
- Preamble Length = 12 symbols (programmed register PreambleLength=8)
- With matched impedances

LoRa Transmitter (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band1		915		MHz
Tx Pwr Level @Module O/P	PA_BOOST pin	17.5	18.5	19.5	dBm
LoRa Receiver (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band1	863	915	928	MHz
RF sensitivity, (Long-Range Mode, highest LNA gain, LNA boost, 62.5 kHz bandwidth)	SF = 10		-133		dBm
	SF = 11		-135		dBm
	SF = 12		-137		dBm
RF sensitivity, (Long-Range Mode, highest LNA gain, LNA boost, 125 kHz bandwidth)	SF = 7		-121		dBm
	SF = 8		-124		dBm
	SF = 9		-127		dBm
	SF = 10		-130		dBm
	SF = 11		-131		dBm
	SF = 12		-134		dBm
RF sensitivity, (Long-Range Mode, highest LNA gain, LNA boost, 500 kHz bandwidth)	SF = 7		-114		dBm
	SF = 8		-117		dBm
	SF = 9		-120		dBm
	SF = 10		-123		dBm
	SF = 11		-126		dBm
	SF = 12		-128		dBm

2-6.2. RF characteristics for GNSS receiver

Parameter	Description	Performance	Unit
C/N @-130 dBm		41	dB
Position Accuracy @-130 dBm	2DRMS	2.5	Meter
TTFF @-130 dBm	Cold start	< 35	Sec
	Hot start	< 1	Sec
Sensitivity	Acquisition	-146	dBm
	Tracking	-158	dBm

2-7. Digital Characteristics

2-7.1. DC characteristics

Input voltage levels

Symbol	Description	Conditions	Min	Typ.	Max	Unit
VIH	I/O input high level voltage	NRST	0.7xVDD_3V3	-	-	V
		BOOT0	0.7xVDD_3V3	-	-	V
		GPIO	0.7xVDD_3V3	-	-	V
		GPS_Digital IO	0.65xVDD_1V8	-	VDD_1V8+0.3-	V
VIL	I/O input low level voltage	NRST	-	-	0.3xVDD_3V3	V
		BOOT0	-	-	0.14xVDD_3V3	V
		GPIO	-	-	0.3xVDD_3V3	V
		GPS_Digital IO	-0.3	-	0.35xVDD_1V8	V
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	K Ω
R_{PD}	Weak pull-down Equivalent resistor	V_{IN} =VDD_3V3	30	45	60	K Ω

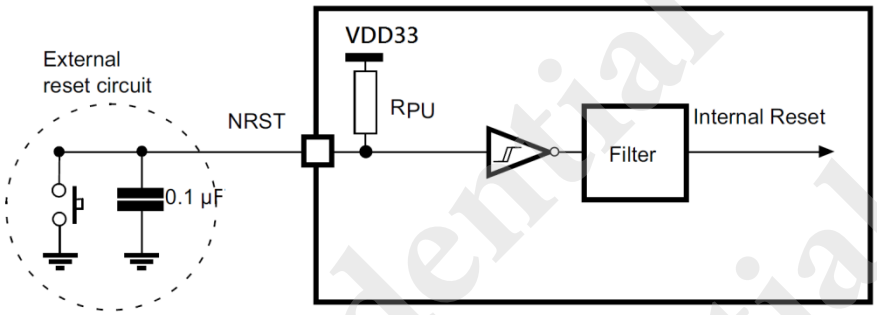
Output voltage levels

Symbol	Description	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port / IIO = +8 mA 2.7 V≦VDD_3V3≦3.6 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		VDD_3V3-0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port / IIO =+ 8 mA 2.7 V≦VDD_3V3≦3.6 V	-	0.4	
V_{OH}	Output high level voltage for an I/O pin	TTL port / IIO =- 6 mA 2.7 V≦VDD_3V3≦3.6 V	2.4	-	
V_{OL}	Output low level voltage for an I/O pin	IIO = +15 mA 2.7 V≦VDD_3V3≦3.6 V	-	1.3	
V_{OH}	Output high level voltage for an I/O pin	IIO = -15 mA 2.7 V≦VDD_3V3≦3.6 V	VDD_3V3-1.3	-	
V_{OL}	Output low level voltage for an I/O pin	IIO = +4 mA 1.65 V≦VDD_3V3≦3.6 V	-	0.45	
V_{OH}	Output high level voltage for an I/O pin	IIO = +4 mA 1.65 V≦VDD_3V3≦3.6 V	VDD_3V3-0.45	-	
V_{OL}	Output low level voltage	GPS_Digital IO	-	0.2xVDD_1V8	
V_{OH}	Output high level voltage	GPS_Digital IO	0.8xVDD_1V8	-	

2-7.2. NRST pin characteristics

The NRST pin input driver uses CMOS technology.
It is connected to a permanent pull-up resistor (R_{PU}).

The following figure is recommended NRST pin protection circuit against parasitic resets.



Symbol	Description	Conditions	Min	Typ.	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		VSS		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage		1.4		VDD_3V3	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2mA 2.7V＜VDD_3V3＜3.6V			0.4	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 1.5mA 1.65V＜VDD_3V3＜2.7V			0.4	V
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis			10% VDD_3V3		mV
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	K Ω
V_F	NRST Input filtered pulse				50	nS
V_{NF}	NRST Input not filtered pulse	VDD_3V3 > 2.7 V		350		nS

3. Pin Definition

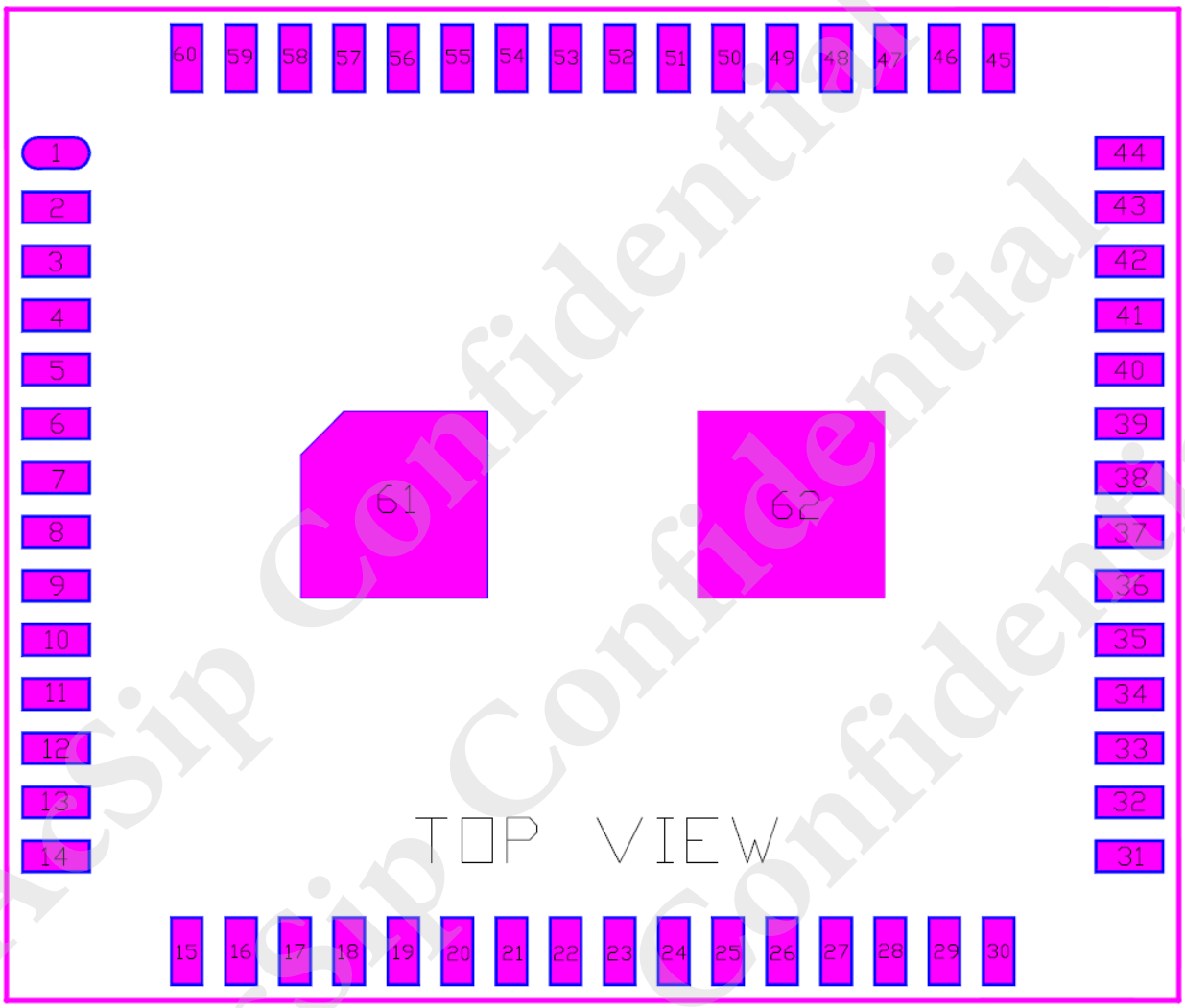
Pin	Definition	I/O	Power Domain	Description
1	VDD_3V3		VDD_3V3	Power Supply
2	GND			Ground pin
3	GND			Ground pin
4	MCU_Reset	I/O	VDD_3V3	Hardware reset pin
5	GND			Ground pin
6	OSC32_IN	I/O		MCU RTC 32.768KHz crystal input
7	OSC32_OUT	I/O		MCU RTC 32.768KHz crystal output
8	GND			Ground pin
9	PA0	I/O	VDD_3V3	MCU pin name: PA0
10	PA2	I/O	VDD_3V3	MCU pin name: PA2
11	PA3	I/O	VDD_3V3	MCU pin name: PA3
12	GND			Ground pin
13	GPS_I2C_SDA	I/O	VDD_1V8	GPS_I2C bus for sensor
14	GPS_I2C_SCL	I/O	VDD_1V8	GPS_I2C bus for sensor
15	PA4	I/O	VDD_3V3	MCU pin name: PA4
16	PA5	I/O	VDD_3V3	MCU pin name: PA5
17	PA6	I/O	VDD_3V3	MCU pin name: PA6
18	PA7	I/O	VDD_3V3	MCU pin name: PA7
19	PC4	I/O	VDD_3V3	MCU pin name: PC4
20	PB0	I/O	VDD_3V3	MCU pin name: PB0
21	PB1	I/O	VDD_3V3	MCU pin name: PB1
22	GPS_TCXO_EN	O	VDD_1V8	GPS 26MHz TCXO enabler
23	GPS_1PPS_OUT	I/O	VDD_1V8	Interrupt output / 1PPS out
24	GPS_RST_X	I	VDD_1V8	GPS Reset pin, Connect to host is active low reset,
25	GPS_UART_TXD	I/O	VDD_1V8	Reserved for GPS Uart_TX test port
26	GPS_UART_RXD	I/O	VDD_1V8	Reserved for GPS Uart_RX test port
27	GND			Ground pin
28	RXTX/RFMOD	I/O	VDD_3V3	Control signal from SX1276, which connects to internal RF switch at the same time.
29	GND			Ground pin
30	RF_ANT	I/O		LoRa RF I/O

Pin	Definition	I/O	Power Domain	Description
31	PA1_RF_FEM_CPS	O	VDD_3V3	Control signal from MCU_PA1, which connects to internal RF switch at the same time.
32	GND			Ground pin
33	NC			
34	GND			Ground pin
35	GND			Ground pin
36	NC			
37	GND			Ground pin
38	NC			
39	GND			Ground pin
40	NC			
41	GND			Ground pin
42	NC			
43	GND			Ground pin
44	GPS_ANT	I		GPS RF Input
45	PA8	I/O	VDD_3V3	MCU pin name: PA8
46	PA9_USART1_TX	I/O	VDD_3V3	MCU pin name: PA9
47	PA10_USART1_RX	I/O	VDD_3V3	MCU pin name: PA10
48	PA11	I/O	VDD_3V3	MCU pin name: PA11
49	PA12	I/O	VDD_3V3	MCU pin name: PA12
50	PA13_SWDIO		VDD_3V3	Serial wire (SWD) debug interface
51	PA14_SWCLK		VDD_3V3	Serial wire (SWD) debug interface
52	GPS_TCXO_CLK_IN	I/O	VDD_1V8	GPS 26MHz Clock input from TCXO
53	GND			Ground pin
54	VDD_1V8		VDD_1V8	Power Supply
55	NC			
56	PB5	I/O	VDD_3V3	MCU pin name: PB5
57	PB6_SCL	I/O	VDD_3V3	MCU pin name: PB6
58	PB7_SDA	I/O	VDD_3V3	MCU pin name: PB7
59	BOOT0	I	VDD_3V3	Boot mode selection pin
60	PB8	I/O	VDD_3V3	MCU pin name: PB8
61	GND			Ground Pin
62	GND			Ground Pin

※ For detailed functions of pin definitions, please refer to STM32L073 datasheet.

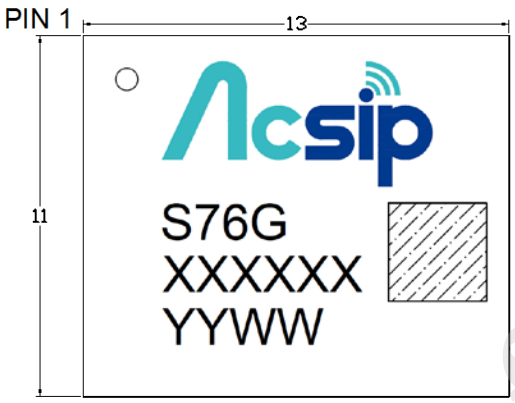
3-1. Pin Assignment

The SiP module will conform to the following pin map, shown in the following diagram (top view)

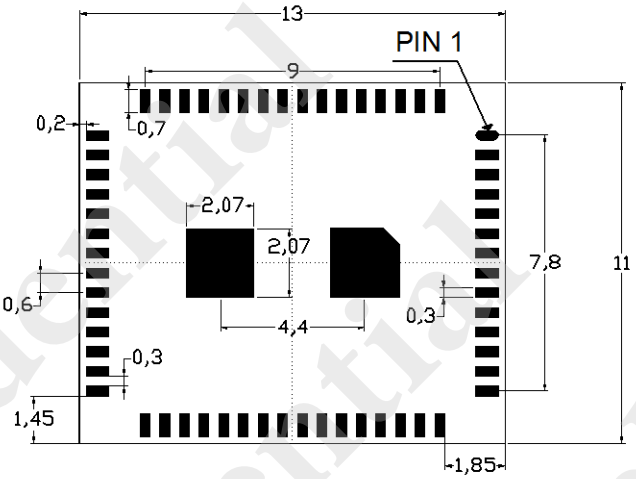


4. Mechanical Dimension

Unit: mm



TOP VIEW



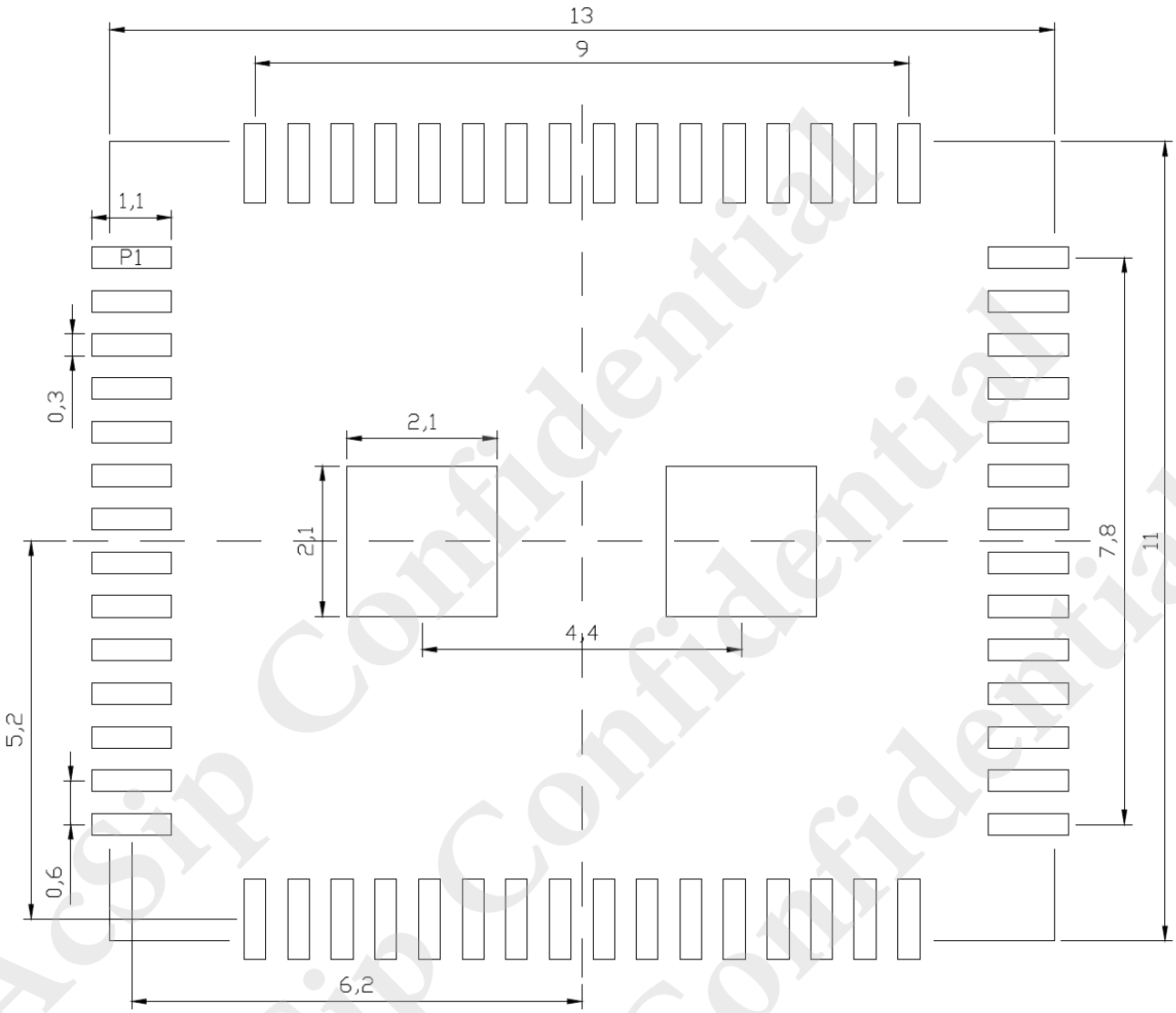
BOTTOM VIEW

SIDE VIEW

Unit : ±0.05mm

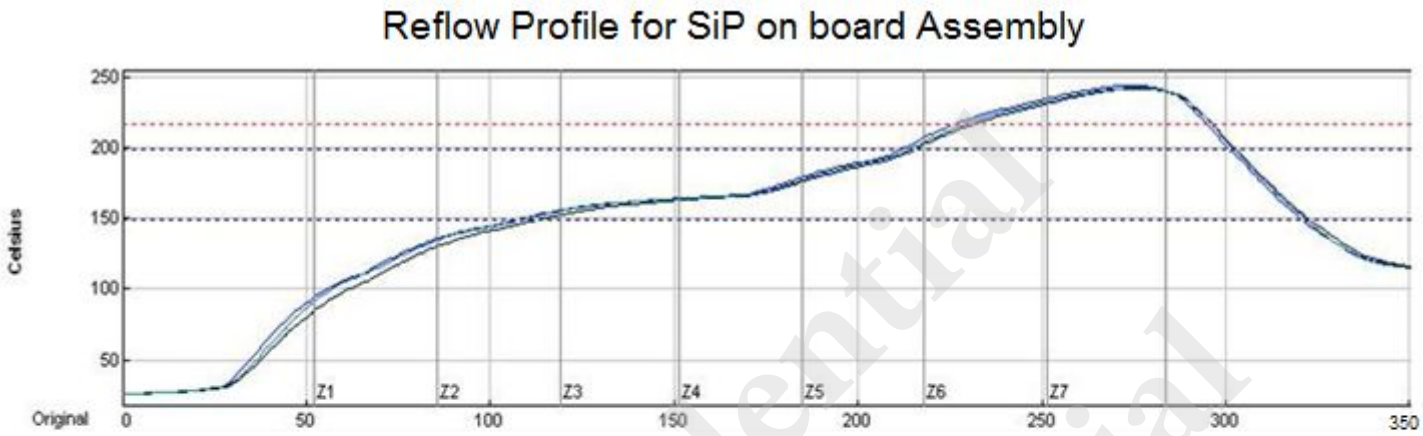
4-1. Recommended Footprint

Unit: mm



TOP View

5. Recommended Reflow Profile



Preheat time	150℃—200℃: 105+/-15sec
Dwell time	Over 220℃: 70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp Up/Down Rate	Up: 3 +0/-2 ℃/ sec Down: 2 +0/-1℃/ sec

6. SiP Module Preparation

6-1. Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

6-2. SMT Preparation

1. Calculated shelf life in sealed bag: 6 months at<40℃ and <90% relative humidity (RH).
2. Peak package body temperature: 250℃.
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.
   A. Mounted within: 168 hours of factory conditions<30℃/60%RH.
   B. Stored at≦10%RH with N2 flow box.
4. Devices require baking, before mounting, if:
   A. Package bag does not keep in vacuumed while first time open.
   B. Humidity Indicator Card is >10% when read at 23±5℃.

C. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.

5. If baking is required, devices may be baked for 12 hours at 125±5℃.

7. Package Information

7-1. Product Marking

Figure 1 below details the standard product marking for all AcSiP Corp. products. Cross reference to the applicable line number and table for a full detail of all the variables.

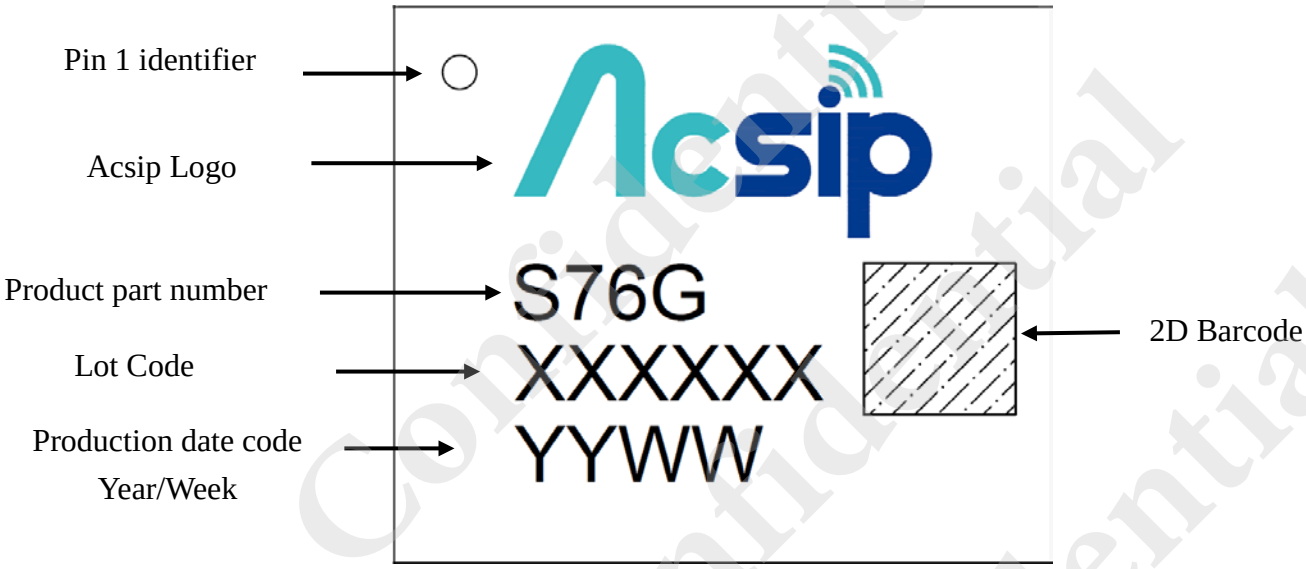
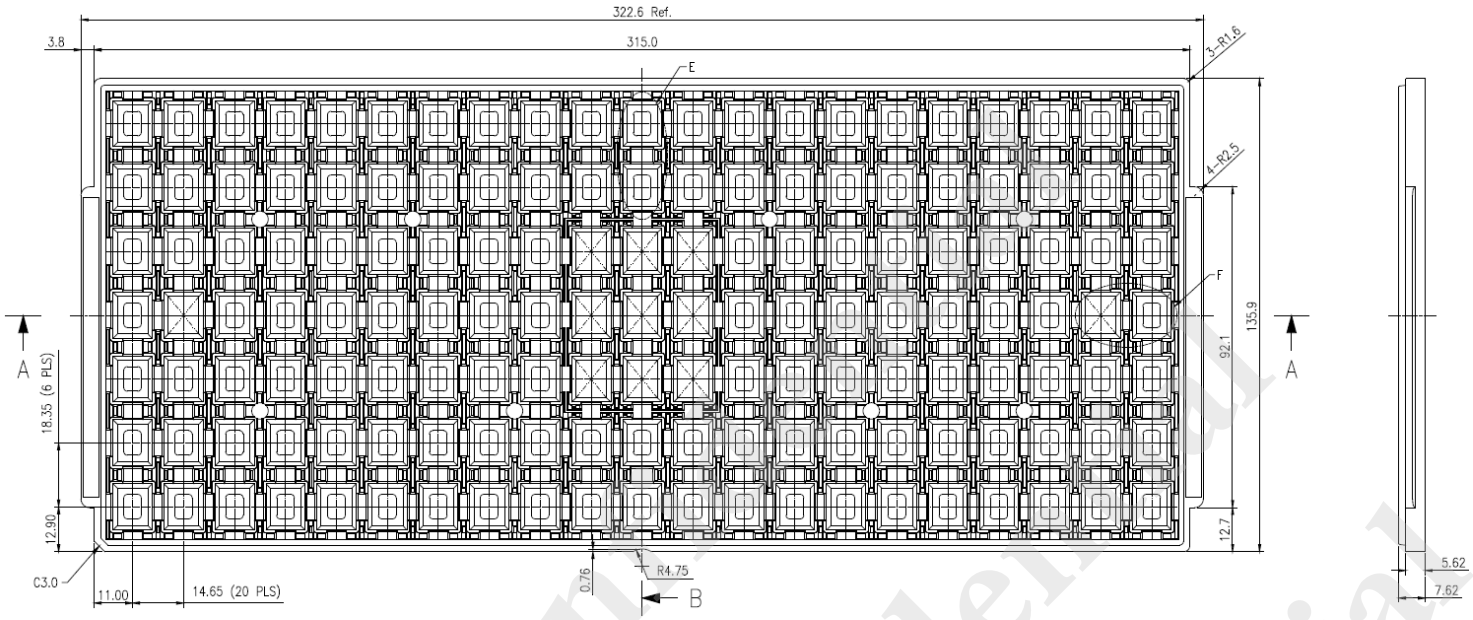


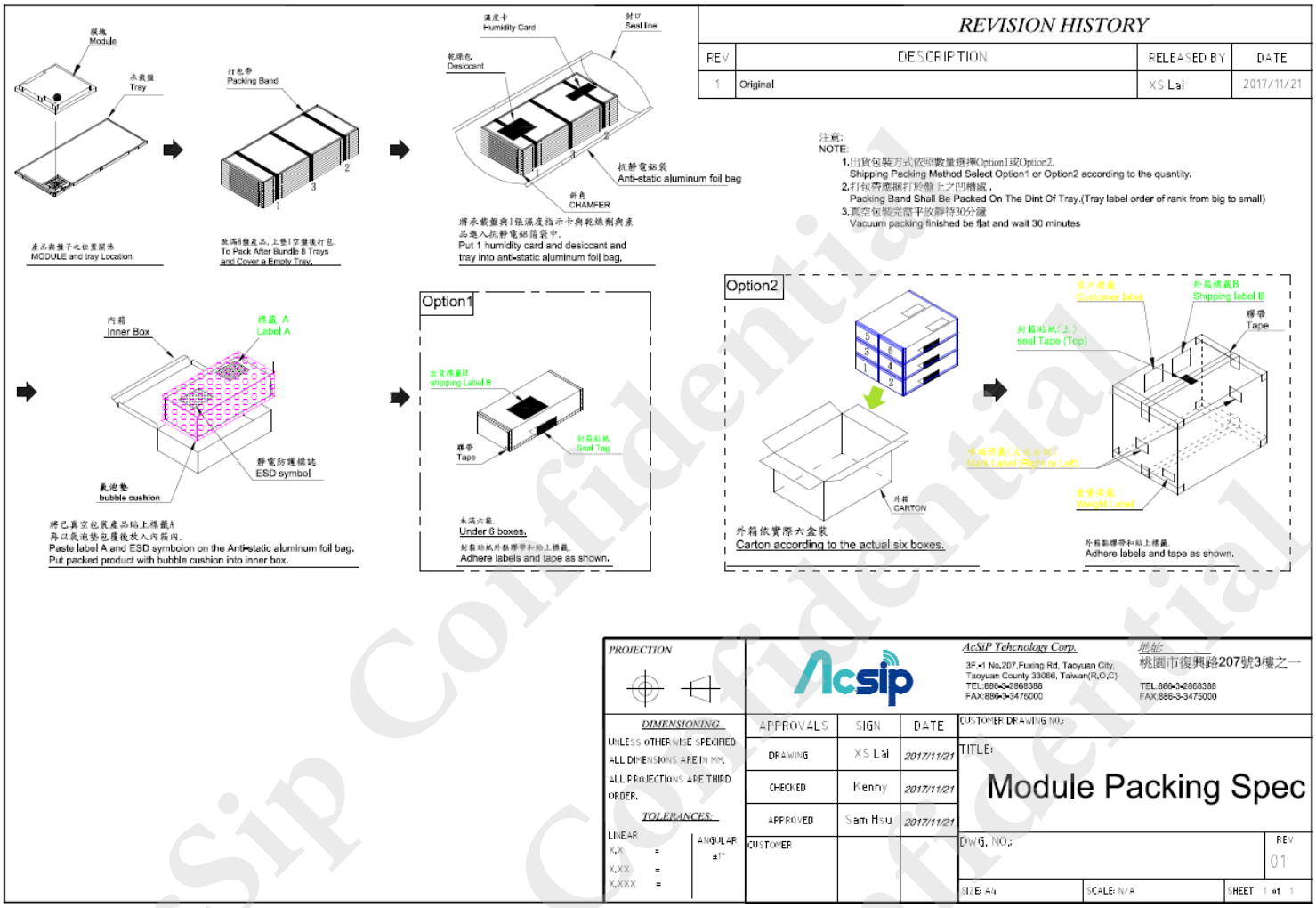
Figure 1 Standard Product Marking Diagram- TOP VIEW

7-2. Tray Dimension

Unit: mm



8-1. Packing Information



8-2. Humidity Indicator Card

Dry Wet

Indicates 指示點:
10%,20%,30,40%,50%,60% relative humidity
10%,20%,30,40%,50%,60% 相對濕度

Color Change 顏色變化:
Brown (Dry) ---> Blue (Wet)
棕色 (乾燥) ---> 藍色 (潮溼)