BG77 Hardware Design

LPWA Module Series

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About the Document

Revision History

Revision	Date	Author	Description
1.0	2020-01-10	Lyndon LIU/ Newgate HUA/ Hyman DING	Initial

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1 Introduction

This document defines BG77 module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document helps customers quickly understand the interface specifications, electrical and mechanical details, as well as other related information of BG77. To facilitate application designs, it also includes some reference designs for customers' reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with BG77.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating BG77 module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for any user's failure to observe these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

BG77 is an embedded IoT (LTE Cat M1, LTE Cat NB2) wireless communication module. It provides data connectivity on LTE-FDD network, and supports half-duplex operation in LTE network. It also provides optional GNSS and voice* [1] functionality to meet customers' specific application demands.

Table 1: Frequency Bands and GNSS Types of BG77 Module

Module	Supported Bands	Power Class	GNSS
BG77	**Cat M1:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B14/B18/ B19/B20/B25/B26/ B27/B28/B66/B85* **Cat NB2 [2]:** LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/ B20/B25/B26/B28/B66/B71/B85*	Power Class 5 (21 dBm)	GPS, GLONASS, BeiDou, Galileo, QZSS

NOTES

1. [1] BG77 supports VoLTE (Voice over LTE) under LTE Cat M1.
2. [2] LTE Cat NB2 is backward compatible with LTE Cat NB1.
3. GNSS function is optional.
4. "*" means under development.

With a compact profile of 14.9 mm × 12.9 mm × 1.7 mm, BG77 can meet almost all requirements for M2M applications such as smart metering, tracking system, security, wireless POS, etc. It is especially suitable for size and weight sensitive applications such as smart watch and other wearable devices.

BG77 is an SMD type module which can be embedded into applications through its 94 LGA pads. It supports internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of BG77 module.

Table 2: Key Features of BG77

Features	Details
Power Supply [1)]	● Supply voltage: 2.6–4.8 V ● Typical supply voltage: 3.3 V
Transmitting Power	Class 5 (21 dBm +1.7/-3 dB) for LTE-FDD bands
LTE Features	● Support 3GPP Rel. 14 ● Support LTE Cat M1 and LTE Cat NB2 ● Support 1.4 MHz RF bandwidth for LTE Cat M1 ● Support 200 KHz RF bandwidth for LTE Cat NB2 ● Cat M1: Max. 588 kbps (DL)/1119 kbps (UL) ● Cat NB2: Max. 127 kbps (DL)/158.5 kbps (UL)
Internet Protocol Features	● Support PPP/TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/NITZ/PING/MQTT/LwM2M/CoAP* protocols ● Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Support 1.8 V USIM/SIM card only
PCM Interface*	Support one digital audio interface: PCM interface
USB Interface	● Compliant with USB 2.0 specification (slave only) ● Support operations at low-speed and full-speed ● Used for AT command communication, data transmission, GNSS NMEA output, software debugging and firmware upgrade ● Support USB serial drivers for Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x
UART Interfaces	**Main UART:** ● Used for data transmission and AT command communication ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Support RTS and CTS hardware flow control **Debug UART:**

	● Used for software debugging and log output ● Support 115200 bps baud rate **GNSS UART:** ● Used for GNSS data and NMEA sentences output ● 115200 bps baud rate by default
GNSS (Optional)	● Gen9 VT of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS) ● 1 Hz data update rate by default
AT Commands	● 3GPP TS 27.007 and 3GPP TS 27.005 AT commands ● Quectel enhanced AT commands
Network Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	Main antenna (ANT_MAIN) and GNSS antenna (ANT_GNSS) interfaces
Physical Characteristics	● Dimensions: (14.9 ±0.15) mm × (12.9 ±0.15) mm × (1.7 ±0.2) mm ● Weight: approx. 0.73 g
Temperature Range	● Operation temperature range: -35 °C to +75 °C [2)] ● Extended temperature range: -40 °C to +85 °C [3)] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface ● DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. In order to ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.
2. [2)] Within operation temperature range, the module is 3GPP compliant.
3. [3)] Within extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the normal operation temperature levels, the module will meet 3GPP specifications again.
4. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of BG77 and illustrates the major functional parts.

- Power management
- Baseband

- Radio frequency
- Peripheral interfaces

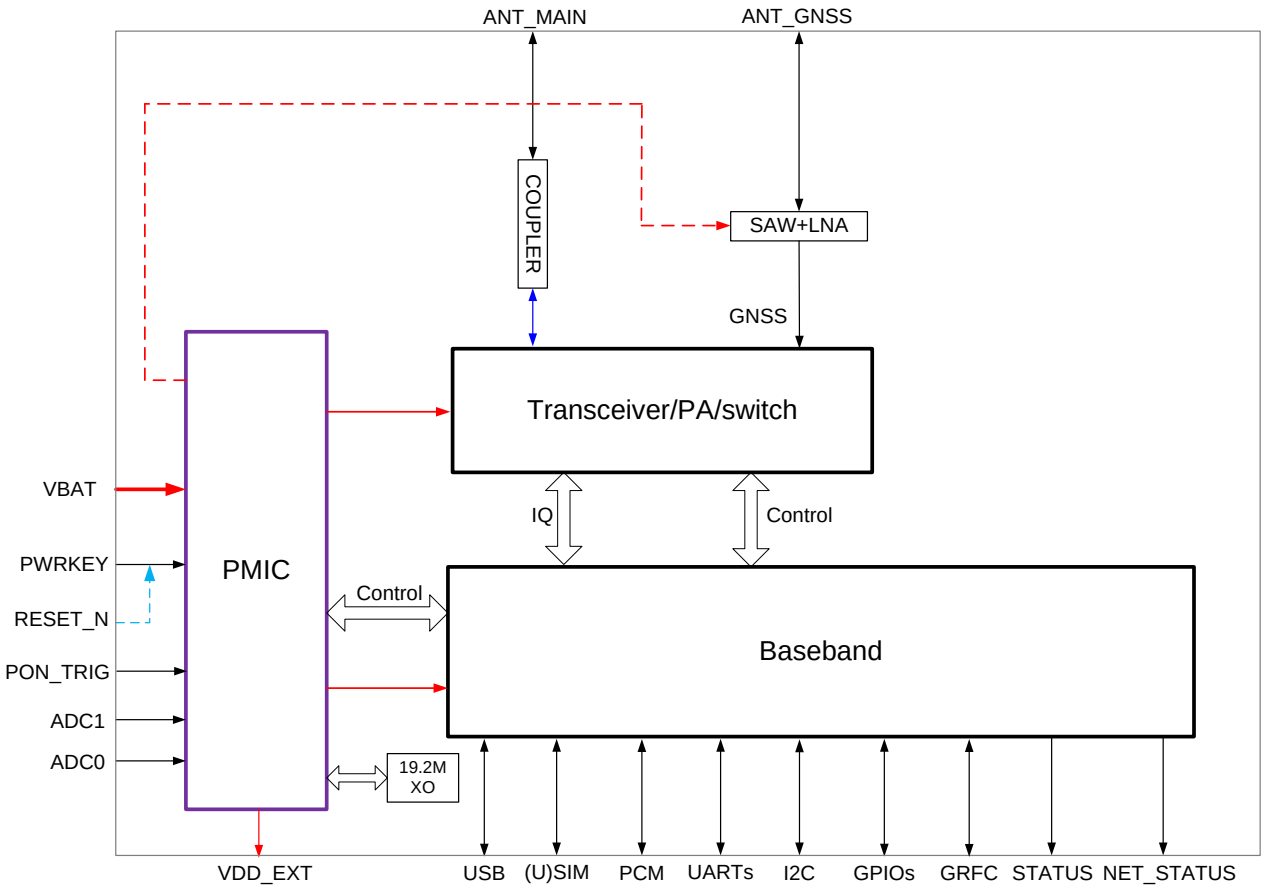


Figure 1: Functional Diagram

NOTES

1. PWRKEY output voltage is 1.5 V because of the voltage drop inside the Qualcomm chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, PWRKEY should never be pulled down to GND permanently.
2. RESET_N is connected directly to PWRKEY inside the module.

2.4. Evaluation Board

In order to facilitate application development with BG77 conveniently, Quectel supplies the evaluation board (EVB), USB to RS-232 converter cable, USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

BG77 is equipped with 94 LGA pads that can be connected to customers' cellular application platforms. The subsequent chapters will provide detailed description of interfaces listed below:

- Power supply
- PON_TRIG Interface
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces*
- Status indication interfaces
- USB_BOOT interface
- ADC interfaces
- GPIO interfaces*
- GRFC interfaces*

NOTE

"*" means under development.

3.1. Pin Assignment

The following figure shows the pin assignment of BG77.

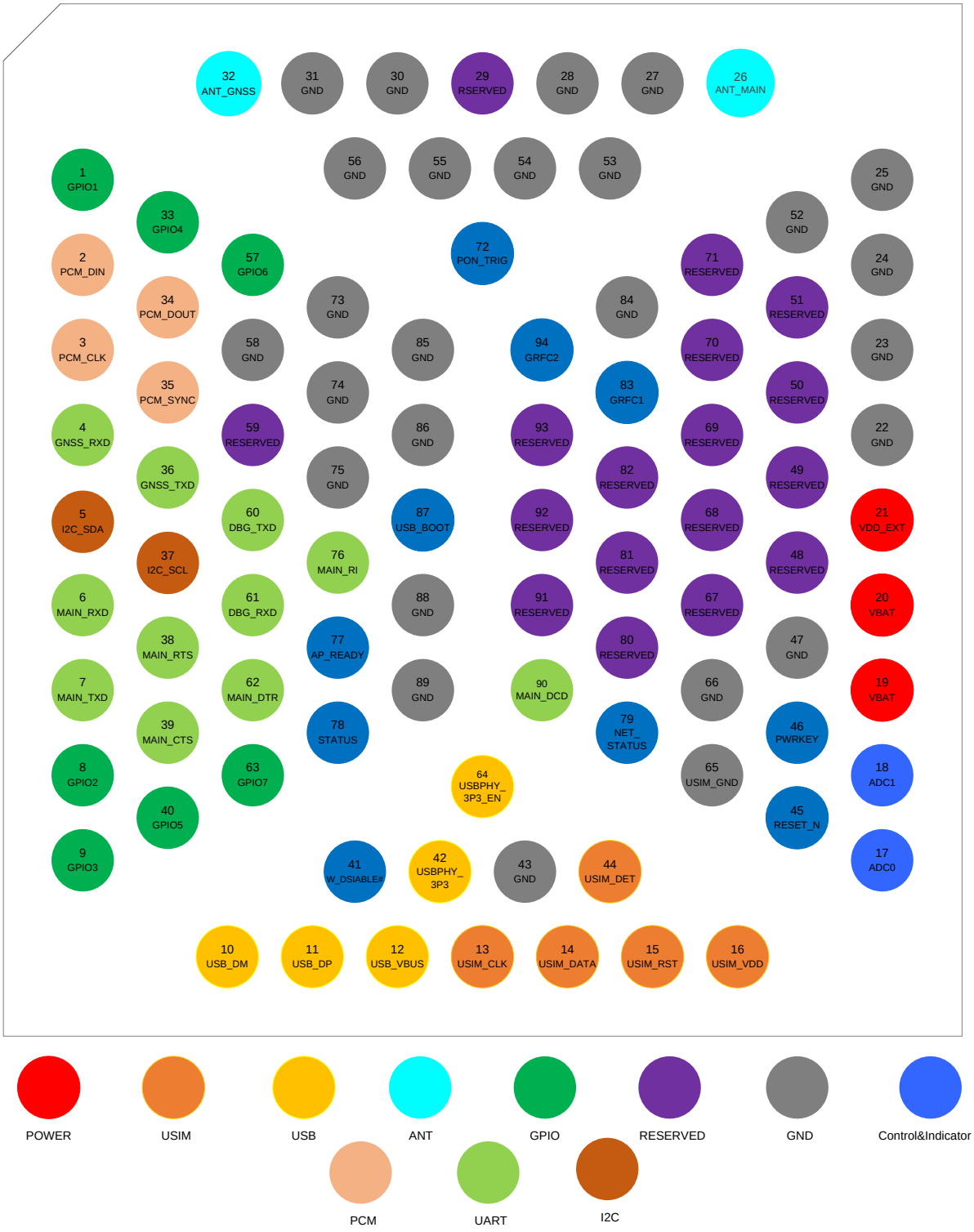


Figure 2: Pin Assignment (Top View)

NOTES

1. PWRKEY output voltage is 1.5 V because of the voltage drop inside the Qualcomm chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, PWRKEY should never be pulled down to GND permanently.
2. RESET_N is connected directly to PWRKEY inside the module.
3. ADC input voltage must not exceed 1.8 V.
4. The input voltage range of USB_VBUS is 1.3–1.8 V.
5. Keep all RESERVED pins and unused pins unconnected.
6. GND pins should be connected to ground in the design.
7. GPIO5 (pin 40), NET_STATUS (pin 79) and GPRC1 (pin 83) are BOOT_CONFIG pins. They should not be pulled up before startup.

3.2. Pin Description

The following tables show the pin definition and description of BG77.

Table 3: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	19, 20	PI	Power supply for the module	Vmax = 4.8 V Vmin = 2.6 V Vnorm = 3.3 V	Please refer to NOTE 1
VDD_EXT	21	PO	1.8 V output power supply for external circuits	Vnorm = 1.8 V $I_O$max = 50 mA	If unused, keep this pin open.
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	46	DI	Turn on/off the module	Vnorm = 1.5 V V_{IL}max = 0.45 V	PWRKEY should never be pulled down to GND permanently.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	45	DI	Reset the module	Vnorm = 1.5 V V_{IL}max = 0.45 V	
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	78	DO	Module operation status indication	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep this pin open.
NET_STATUS	79	DO	Module network activity status indication	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	BOOT_CONFIG. Do not pull it up before startup.

					1.8 V power domain. If unused, keep this pin open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	12	AI	USB connection detection	V_{IH}max = 1.8 V V_{IH}min = 1.3 V	
USB_DP	11	IO	USB differential data (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	10	IO	USB differential data (-)		
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Vnorm = 3.3 V	
USBPHY_3P3_EN	64	DO	External LDO enable control for USB	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET*	44	DI	(U)SIM card hot-plug detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	16	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	15	DO	(U)SIM card reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_DATA	14	IO	(U)SIM card data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_CLK	13	DO	(U)SIM card clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_GND	65		Specified ground for (U)SIM card		
Main UART Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RXD	6	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_TXD	7	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_CTS	39	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RTS	38	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
MAIN_DCD	90	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
MAIN_RI	76	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	61	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
DBG_TXD	60	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
GNSS UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_TXD	36	DO	GNSS UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this

					pin open.
GNSS_RXD	4	DI	GNSS UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	3	DO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_SYNC	35	DO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
PCM_DIN	2	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM_DOUT	34	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
I2C Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	37	OD	I2C serial clock (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep this pin open.
I2C_SDA	5	OD	I2C serial data (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep this pin open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	26	IO	Main antenna interface		50 Ω impedance

ANT_GNSS	32	AI	GNSS antenna interface		50 Ω impedance. If unused, keep this pin open.
GPIO Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	1	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO2	8	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO3	9	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO4	33	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO5	40	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GPIO6	57	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.

GPIO7	63	IO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	17	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep this pin open.
ADC1	18	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep this pin open.
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#*	41	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.
AP_READY*	77	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USB_BOOT	87	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PON_TRIG	72	DI	Wake up the module from PSM		1.8 V power domain. Rising-edge triggered. Pulled-down by default. If unused, keep this pin open.
GRFC Interfaces*					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GRFC2	94	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	29, 48–51, 59, 67–71, 80–82, 91–93		Reserved		Keep these pins open.

NOTES

1. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. In order to ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.
2. PWRKEY output voltage is 1.5 V because of the voltage drop inside the Qualcomm chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, PWRKEY should never be pulled down to GND permanently.
3. RESET_N is connected directly to PWRKEY inside the module.
4. The input voltage range of USB_VBUS is 1.3–1.8 V.
5. USBPHY_3P3 and USBPHY_3P3_EN pins are used for USB PHY circuits.
6. GPIO5 (pin 40), NET_STATUS (pin 79) and GPRC1 (pin 83) are BOOT_CONFIG pins. They should not be pulled up before startup.
7. ADC input voltage must not exceed 1.8 V.
8. Keep all RESERVED pins and unused pins unconnected.
9. "*" means under development.

3.3. Operating Modes

The table below briefly summarizes the various operating modes of BG77.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Connected	Network has been connected. In this mode, the power consumption may vary with the network setting and data transfer rate.
	Idle	Software is active. The module remains registered on network, and it is ready to send and receive data.
Extended Idle Mode DRX (e-I-DRX)	BG77 module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE#* pin can set the module into airplane mode. In this case, RF function will be invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to a lower level. During this mode, the module can still receive paging message, SMS and TCP/UDP data from the network normally.	
Power OFF Mode	In this mode, the power management unit shuts down the power supply. The software is not active. The serial interfaces are not accessible. But the operating voltage (connected to VBAT) remains applied.	
Power Saving Mode (PSM)	The module may enter PSM to reduce its power consumption. PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections.	

NOTES

1. During e-I-DRX, it is recommended to use UART interface for data communication, as the use of USB interface will increase power consumption.
2. "*" means under development.

3.4. Power Saving

3.4.1. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

W_DISABLE#* is pulled up by default. Driving it low will let the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE#* is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command which is still under development. Details about the command will be provided in ***document [2]***.
2. The execution of **AT+CFUN** command will not affect GNSS function.
3. "*" means under development.

3.4.2. Power Saving Mode (PSM)

BG77 module can enter PSM to reduce its power consumption. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. So BG77 in PSM cannot immediately respond users' requests.

When the module wants to use the PSM it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, it will confirm the usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g. when the conditions are changed in the module, the module consequently requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS** command.

Either of the following methods will wake up the module from PSM:

- A rising edge on PON_TRIG will wake up the module from PSM. (Recommended)

- Drive PWRKEY low will wake up the module.
- When the T3412_Ext timer expires, the module will be woken up automatically.

NOTE

Please refer to ***document [2]*** for details about **AT+CPSMS** command.

3.4.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what was requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by **AT+CEDRXS=1** command.

NOTE

Please refer to ***document [2]*** for details about **AT+CEDRXS** command.

3.4.4. Sleep Mode

BG77 is able to reduce its current consumption to a lower value during the sleep mode. The following sub-chapters describe the power saving procedure of BG77.

3.4.4.1. UART Application

If the host communicates with the module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK = 1** command to enable sleep mode.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

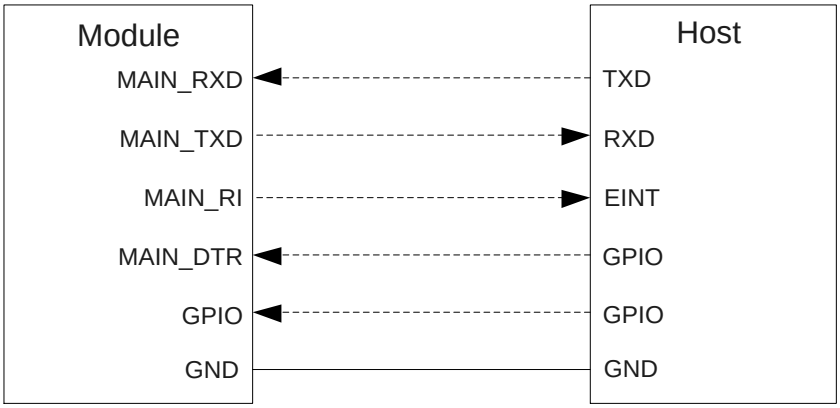


Figure 3: Sleep Mode Application via UART

- When BG77 has URC to report, MAIN_RI signal will wake up the host. Please refer to ***Chapter 3.14*** for details about MAIN_RI behavior.
- Driving the host MAIN_DTR low will wake up the module.
- AP_READY* will detect the sleep state of the host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"** command in ***document [2]*** for details.

NOTE

"*" means under development.

3.5. Power Supply

3.5.1. Power Supply Pins

BG77 provides two VBAT pins for connection with an external power supply.

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT [1)]	19, 20	Power supply for the module	2.6	3.3	4.8	V
GND	22–25, 27, 28, 30, 31, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89	Ground	-	-	-	-

NOTES

[1)] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. In order to ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

3.5.2. Decrease Voltage Drop

The power supply range of BG77 is from 2.6 V to 4.8 V. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. In order to ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V. Please assure the input voltage will never drop below 2.6 V.

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be no less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a TVS with low leakage current and suitable reverse stand-off voltage, and also it is recommended to place it as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

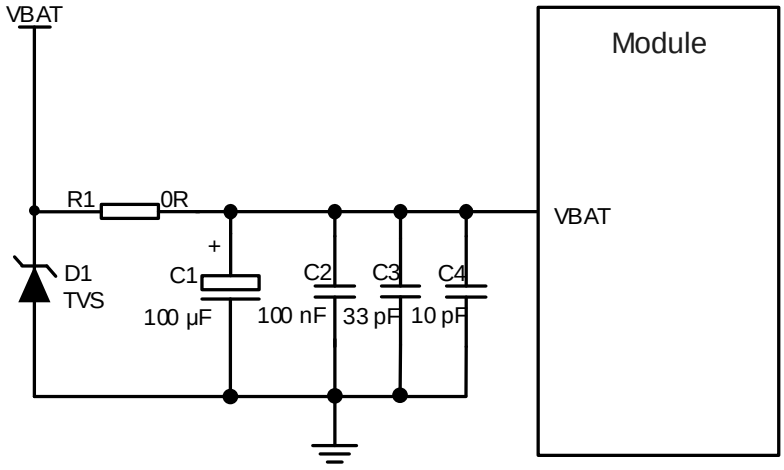


Figure 4: Star Structure of the Power Supply

3.5.3. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT voltage value. For more details, please refer to ***document [2]***.

3.6. Turn on and off Scenarios

3.6.1. Turn on Module Using the PWRKEY Pin

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	46	Turn on/off the module	Vnorm = 1.5 V V_{IL}max = 0.45 V	The output voltage is 1.5 V because of the voltage drop inside the Qualcomm chipset.

When BG77 is in power off mode, it can be turned on by driving PWRKEY low for 500–1000 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

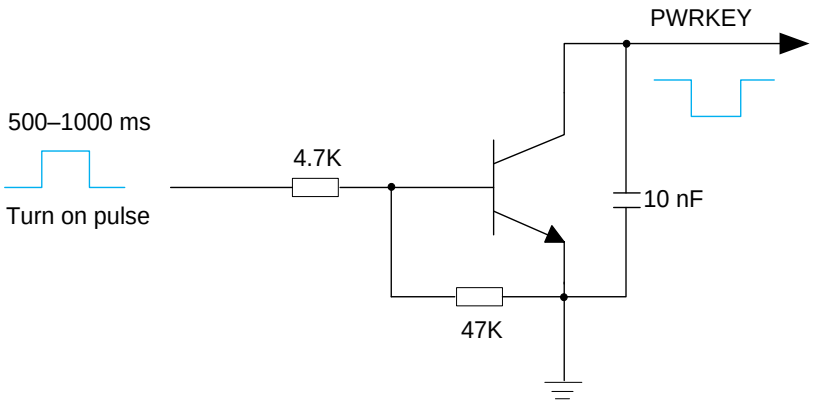


Figure 5: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

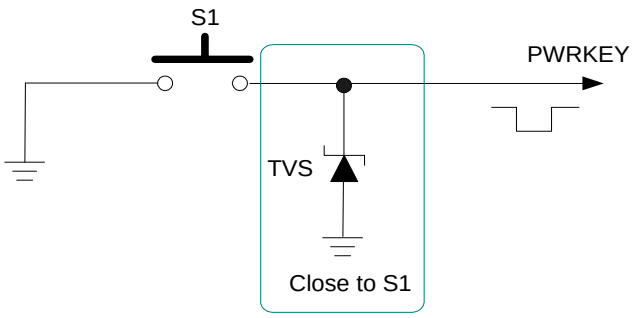


Figure 6: Turn on the Module Using Keystroke

The power on timing is illustrated in the following figure.

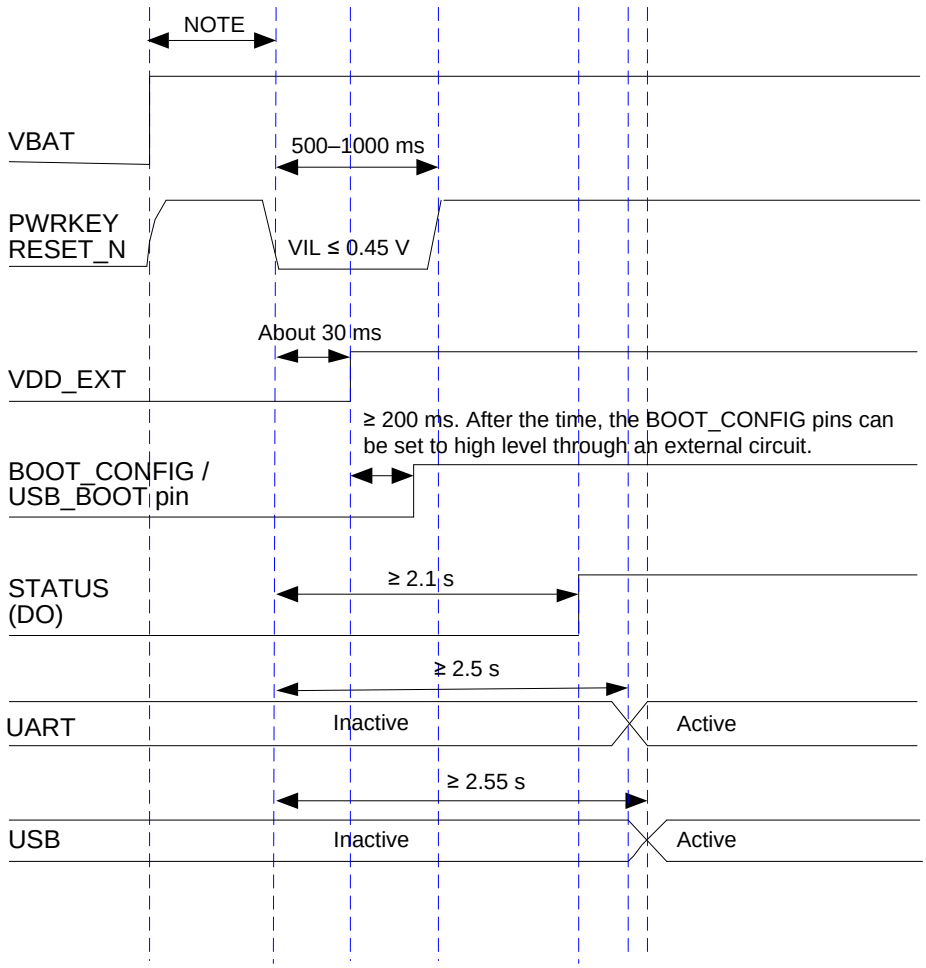


Figure 7: Power-on Timing

NOTES

1. Make sure that VBAT is stable before pulling down PWRKEY pin and keep the interval no less than 30 ms.
2. PWRKEY output voltage is 1.5 V because of the voltage drop inside the Qualcomm chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, PWRKEY should never be pulled down to GND permanently.

3.6.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module through PWRKEY.
- Normal power down procedure: Turn off the module through **AT+QPOWD** command.

3.6.2.1. Turn off Module through PWRKEY

Driving PWRKEY low for 650–1500 ms, the module will execute power-down procedure after PWRKEY is released.

The power-off timing is illustrated in the following figure.

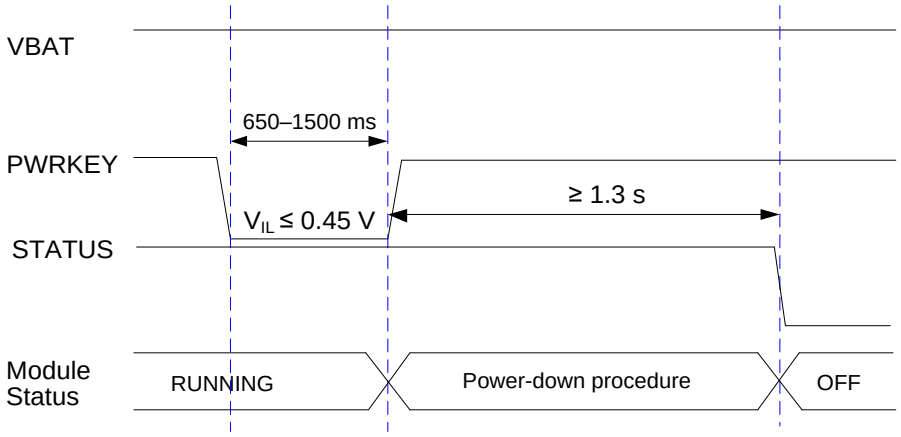


Figure 8: Power-off Timing

3.6.2.2. Turn off Module through AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

3.7. Reset the Module

RESET_N is used to reset the module. Due to platform limitations, the chipset has integrated the reset function into PWRKEY, and RESET_N is connected directly to PWRKEY inside the module.

The module can be reset by driving RESET_N low for 2–3.8 s.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	45	Reset the module	V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connected directly to PWRKEY inside the module).

The reset timing is illustrated in the following figure.

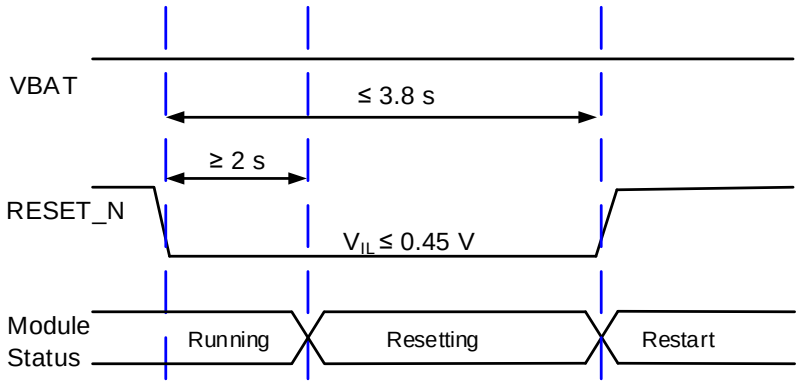


Figure 9: Reset Timing

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N pin.

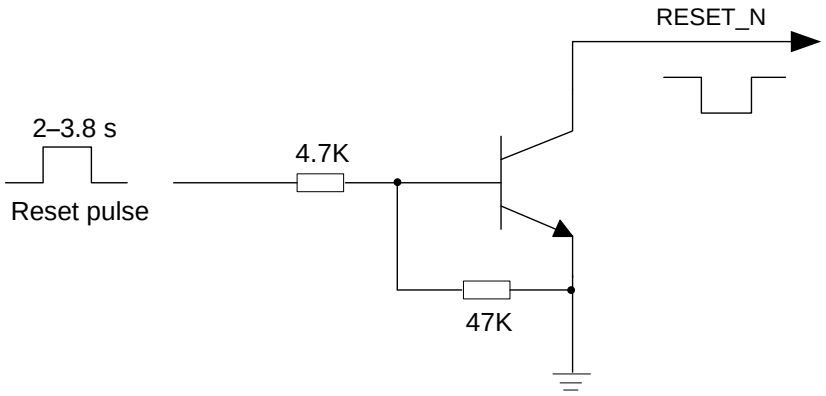


Figure 10: Reference Circuit of RESET_N by Using Driving Circuit

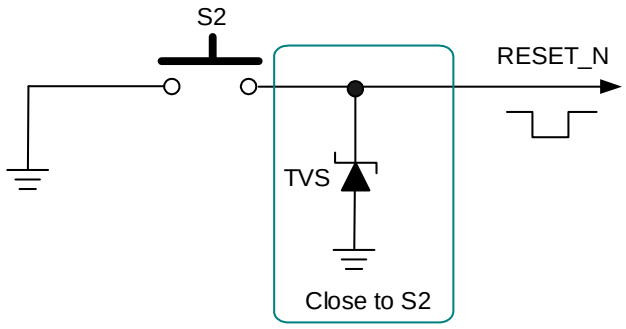


Figure 11: Reference Circuit of RESET_N by Using Button

NOTES

Please assure that there is no large capacitance on RESET_N pin.

3.8. PON_TRIG Interface

BG77 provides one PON_TRIG pin which is used to wake up the module from PSM. When the pin detects a rising edge, the module will be woken up from PSM.

Table 9: Pin Definition of PON_TRIG Interface

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	72	DI	Wake up the module from PSM	Rising-edge triggered. Pulled-down by default. 1.8 V power domain.

A reference circuit is shown in the following figure.

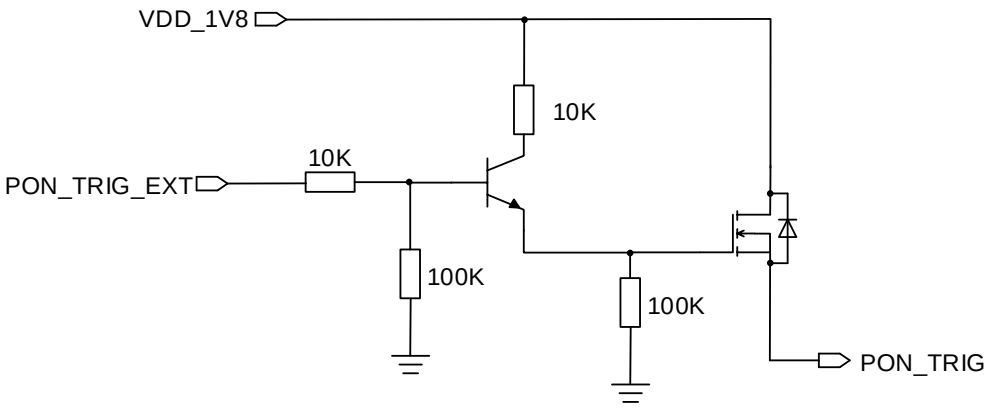


Figure 12: Reference Circuit of PON_TRIG Circuit

NOTE

VDD_1V8 is provided by an external LDO.

3.9. (U)SIM Interface

BG77 supports 1.8 V (U)SIM card only. The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET*	44	DI	(U)SIM card hot-plug detection	1.8 V power domain.
USIM_VDD	16	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.
USIM_RST	15	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	14	IO	(U)SIM card data	1.8 V power domain.
USIM_CLK	13	DO	(U)SIM card clock	1.8 V power domain.
USIM_GND	65		Specified ground for (U)SIM card	

BG77 supports (U)SIM card hot-plug via USIM_DET, and both high and low level detections are supported. The function is disabled by default, and please refer to **AT+QSIMDET** command in ***document [2]*** for details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

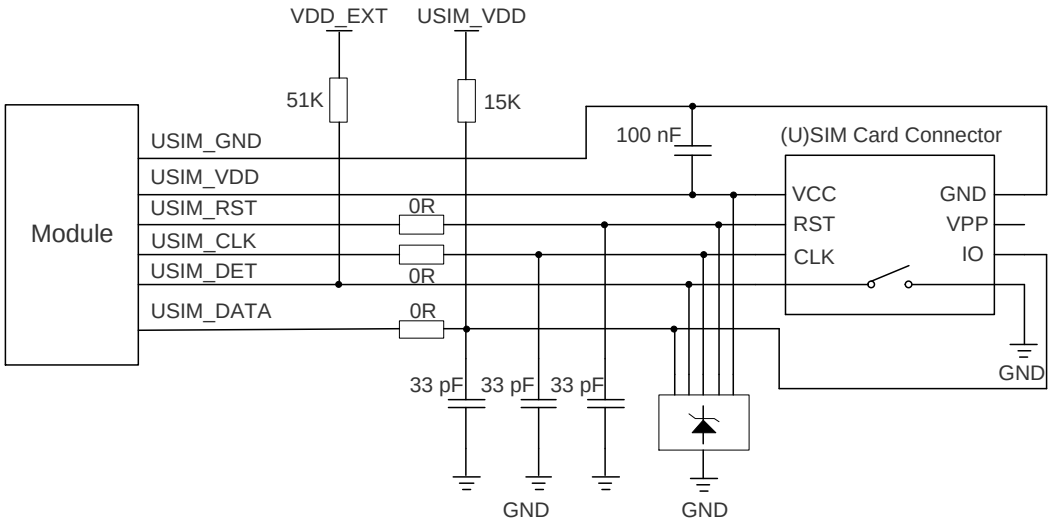


Figure 13: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

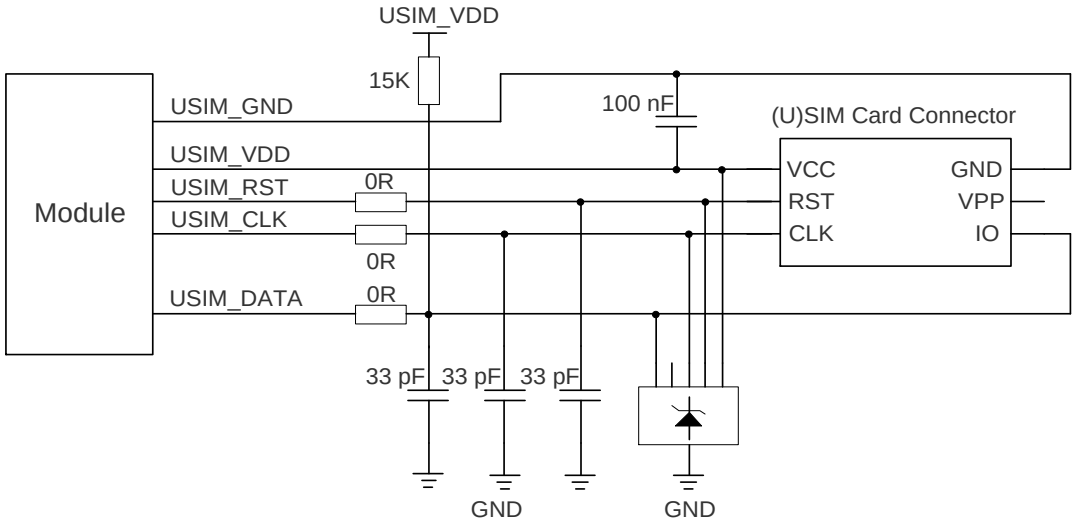


Figure 14: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be ground shielded.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. In order to facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

NOTE

"*" means under development.

3.10. USB Interface

BG77 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports operation at low-speed (1.5 Mbps) and full-speed (12 Mbps) modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	12	AI	USB connection detection	Input range: 1.3–1.8 V
USB_DP	11	IO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	10	IO	USB differential data (-)	
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Vnorm = 3.3 V

USBPHY_3P3_EN	64	DO	External LDO enable of USB	1.8 V power domain
GND	43		Ground	

For more details about USB 2.0 specification, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade or debugging in application designs. The following figures illustrate reference designs of USB PHY and USB interface.

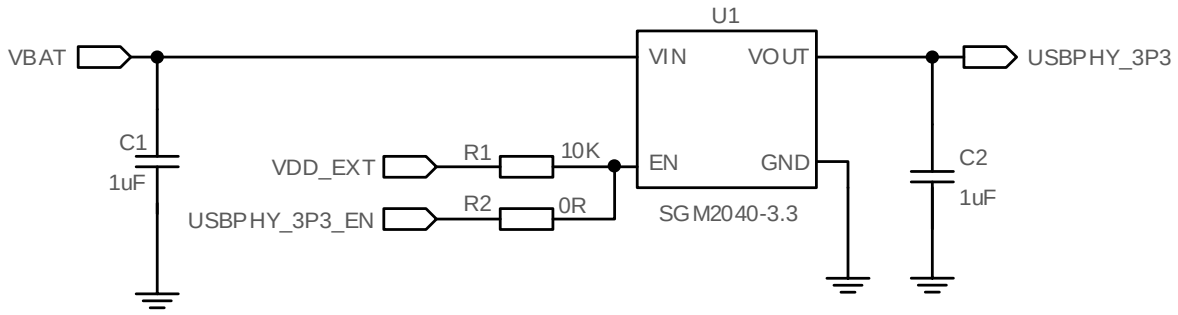


Figure 15: Reference Design of USB PHY

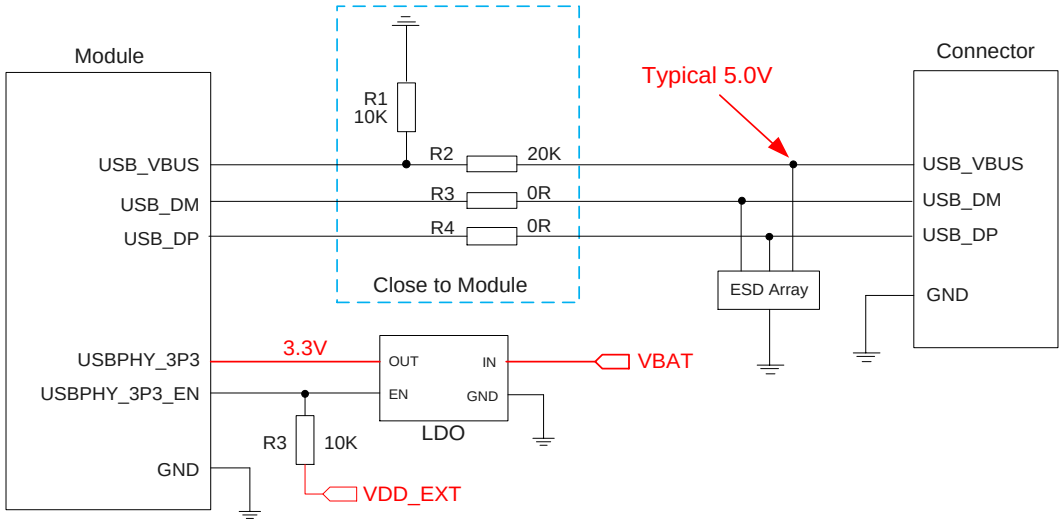


Figure 16: Reference Design of USB Interface

In order to ensure the integrity of USB data line signal, components R3 and R4 should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with while designing the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so please pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection devices as close to the USB connector as possible.

NOTES

1. BG77 can only be used as a slave device.
2. The input voltage range of USB_VBUS is 1.3–1.8 V.

3.11. UART Interfaces

The module provides three UART interfaces: the main UART, debug UART and the GNSS UART interfaces. Features of them are illustrated below:

- The main UART interface supports 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART interface supports a fixed baud rate of 115200 bps, and is used for software debugging and log output.
- The GNSS UART interface supports 115200 bps baud rate by default, and is used for GNSS data and NMEA sentences output.

The following tables show the pin definition of the three UART interfaces.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	1.8 V power domain

MAIN_RXD	6	DI	Main UART receive	1.8 V power domain
MAIN_TXD	7	DO	Main UART transmit	1.8 V power domain
MAIN_CTS	39	DO	Main UART clear to send	1.8 V power domain
MAIN_RTS	38	DI	Main UART request to send	1.8 V power domain
MAIN_DCD	90	DO	Main UART data carrier detect	1.8 V power domain
MAIN_RI	76	DO	Main UART ring indication	1.8 V power domain

NOTE

AT+IPR command can be used to set the baud rate of the main UART interface, and **AT+IFC** command can be used to set the hardware flow control (the function is disabled by default). Please refer to ***document [2]*** for more details about these AT commands.

Table 13: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	60	DO	Debug UART transmit	1.8 V power domain
DBG_RXD	61	DI	Debug UART receive	1.8 V power domain

Table 14: Pin Definition of GNSS UART Interface

Pin Name	Pin No.	I/O	Description	Comment
GNSS_TXD	36	DO	GNSS UART transmit	1.8 V power domain
GNSS_RXD	4	DI	GNSS UART receive	1.8 V power domain

The logic levels of UART interfaces are described in the following table.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V

V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if customers' application is equipped with a 3.3 V UART interface. The voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design of the main UART interface:

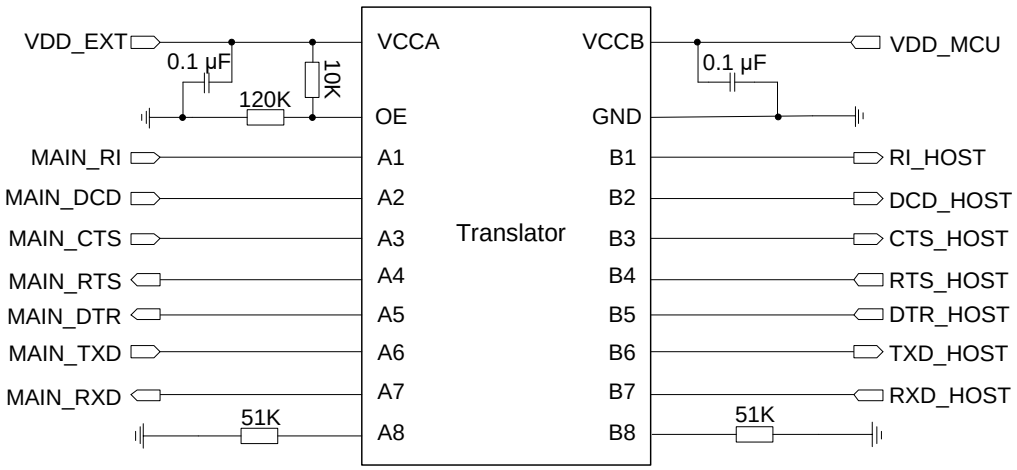


Figure 17: Main UART Reference Design (Translator Chip)

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of circuits in solid lines, but please pay attention to the direction of connection.

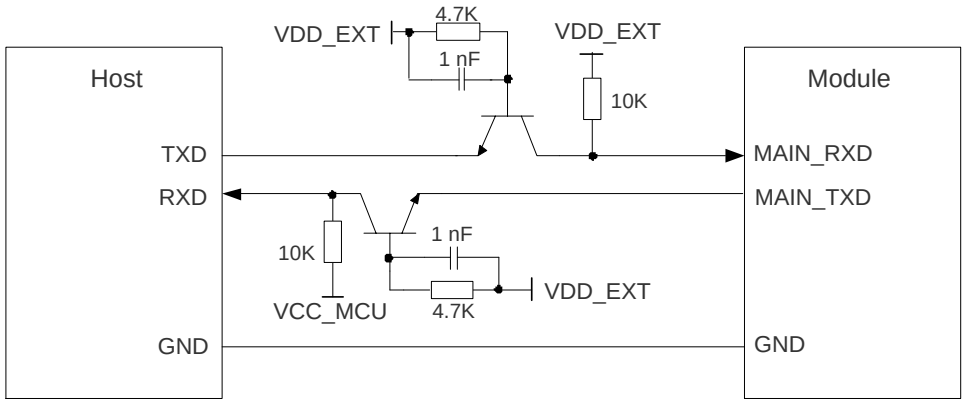


Figure 18: Main UART Reference Design (Transistor Circuit)

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.

3.12. PCM and I2C Interfaces*

BG77 provides one Pulse Code Modulation (PCM) digital interface and one I2C interface. The following table shows the pin definition of the two interfaces which can be applied on audio codec design.

Table 16: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	3	DO	PCM clock	1.8 V power domain
PCM_SYNC	35	DO	PCM data frame sync	1.8 V power domain
PCM_DIN	2	DI	PCM data input	1.8 V power domain
PCM_DOUT	34	DO	PCM data output	1.8 V power domain
I2C_SCL	37	OD	I2C serial clock (for external codec)	Require external pull-up to 1.8 V
I2C_SDA	5	OD	I2C serial data (for external codec)	Require external pull-up to 1.8 V

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

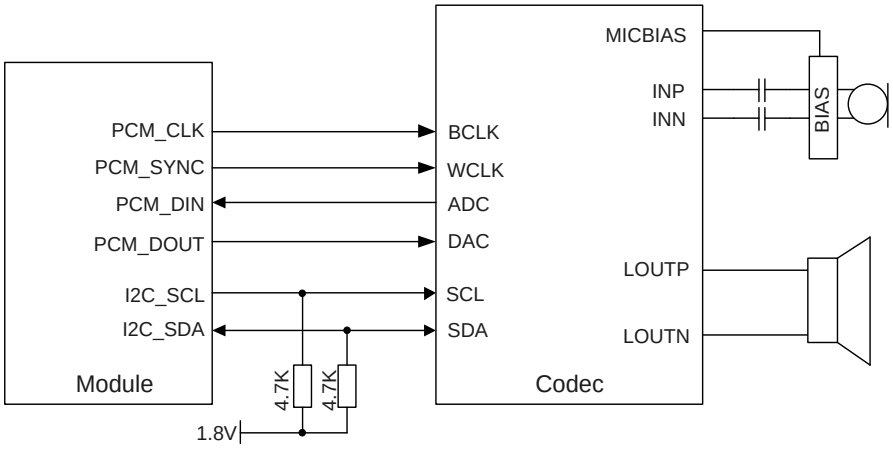


Figure 19: Reference Circuit of PCM Application with Audio Codec

NOTE

"*" means under development.

3.13. Network Status Indication

BG77 provides one network status indication pin: NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 17: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	79	DO	Module network activity status indication	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.

Table 18: Working State of NET_STATUS

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

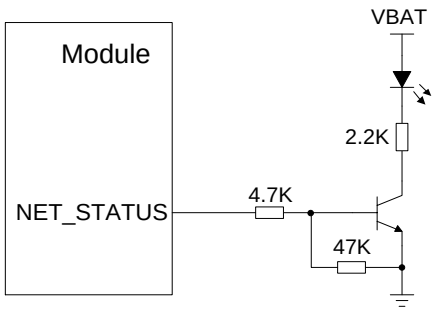


Figure 20: Reference Design of the Network Status Indicator

NOTES

NET_STATUS is a BOOT_CONFIG pin. It should not be pulled up before startup.

3.14. STATUS

The STATUS pin is used to indicate the operation status of BG77. It will output high level when the module is powered on.

The following table describes the pin definition of STATUS.

Table 19: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	78	DO	Module operation status indication	1.8 V power domain

The following figure shows a reference circuit of STATUS.

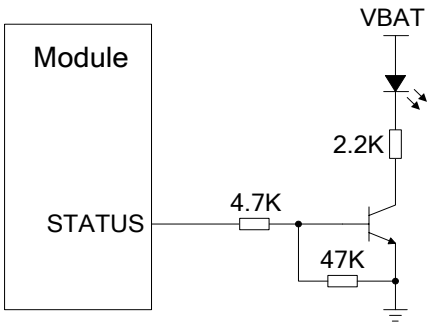


Figure 21: Reference Design of STATUS

3.15. Behaviors of MAIN_RI

AT+QCFG="risignaltype","physical" command can be used to configure MAIN_RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of MAIN_RI pin.

The default behaviors of MAIN_RI are shown as below.

Table 20: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps in high level.
URC	MAIN_RI outputs 120 ms low pulse when new URC returns.

The default MAIN_RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"** command. For more details about **AT+QCFG***, please refer to ***document [2]***.

NOTES

1. URC can be outputted from UART port, USB AT port and USB modem port, through configuration via **AT+QURCCFG** command. The default port is USB AT port.
2. "*" means under development.

3.16. USB_BOOT Interface

BG77 provides a USB_BOOT pin. During development or factory production, USB_BOOT can force the module to boot from USB port for firmware upgrade.

Table 21: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	87	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

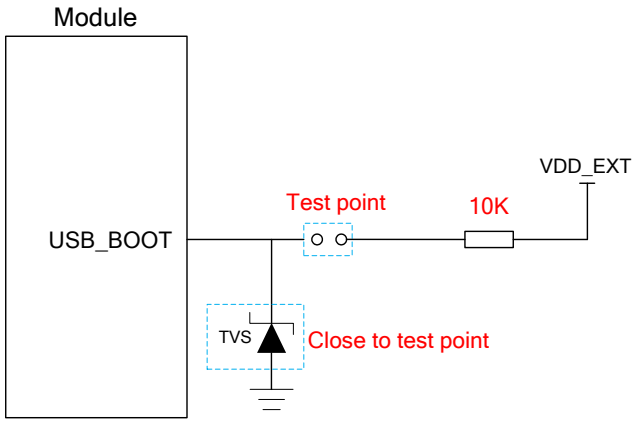


Figure 22: Reference Design of USB_BOOT Interface

The following figure shows the timing of USB_BOOT.

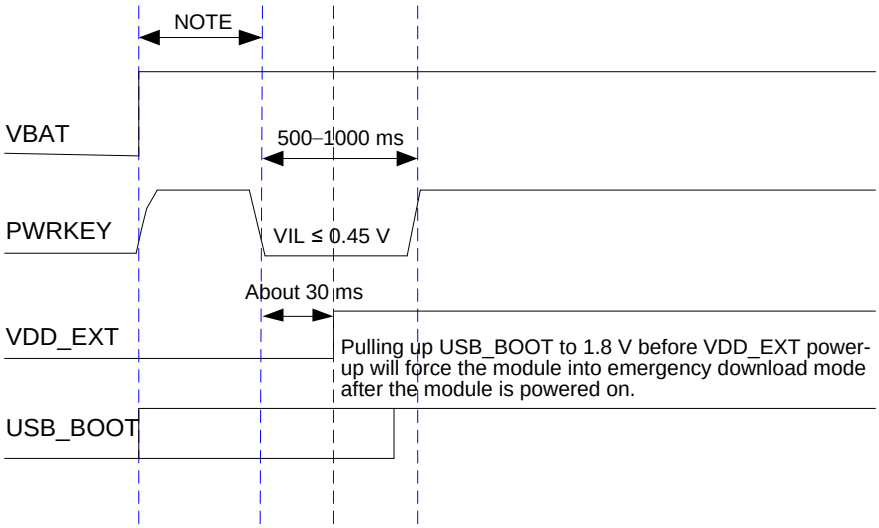


Figure 23: Timing of Turning on Module with USB_BOOT

NOTES

1. It is recommended to reserve the above circuit design during application design.
2. Please make sure that VBAT is stable before pulling down PWRKEY. It is recommended that the time between powering up VBAT and pulling down PWRKEY is no less than 30ms.
3. When using MCU to control the module entering emergency download mode, please follow the above timing sequence. Connecting the test points as shown in ***Figure 22*** can manually force the module to enter download mode.

3.17. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about the AT command, please refer to ***document [2]***.

In order to improve the accuracy of ADC voltage values, the trace of ADC should be ground surrounded.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description
ADC0	17	AI	General-purpose ADC interface
ADC1	18	AI	General-purpose ADC interface

The following table describes the characteristics of ADC interfaces.

Table 23: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0.1		1.8	V
Resolution (LSB)		64.979		μV
Analog Bandwidth		500		kHz
Sample Clock		4.8		MHz
Input Resistance	10			MΩ

NOTES

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1%.

3.18. GPIO Interfaces*

The module provides seven general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"*** command can be used to configure the status of GPIO pins. For more details about the AT command, please refer to ***document [2]***.

Table 24: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	Description
GPIO1	1	General-purpose input/output
GPIO2	8	General-purpose input/output
GPIO3	9	General-purpose input/output
GPIO4	33	General-purpose input/output
GPIO5	40	General-purpose input/output
GPIO6	57	General-purpose input/output
GPIO7	63	General-purpose input/output

The following table describes the characteristics of GPIO interfaces.

Table 25: Logic Levels of GPIO Interfaces

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

NOTES

1. GPIO5 (pin 40) is a BOOT_CONFIG pin. It should not be pulled up before startup.
2. "*" means under development.

3.19. GRFC Interfaces*

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 26: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	Description	Comments
GRFC1	83	Generic RF controller	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.
GRFC2	94	Generic RF controller	1.8 V power domain.

Table 27: Logic Levels of GRFC Interfaces

Parameter	Min.	Max.	Unit
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

Table 28: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	880–2200	B1, B2, B3, B4, B8, B25, B66
Low	High	791–894	B5, B18, B19, B20, B26, B27
High	Low	698–803	B12, B13, B14, B28, B85*
High	High	617–698	B71

NOTES

1. GRFC1 (pin 83) is a BOOT_CONFIG pin. It should not be pulled up before startup.
2. "*" means under development.

4 GNSS Receiver

4.1. General Description

BG77 includes a fully integrated global navigation satellite system solution that supports Gen9 VT of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

The module supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, BG77 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows the GNSS performance of BG77.

Table 29: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	TBD	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
	Warm start @open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s

	Hot start @open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between GNSS antenna and main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG77 includes a main antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna interface is shown below.

Table 30: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	26	IO	Main antenna interface	50 Ω characteristic impedance

5.1.2. Operating Frequency

Table 31: BG77 Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz

LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B14 [1)]	788–798	758–768	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B27 [1)]	807–824	852–869	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz
LTE-FDD B71 [2)]	663–698	617–652	MHz
LTE-FDD B85*	698–716	728–746	MHz

NOTES

1. [1)] LTE-FDD B14 and B27 are supported by Cat M1 only.
2. [2)] LTE-FDD B71 is supported by Cat NB2 only.
3. "*" means under development.

5.1.3. Reference Design of Main Antenna Interface

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

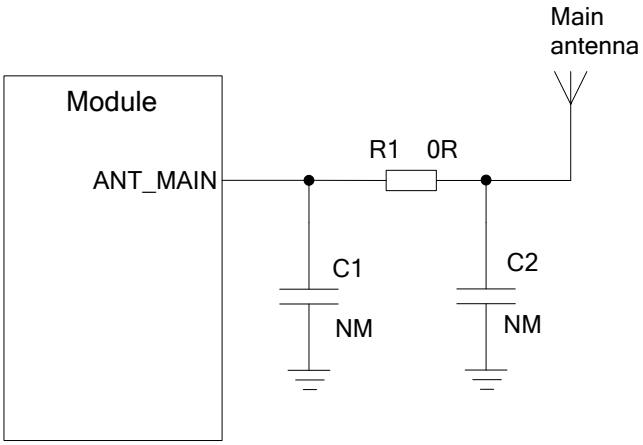


Figure 24: Reference Design of Main Antenna Interface

5.1.4. Reference Design of RF Layout

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

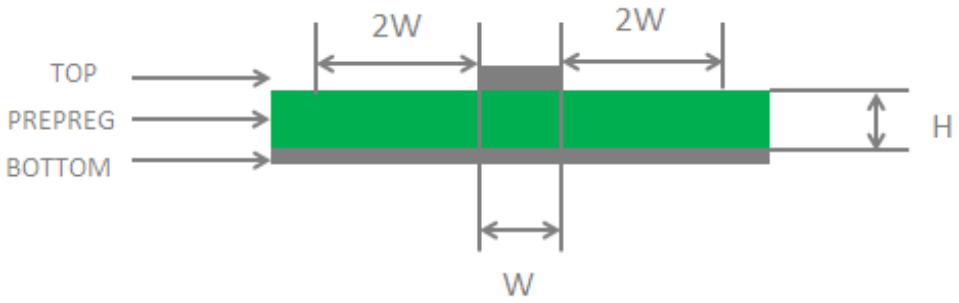


Figure 25: Microstrip Design on a 2-layer PCB

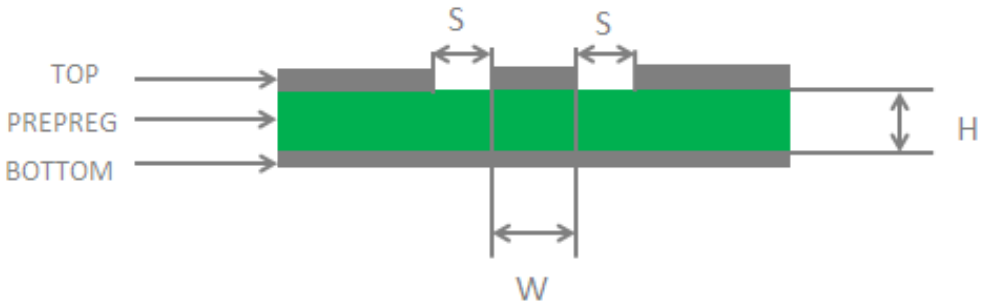


Figure 26: Coplanar Waveguide Design on a 2-layer PCB

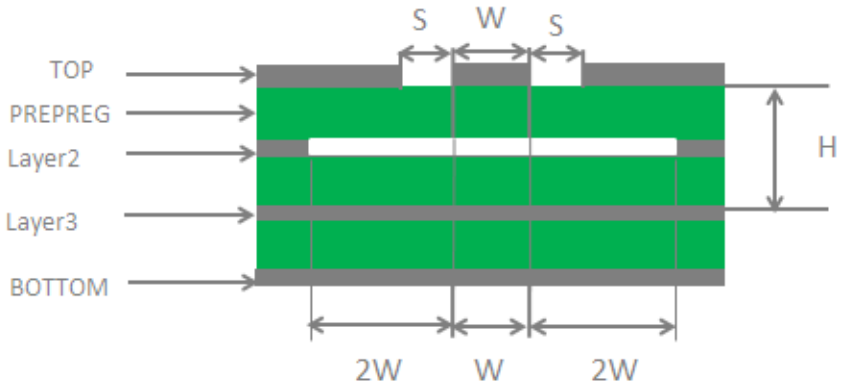


Figure 27: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

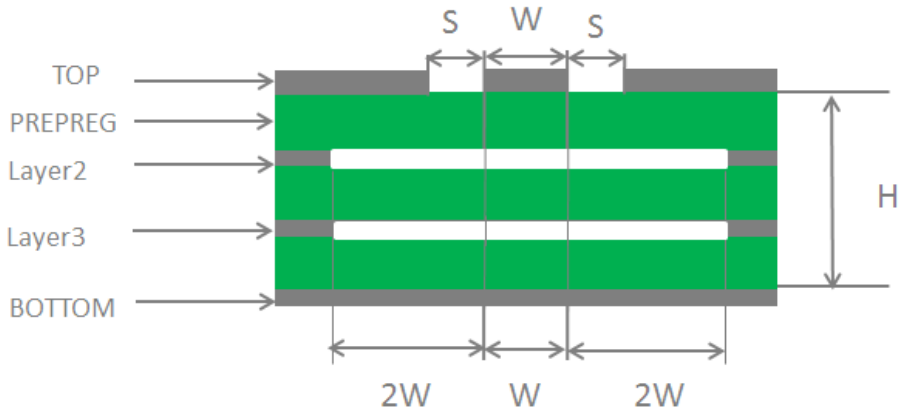


Figure 28: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 × W).

For more details about RF layout, please refer to ***document [4]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	32	AI	GNSS antenna interface	50 Ω impedance

Table 33: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou	1561.098 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

A reference design of GNSS antenna interface is shown as below.

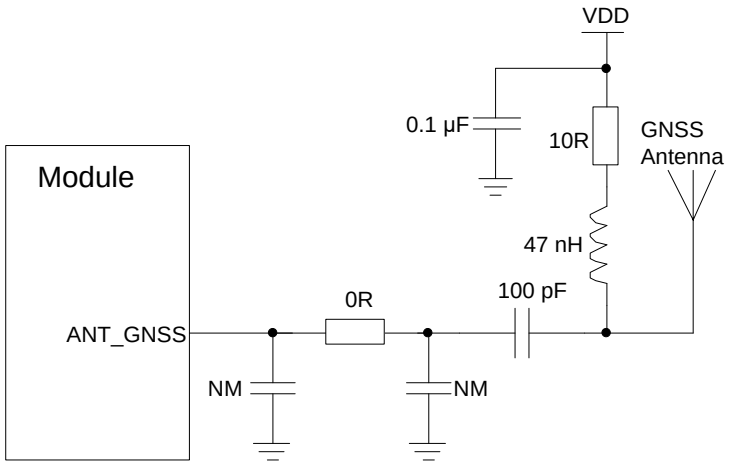


Figure 29: Reference Circuit of GNSS Antenna Interface

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on main antenna and GNSS antenna.

Table 34: Antenna Requirements

Antenna Type	Requirements
GNSS [1)]	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
LTE	VSWR: ≤ 2 Efficiency: > 30% Max Input Power (W): 50 Input Impedance (Ω): 50

	Cable Insertion Loss: < 1 dB (LTE B5/B8/B12/B13/B14/B18/B19/B20/B26/B27/B28/B71/B85) Cable Insertion Loss: < 1.5 dB (LTE B1/B2/B3/B4/B25/B66)

NOTES

1. [1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.
2. "*" means under development.

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by *HIROSE*.

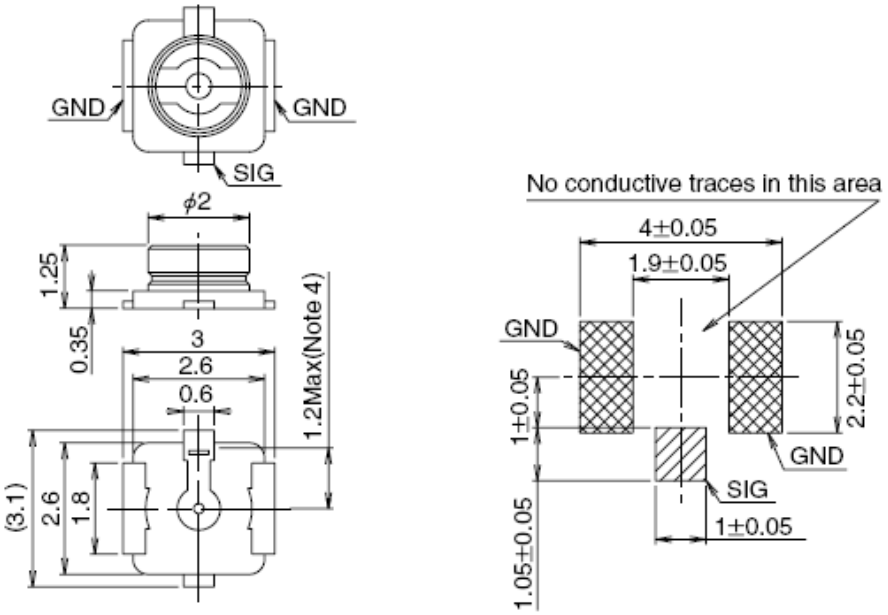


Figure 30: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

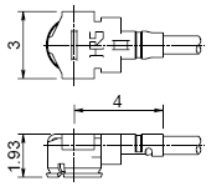
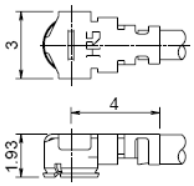
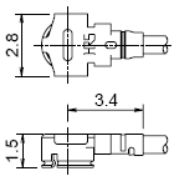
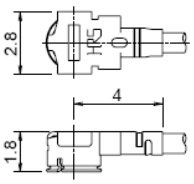
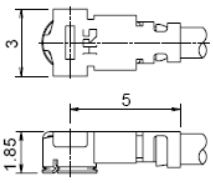
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 31: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

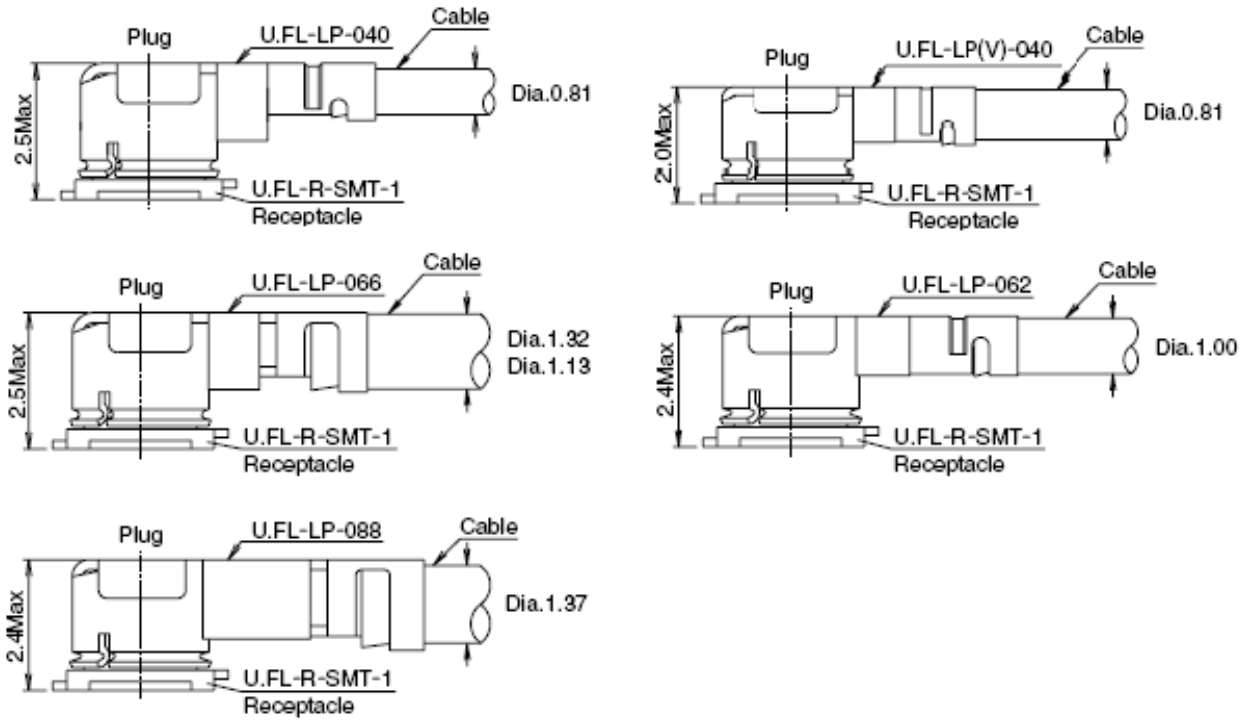


Figure 32: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6.0	V
USB_VBUS	1.3	1.8	V
Voltage at Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT [1)]	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	2.6	3.3	4.8	V
USBPHY_3P3	Power for USB PHY circuit			3.3		V
USB_VBUS	USB detection		1.3		1.8	V

NOTE

[1] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. In order to ensure full-function mode, the minimum power supply voltage should be higher than 2.8 V.

6.3. Operation and Storage Temperatures

The operation and storage temperatures of the module are listed in the following table.

Table 37: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1]	-35	+25	+75	ºC
Extended Temperature Range [2]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the normal operation temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The following table shows current consumption of BG77.

Table 38: BG77 Current Consumption

Parameter	Description	Conditions	Avg.	Max.	Unit
I_{VBAT}	Leakage	Power-off @ USB/UART disconnected	13		μA
	PSM	PSM @ USB/UART disconnected	3.2		μA
	Rock Bottom	**AT+CFUN=0** @ Sleep mode	0.6		mA
	Sleep Mode (USB disconnected)	DRX = 1.28 s @ LTE Cat M1	1.63	118	mA
		DRX = 1.28 s @ LTE Cat NB1	1.5	85	mA
		e-I-DRX = 81.92 s @ LTE Cat M1	0.76	118	mA
		e-I-DRX = 81.92 s @ LTE Cat NB1	0.79	90	mA
	Idle State	DRX = 1.28 s @ LTE Cat M1	TBD	TBD	mA
		DRX = 1.28 s @ LTE Cat NB1	TBD	TBD	mA
		e-I-DRX = 81.92 s @ LTE Cat M1	TBD	TBD	mA
		e-I-DRX = 81.92 s @ LTE Cat NB1	TBD	TBD	mA
	LTE Cat M1 data transfer (GNSS OFF)	LTE-FDD B1 @ 21.13 dBm	199	441	mA
		LTE-FDD B2 @ 21.22 dBm	198	434	mA
		LTE-FDD B3 @ 20.97 dBm	205	455	mA
		LTE-FDD B4 @ 21.08 dBm	203	444	mA
		LTE-FDD B5 @ 21.14 dBm	225	520	mA
		LTE-FDD B8 @ 21.34 dBm	223	514	mA
		LTE-FDD B12 @ 21.1 dBm	196	418	mA
		LTE-FDD B13 @ 20.94 dBm	228	522	mA
		LTE-FDD B14 @ 20.49 dBm	210	457	mA
		LTE-FDD B18 @ 21.24 dBm	223	512	mA
		LTE-FDD B19 @ 21.46 dBm	223	510	mA
		LTE-FDD B20 @ 21.13 dBm	228	526	mA

	LTE-FDD B25 @ 21.28 dBm	203	449	mA
	LTE-FDD B26 @ 20.86 dBm	226	527	mA
	LTE-FDD B27 @ 21.16 dBm	216	492	mA
	LTE-FDD B28A @ 20.99 dBm	200	434	mA
	LTE-FDD B28B @ 20.99 dBm	207	454	mA
	LTE-FDD B66 @ 20.98 dBm	204	447	mA
	LTE-FDD B85* @ 21.05 dBm	TBD	TBD	mA
LTE Cat NB2 data transfer (GNSS OFF)	LTE-FDD B1 @ 21.02 dBm	133	329	mA
	LTE-FDD B2 @ 21.03 dBm	137	350	mA
	LTE-FDD B3 @ 20.97 dBm	144	367	mA
	LTE-FDD B4 @ 21.08 dBm	142	360	mA
	LTE-FDD B5 @ 21.03 dBm	162	427	mA
	LTE-FDD B8 @ 21.09 dBm	158	405	mA
	LTE-FDD B12 @ 21.02 dBm	129	329	mA
	LTE-FDD B13 @ 20.11 dBm	165	427	mA
	LTE-FDD B18 @ 20.922 dBm	164	427	mA
	LTE-FDD B19 @ 21.02 dBm	160	417	mA
	LTE-FDD B20 @ 20.94 dBm	163	421	mA
	LTE-FDD B25 @ 21.01 dBm	140	356	mA
	LTE-FDD B26 @ 20.74 dBm	163	434	mA
	LTE-FDD B28 @ 20.98 dBm	149	378	mA
	LTE-FDD B66 @ 20.99 dBm	144	368	mA
	LTE-FDD B71 @ 21.13 dBm	131	330	mA
	LTE-FDD B85* @ 20.96 dBm	TBD	TBD	mA

6.5. RF Output Power

The following table shows the RF output power of BG77.

Table 39: BG77 RF Output Power

Frequency	Max.	Min.
LTE-FDD B1/B2/B3/B4/B5/B8/B12/B13/B14 [1]/B18/B19/B20/B25/ B26/B27 [2] /B28/B66/B71/B85*	21 dBm +1.7/-3dB	<-39 dBm

NOTES

1. [1] LTE-FDD B14 and B27 are supported by Cat M1 only.
2. [2] LTE-FDD B71 is supported by Cat NB2 only.
3. "*" means under development.

6.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of BG77.

Table 40: BG77 Conducted RF Receiving Sensitivity

Network	Band	Primary	Diversity	Sensitivity (dBm)	
				Cat M1/3GPP	Cat NB2 [1]/3GPP
LTE	LTE-FDD B1	Supported	Not Supported	-106.4/-102.3	-114/-107.5
	LTE-FDD B2			-106.4/-100.3	-114.5/-107.5
	LTE-FDD B3			-106/-99.3	-115/-107.5
	LTE-FDD B4			-106/-102.3	-114/-107.5
	LTE-FDD B5			-104/-100.8	-114/-107.5
	LTE-FDD B8			-107/-99.8	-115.5/-107.5
	LTE-FDD B12			-106/-99.3	-115/-107.5

LTE-FDD B13	-107/-99.3	-115/-107.5
LTE-FDD B14 2)	-107/-99.3	Not Supported
LTE-FDD B18	-107/-102.3	-115.5/-107.5
LTE-FDD B19	-107/-102.3	-115.5/-107.5
LTE-FDD B20	-107/-99.8	-115/-107.5
LTE-FDD B25	-107.5/-100.3	-114/-107.5
LTE-FDD B26	-107/-100.3	-115/-107.5
LTE-FDD B27 2)	-108/-100.8	Not Supported
LTE-FDD B28	-107/-100.8	-115/-107.5
LTE-FDD B66	-106/-101.8	-115/-107.5
LTE-FDD B71 3)	Not Supported	-114/-107.5
LTE-FDD B85*	TBD/-100	TBD/-107.5

NOTES

1. 1) LTE Cat NB2 receiving sensitivity without repetitions.
2. 2) LTE-FDD B14 and B27 are supported by Cat M1 only.
3. 3) LTE-FDD B71 is supported by Cat NB2 only.
4. "*" means under development.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of BG77 module.

Table 41: Electrostatic Discharge Characteristics (25 ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	kV
Main/GNSS Antenna Interfaces	±5	±10	kV

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Top and Side Dimensions

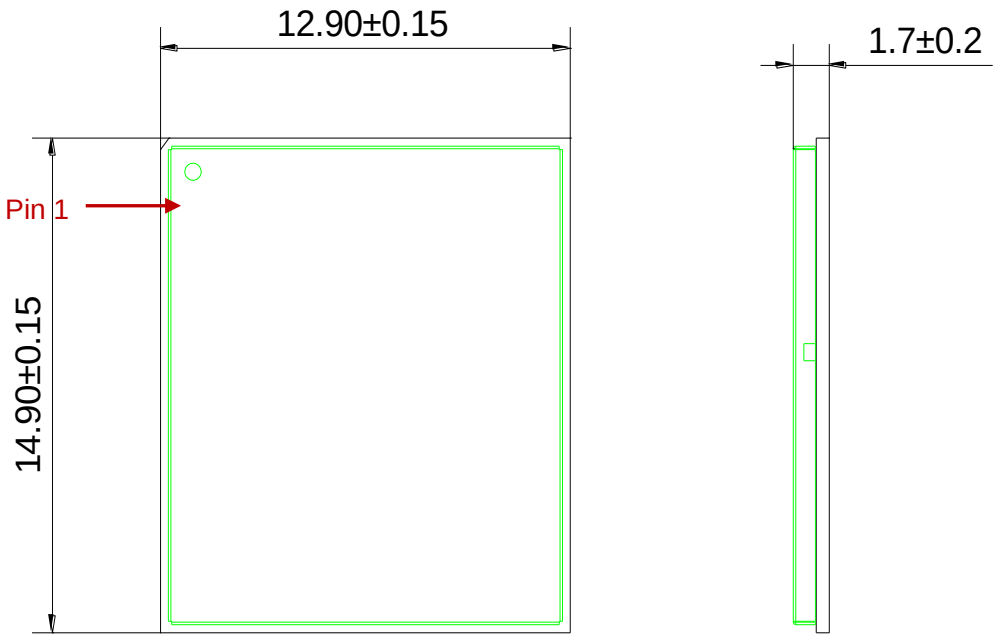


Figure 33: Module Top and Side Dimensions

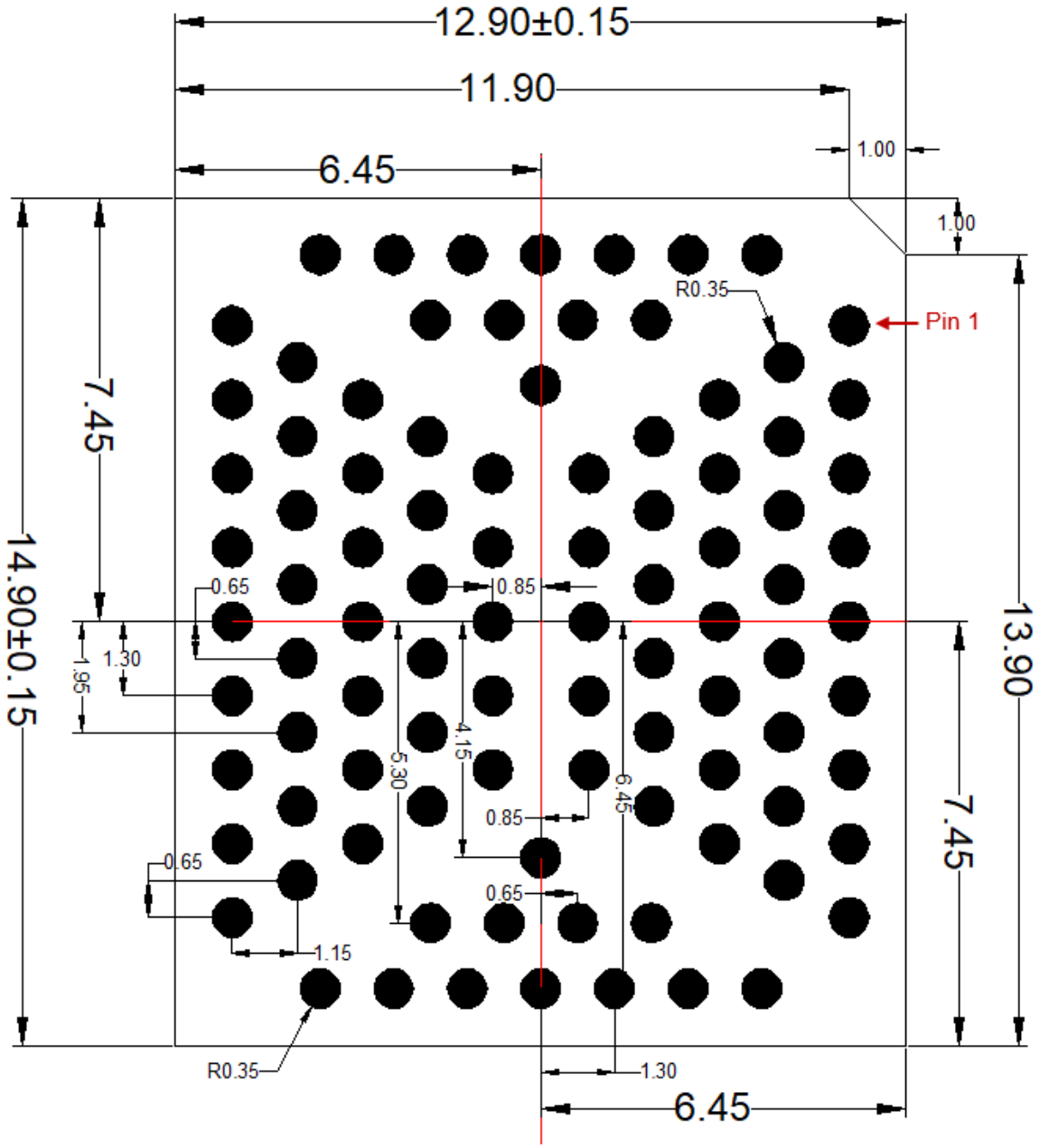


Figure 34: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

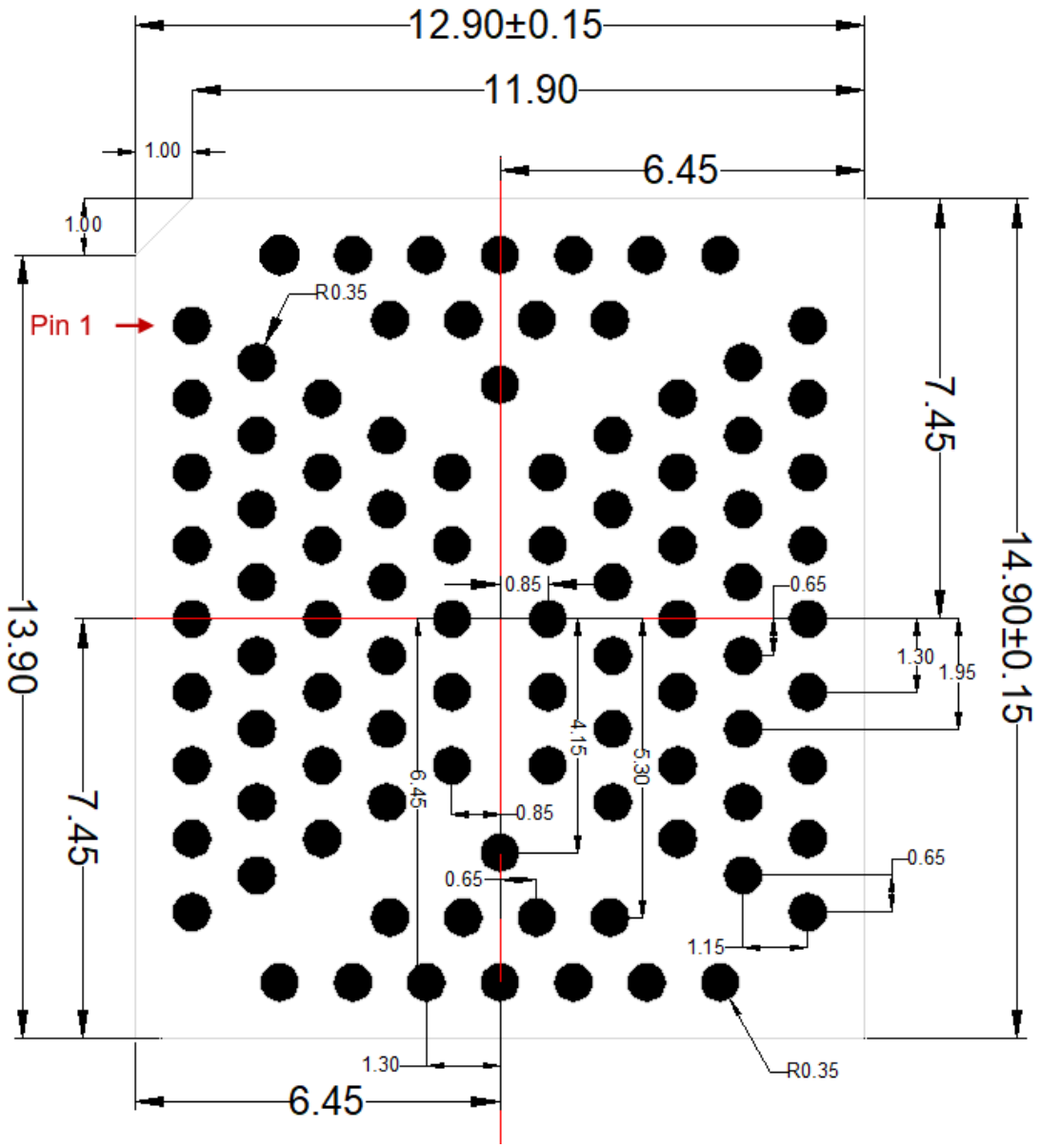


Figure 35: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, please keep about 3 mm between the module and other components on the motherboard.
2. All reserved pins must be kept open.
3. For stencil design requirements of the module, please refer to ***document [5]***.

7.3. Top and Bottom Views

Figure 36: Top View of the Module

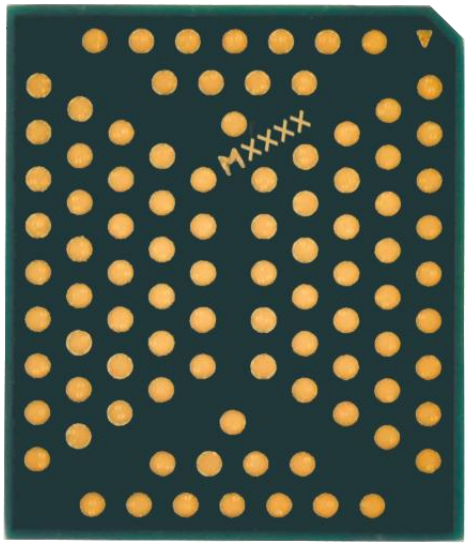


Figure 37: Bottom View of the Module

NOTE

These are renderings of BG77 module. For authentic appearance, please refer to the module that you receive from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

BG77 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below.

1. Shelf life in the vacuum-sealed bag: 12 months at < 40 ºC/90% RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤ 30 ºC/60% RH.
   - Stored at < 10% RH.
3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23 ±5 ºC and the humidity indication card shows the humidity is > 10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤ 30 ºC/60% RH.
4. If baking is required, devices may be baked for 8 hours at 120 ±5 ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120 ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly

so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, please refer to ***document [5]***.

It is suggested that the peak reflow temperature is 238–245 ºC, and the absolute maximum reflow temperature is 245 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

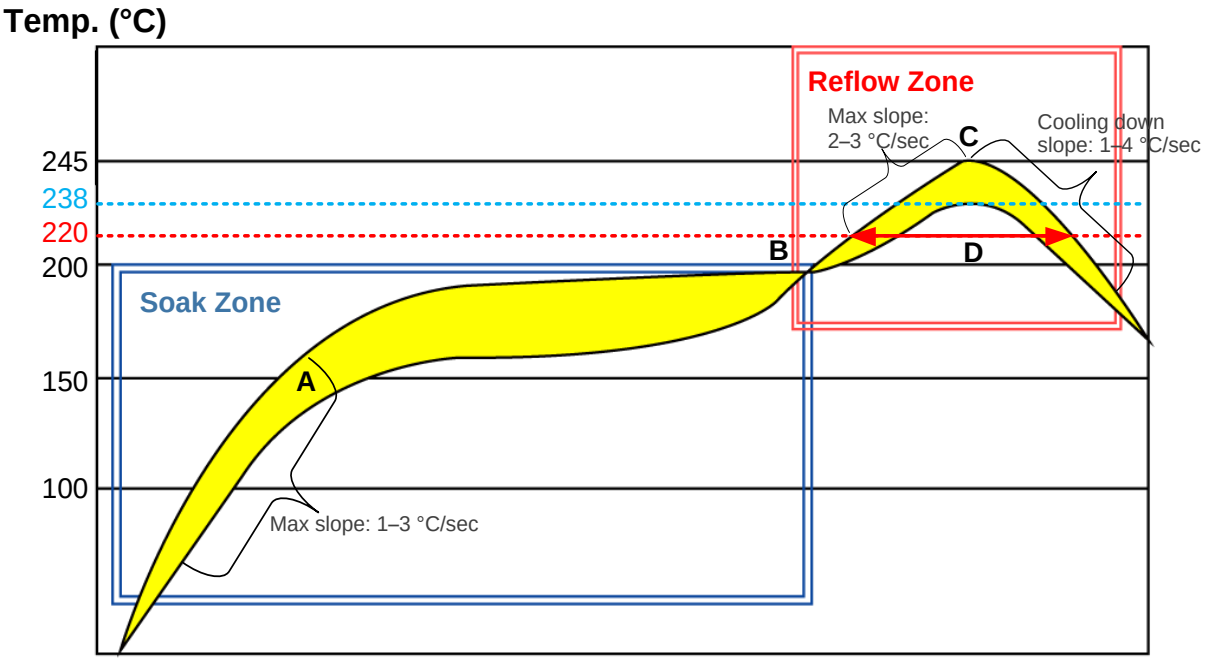


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 42: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3 °C/sec
Soak time (between A and B: 150 °C and 200 °C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3 °C/sec
Reflow time (D: over 220 °C)	40 to 60 sec

Max temperature	238 to 245 °C
Cooling down slope	1 to 4 °C/sec
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

BG77 is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The following figures show the packaging details, measured in millimeter (mm).

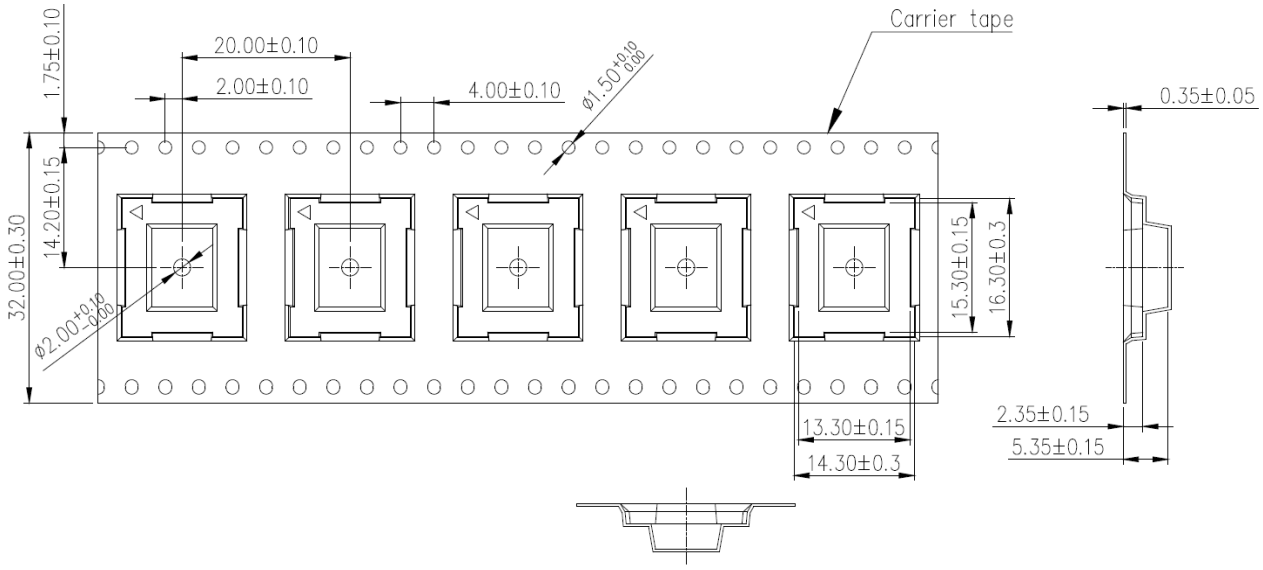


Figure 39: Tape Dimensions

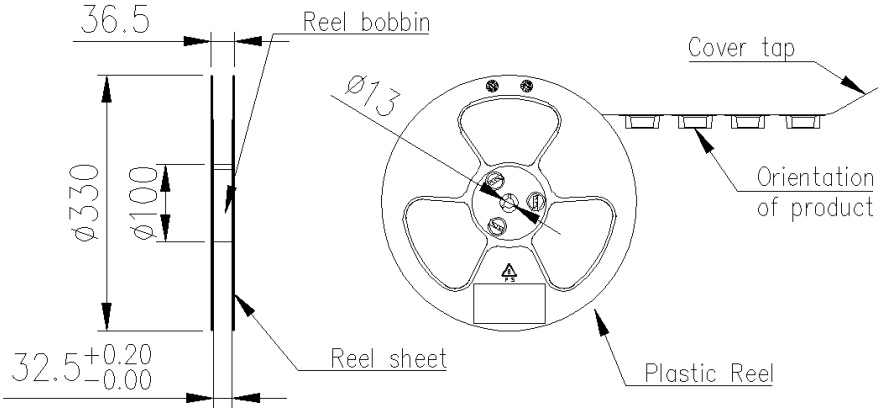


Figure 40: Reel Dimensions

Table 43: BG77 Packaging Specifications

Model Name	MOQ for MP	Minimum Package: 500	Minimum Package x 4 = 2000
BG77	500 pcs	Size: 370 mm × 350 mm × 56 mm N.W: TBD G.W: TBD	Size: 380 mm × 250 mm × 365 mm N.W: TBD G.W: TBD

9 Appendix A References

Table 44: Related Documents

SN	Document Name	Remark
[1]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB User Guide
[2]	Quectel_BG95&BG77_AT_Commands_Manual	BG95/BG77 AT Commands Manual
[3]	Quectel_BG95&BG77_GNSS_Application_Note	BG95/BG77 GNSS Application Note
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 45: Terms and Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
EGSM	Extended GSM (Global System for Mobile Communications)
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge

FDD	Frequency Division Duplex
HSS	Home Subscriber Server
I/O	Input/Output
Inorm	Normal Current
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MO	Mobile Originated
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RTS	Request to Send
SMS	Short Message Service
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value

V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

10 Appendix B Compulsory Certifications

By the issue date of the document, BG77 has been certified by JATE and TELEC.

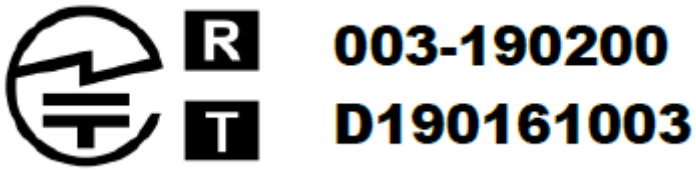


Figure 41: JATE/TELEC Certification ID