NOVATEK
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Data Sheet

NT35510

One-chip Driver IC with internal GRAM
for 16.7M colors 480RGB x 864 a-Si TFT LCD
with CPU / RGB / MIPI / MDDI Interface
or without internal CGRAM
for 16.7M colors 480RGB x 1024 a-Si TFT LCD
with RGB Interface

V0.05

Preliminary

REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/02/12
0.01	- Page 9, remove 320RGB x 480 - Page 10, Features, remove 320RGB x 480 and MUX description VGHO VGLO for gate control signals, remove VDDIM/VSSIM - Page11, update power voltage range - Page12, Block diagram - Page 13 to 22 : Add : VDD_DET,DIOPWR,PSWAP,DSWAP ,VGHO,VGLO,VRGH, VREFCP,CSP,CSN,LVGL,C61P,C61N,VRGH, VREF,GOUT, Remove : VDDIM/VSSIM, VDDEL Update : MVDDL,VGL,VGH,Test pins - Page23, update IF table - Page 51 to 66 : update SPI,IM3= 1 setting in figure - Page102,103, change DSIM, DSIG bit Reg to 0xB100 - Page115,124 Add WRPFD 50h on table - Page201,modified to 480x864 memory - Page202,Remove 320x480 - Page204, update whole Frame memory table - Page205, TE map to 480 lines, DOPCTR change to B100h - Page207, tvdl TBD - Page225,226,update VDD in figure - Page227,Modes to 7 - Page232,Sout update to Gout - Page235,Add chip attachment Detection section - Page237, update Gamma Structure - Page255,270,update FOSC, Example - Page266,update KB_CLED - Page272, Add inversion section - Page273,274, Power Architecture - Page275, update DIOPWR,VREFCP,VGMP1,VGLO - Page276,updateC61P/N,LVGL,VGLO,VRGH,VREFCP,DIOPWR, VGMP1/2,VGMN,VGSP,VGSN, - Page291, change name to RAMKP - Page306 to 312,remove 320x 480 resolution setting - Page337, 5400h Cmd add A and G bit - Page385, Absolute Max Rating for MV HV, remove VDDIM - Page386, VDDIM remove - Page387, Vdev value modified - Page402,403, Remove MVDDI in note - Page406, Remove 320 x 480, update 360x640 Sout sequence - Page173 to 181,MDDI windowless packet - Page377,379, A1,A8 cmd update - Page387 to 396, VDDI to 3.3V - Page362 to 376 70h to 7Eh cmd default value - Page28,29,30,40,41,42 MPU figure update - Page 12,274 Block and power architecture update	Kevin	SW	Dennis	2010/03/17

0.02	- Page 10,remove 360RGB x 640, Add 480RGBx720 - Page 11, update GPO[3:0] - Page 12, update VGHO, VGLO - Page 13, update Block Diagram - Page 18, update IM, GPO, VSEL, and EXB1T - Page 20, update VGLO,LVGL - Page 21, update VGLX,VGL_REG, Remove CP6_P/N - Page 23, update VDD_BC - Page 24, update CONTACT1~4, VSSIDUM - Page 25, update IF description table - Page 207, update Address Counter - Page 235, update Resolution Data - Page 252, remove CLED_VOL - Page 271, remove KB_CLED_VOL - Page 277, add 4 dot inversion - Page 306,308,313,326 resolution update, remove nHD, add 480x720 - Page 384, update absolute voltage - Page 385, update DC spec - Page 386, update Note3,Note5 - Page 405, update resolution - Page 406, update Alignment Mark	Kevin	SW	Dennis	2010/04/06
0.03	- Page 10,11,205,206,234,305,307,312,325,404, update resolution - Page 13, update Block diagram - Page 17-24, update pin description(MDDI not support DSWAP, Update TE_R,TE_L, DSTB_SEL, RESX,VSEL,VREF_PWR, I2C_SDA remove VDD_BD, ENDIOV) - Page 104,121, remove generic data type 0x24 - Page 134, update EoTP Option - Page 175, update MDDI support type - Page 176,177, update sub frame header, link shut down packet - Page 179,180, update skew calibration packet, client capability packet - Page 184, update packet type is 20 - Page 209,214, update TE off,output is low, tering effect bus trigger - Page 241, update gamma to 10 bits setting - Page 276, update 3-dots inversion - Page 384, update VIH,VIL,VOH,VOL - Page 388, update hibernation wake up - Page 390,392 update Note2 - Remove pad chapter to application note	Kevin	SW	Dennis	2010/05/18

0.04	- Page 14, update Block diagram of RGBBP - Page 16, update WRX/SCL/I2C_SCL, SDI/I2C_SDA - Page 19~25, update IM3 pin description,RGBBP(remove I2C_SA1) OSC_Test description, KBBC to test pin - Page 21, update VREF_PWR description - Page 26, update IM table - Page 42~44, update MPU read scription - Page 49~52, update SPI+RGB or SPI+MDDI description - Page 60, update I2C Address - Page 181,182, update 16 bit SPI pause description - Page 187~189, update RGB figure - Page 200, update TE waveform in RGB mode 2 - Page 237, MTP sequence - Page 238~258, update one dimming control for LABC & CABC, remove KBBC function description - Page 260,update 0x04 Cmd, remove KBBC Cmd - Page 262, update 0xA1,0xA8 Cmd - Remove all the KBBC related function, register	Kevin	SW	Dennis	2010/07/27
0.05	- Page 11, 12, 190, 191, 219, 284~287, 291, 304, 376, remove 480RGBx360 - Page 15, update MTP_PWR application voltage - Page 16, update CSX, RDX, DC/X, SDI, SDO - Page 18, update DSWAP - Page 38 & 44, update typo for data format in table - Page 53, update read data 8-8-8-bit only in SPI - Page 183, 184, update note for min. porch of RGB interface - Page 232, update MTP sequence and MTP_PWR voltage - Page 235, 236, remove PWM_ENH_OE bit (keep x2) - Page 312, 314, update typo for BCTRL and BL - Page 371, 372: update figures - Page 373: update figure, add RGB+I2C - Page 374: update figures, IM setting - Page 375: update figures, IM setting	Kevin	SW	Dennis	2010/10/15

1 DESCRIPTION

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35510. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

The NT35510 device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640 with internal CGRAM and 480RGB x 1024 by pass internal CGRAM. It includes a 9,953,280 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit..

The NT35510 supports MDDI interface, MIPI Interface, 16/18/24 bits RGB interface, 8/16/24-bit system interfaces, serial peripheral interfaces (SPI) and I2C interface. The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area. The 480RGB x 1024 by pass CGRAM application is used for RGB interface only.

The NT35510 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 864-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

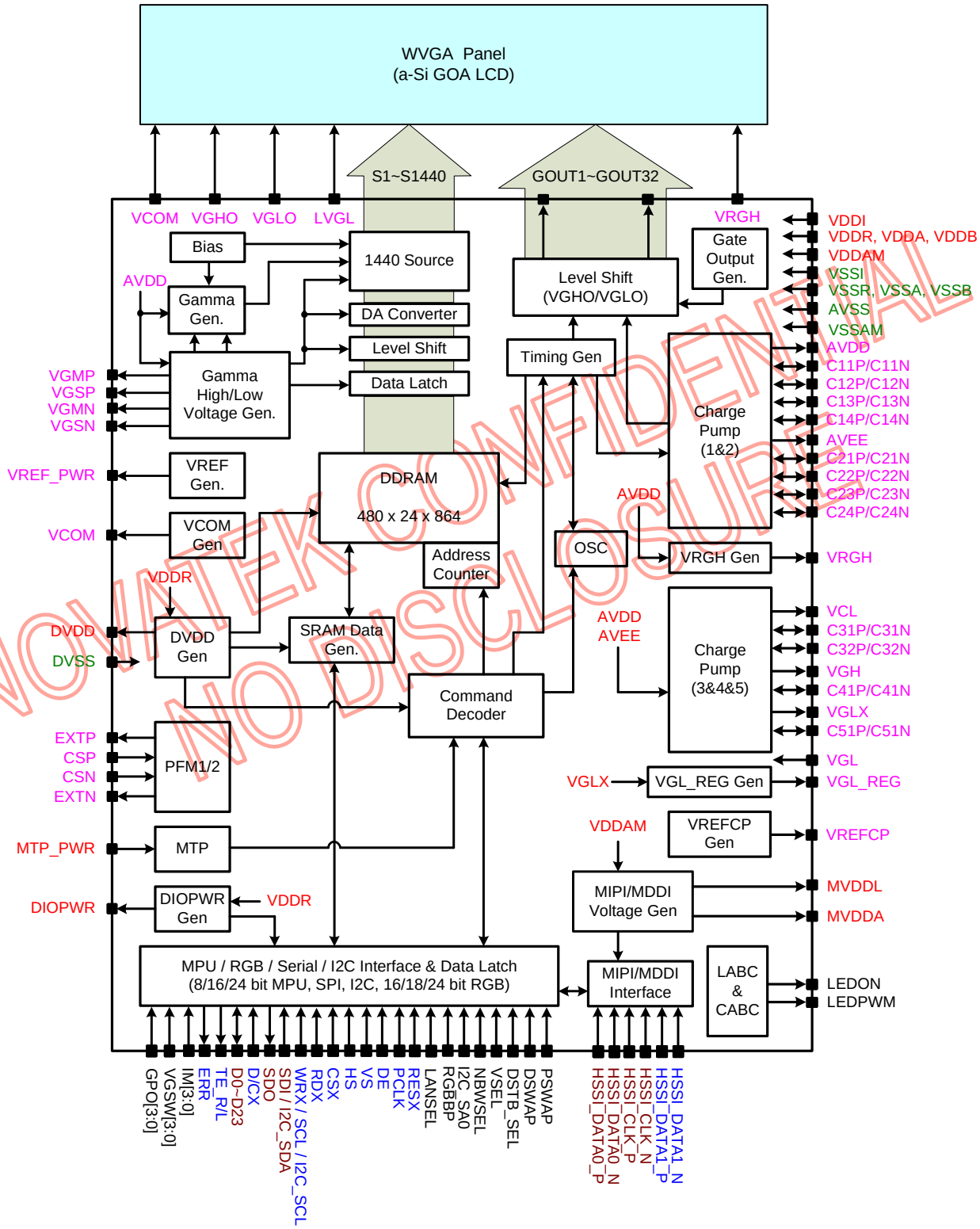
This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA..

2 FEATURES

- Single chip WVGA a-Si TFT LCD Controller/driver with Display RAM.
- Display resolution option
  - 480RGB x 1024 by pass GRAM
  - 480RGB x 864 with 480x24-bitsx 864 GRAM
  - 480RGB x 854 with 480x24-bitsx 854 GRAM
  - 480RGB x 800 with 480x24-bitsx 800 GRAM
  - 480RGB x 720 with 480x24-bitsx 720 GRAM
  - 480RGB x 640 with 480x24-bitsx 640 GRAM
- Display data RAM (frame memory): 480 x 864 x 24-bits = 9,953,280 bits
- Display mode (Color mode)
  - Full color mode: 16.7M-colors
  - Reduce color mode: 262K colors
  - Reduce color mode: 65K colors
  - Idle mode: 8-colors
- Interface
  - 8-/16-/24-bits 80-series MPU interface
  - 16-bit serial peripheral interface
  - I2C interface
  - 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
  - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
  - Mobile Display Digital Interface (MDDI V1.2, 1 strobe and 1 or 2 data lane pairs)
- Display features
  - Window address functions for specifying a rectangular area on the internal RAM to write data
  - Individual gamma correction setting for RGB dots
  - Deep standby function
- On chip
  - VGHO/VGLO voltage generator for gate control signal and panel
  - Oscillator for display clock
  - Supports gate control signals to gate driver in the panel
  - On module color characteristics
  - On module checksums checking
  - Four GPO (General Purpose Output) pins for external control
- Supply voltage range
  - I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.3V (VDDI) or 1.1 ~ 1.3V (VDDIL)
  - Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.3V ~ 4.8V
  - MIPI/MDDI regulator supply voltage range for VDDAM to VSSAM: 2.3V ~ 4.8V

◆ Output voltage levels
- Positive gate driver voltage range for VGH: AVDD+VDDB ~ 2xAVDD - AVEE
- Negative gate driver voltage range for VGLX: AVEE+VCL ~ 2xAVEE-AVDD
- Step-up 1 output voltage range for AVDD: 4.5 ~ 6.5V
- Step-up 2 output voltage range for AVEE: -4.5 ~ -6.5V
- Positive gamma high voltage range for VGMP: 3.0 ~ 6.3V (AVDD-0.3V)
- Positive gamma low voltage range for VGSP: 0.0, 0.3 ~ 3.7V
- Negative gamma high voltage range for VGMN: -3.0 ~ -6.3V (AVEE+0.3V)
- Negative gamma low voltage range for VGSN: 0.0, -0.3 ~ -3.7V
- Common electrode voltage range for VCOM: 0.0 ~ -3.5V (VCL+0.3V)
- Panel voltage range for VRGH: 1.0V ~ 6.0V(AVDD-0.3V)

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1 Power Supply Pins

Symbol	Name	Description
VDDB	DC/DC Power	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	Analog Power	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	Regulator Power	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDD_DET	Detection Power	Connect to VDDB/VDDA/VDDR for detection.
VDDAM	MIPI Power	Power supply for MIPI/MDDI analog regulator system
VDDI	I/O Power	Power supply for interface system except MIPI/MDDI interface
DVDD	Digital Voltage	Regulator output for logic system power (1.5V typical) Connect a capacitor for stabilization.
DIOPWR	Dual I/O Voltage	Regulator output for dual I/O voltage system (1.2V/1.8V typical). Connect a capacitor for stabilization.
MVDDA	MIPI/MDDI Voltage	Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization. If not use MIPI/MDDI interface, please open this pin.
MVDDL	MIPI Voltage	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI interface, please open this pin
VSSB	DC/DC GND	System ground for DC/DC converter
VSSA	Analog GND	System ground for analog system
VSSR	Regulator GND	System ground for regulator system
VSSAM	MIPI GND	System ground for internal MIPI/MDDI analog system
VSSI	I/O GND	System ground for interface system except MIPI/MDDI interface
DVSS	Digital GND	System ground for internal digital system
AVSS	Source OP GND	System ground for source OP system.
MTP_PWR	MTP Power	MTP programming power supply pin (7.5 to 8.0V and 7.75V typical) Must be left open or connected to DVSS in normal condition.

4.2 80-System Interface Pins

Symbol	I/O	Description
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	WRX: Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
RDX	I	Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface. This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D/CX	I	Display data / command selection in 80-series MPU I/F. D/CX = ”0” : Command D/CX = ”1” : Display data or Parameter This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 24-bit interface: D[23:0] are used These pins are not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: “1” = VDDI level, “0” = VSSI level.

4.3 SPI /I2C Interface Pins

Symbol	I/O	Description
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
SDI / I2C_SDA	I/O	SCL: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU, I2C, MIPI or MDDI I/F, please open this pin.

NOTE: “1” = VDDI level, “0” = VSSI level.

4.4 RGB Interface Pins

Symbol	I/O	Description
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
DE	I	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F.. For RGB I/F: 16-bit/pixel: D[20:16]=R[4:0], D[13:8]=G[5:0] and D[4:0]=B[4:0], connect unused pins to VSSI 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSSI 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0] These pins are not used for MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: "1" = VDDI level, "0" = VSSI level.

4.5 MIPI/MDDI Interface Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>HSSI_CLK_P
HSSI_CLK_N</td><td>I</td><td>-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.
-These pins are MDDI_STB_P/M differential strobe signals if MDDI interface is used.
-HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D0_P
HSSI_D0_N</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals if MIPI interface is used.
-These pins are MDDI_DATA0_P/M differential strobe signals if MDDI interface is used.
-HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P
HSSI_D1_N</td><td>I</td><td>-These pins are DSI-D1+/- differential data signals if MIPI interface is used.
-These pins are MDDI_DATA1_P/M differential strobe signals if MDDI interface is used.
-HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>ERR</td><td>O</td><td>CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated.
When this pin is activated, it output high if CRC/ECC error found.
If not used, please open this pin.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface.
<table>
<tr><th>LANSEL</th><th>Data Lane of MIPI/MDDI</th></tr>
<tr><td>0</td><td>1 data lane</td></tr>
<tr><td>1</td><td>2 data lanes</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.
For MIPI interface, both DSWAP and PSWAP function are available.
For MDDI interface, only PSWAP function is available. Please connect DSWAP pin to VSSI.
<table>
<tr><th colspan="2">Pin Name</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th></tr>
<tr><td rowspan="4">Input MIPI Signal</td><td>DSWAP=0
PSWAP=0</td><td>DSI-D0+</td><td>DSI-D0-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D1+</td><td>DSI-D1-</td></tr>
<tr><td>DSWAP=0
PSWAP=1</td><td>DSI-D0-</td><td>DSI-D0+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D1-</td><td>DSI-D1+</td></tr>
<tr><td>DSWAP=1
PSWAP=0</td><td>DSI-D1+</td><td>DSI-D1-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D0+</td><td>DSI-D0-</td></tr>
<tr><td>DSWAP=1
PSWAP=1</td><td>DSI-D1-</td><td>DSI-D1+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D0-</td><td>DSI-D0+</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
</table>

4.6 Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESX</td><td>I</td><td>
This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.
The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.
<table>
<tr><th colspan="2">Input Voltage Level (DSTB_SEL="0")</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td rowspan="2">VDDI=1.65~3.3V</td><td>Logic High level input voltage</td><td>0.7xVDDI</td><td>VDDI</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td><td>V</td></tr>
<tr><td rowspan="2">VDDI=1.1~1.3V</td><td>Logic High level input voltage</td><td>0.88</td><td>1.35</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
<table>
<tr><th colspan="2" rowspan="2">Input Voltage Level (DSTB_SEL="1")</th><th colspan="2">VDDI=1.65~3.3V</th><th colspan="2">VDDIL=1.1~1.3V</th><th rowspan="2">Unit</th></tr>
<tr><th>Min.</th><th>Max.</th><th>Min.</th><th>Max.</th></tr>
<tr><td rowspan="2">VSEL =High</td><td>Logic High level input voltage</td><td>0.7xVDDI</td><td>VDDI</td><td>1.155</td><td>1.95</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td><td>VSSI</td><td>0.585</td><td>V</td></tr>
<tr><td rowspan="2">VSEL =Low</td><td>Logic High level input voltage</td><td>0.88</td><td>1.35V</td><td>0.88</td><td>1.35V</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>TE
(TE_L)</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is output low.
If not used, please open this pin.</td></tr>
<tr><td>TE_R</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
The same output signal as TE (TE_L) pin.
If not used, please open this pin.</td></tr>
<tr><td>IM[3:0]</td><td>I</td><td>
Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM[3:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>0000</td><td>80-series 8-bit MPU I/F, D[7:0]</td><td>80-series 8-bit MPU I/F, D[7:0]</td></tr>
<tr><td>0001</td><td>80-series 16-bit MPU I/F, D[15:0]</td><td>80-series 16-bit MPU I/F, D[15:0]</td></tr>
<tr><td>0010</td><td>80-series 24-bit MPU I/F, D[23:0]</td><td>80-series 24-bit MPU I/F, D[23:0]</td></tr>
<tr><td>0011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>1011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0100</td><td>RGB I/F, D[23:0]</td><td>I2C I/F, I2C_SDA</td></tr>
<tr><td>0101</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td></tr>
<tr><td>0110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>0110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0111</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
I2C I/F, I2C_SDA serial data</td></tr>
</table>
</td></tr>
<tr><td>RGBBP</td><td>I</td><td>Display data written path control in RGB interface.
RGBBP="0", display data written to frame memory.
RGBBP="1", display data written to line buffer (frame memory by pass mode)
When not used in other interfaces, please connect to VSSI.</td></tr>
</table>

<table>
<tr><td>I2C_SA0</td><td>I</td><td>Select the I2C interface address from MPU. If not used, please connect to VSSI.
<table>
<tr><th>I2C_SA0</th><th>Slave Address</th></tr>
<tr><td>0</td><td>10011 00</td></tr>
<tr><td>1</td><td>10011 01</td></tr>
</table></td></tr>
<tr><td>VSEL</td><td>I</td><td>Input pin to switch the I/O voltage.
This VSEL function only apply for RESX, TE, LEDPWM, LEDON, KBBC pins.
The VSEL dual IO function is valid when DSTB_SEL=”1”.
<table>
<tr><th rowspan="2">DSTB_SEL</th><th rowspan="2">VDDI</th><th rowspan="2">VSEL</th><th rowspan="2">DIOPWR</th><th colspan="2">Output Voltage Level</th></tr>
<tr><th>TE</th><th>LEDON
LEDPWM</th></tr>
<tr><td>0</td><td>1.65~3.3V
or
1.1~1.3V</td><td>X</td><td>Off</td><td>VOH=VDDI
VOL=VSSI</td><td>VOH=VDDI or VDDA
VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.65~3.3V</td><td>Low</td><td>1.2V</td><td>VOH=1.2V
VOL=VSSI</td><td>VOH=1.2V
VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8V</td><td>VOH=VDDI or DIOPWR
VOL=VSSI</td><td>VOH=VDDI or VDDA
VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.1~1.3V</td><td>Low</td><td>1.2V</td><td>VOH=1.2V
VOL=VSSI</td><td>VOH=1.2V
VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8V</td><td>VOH=1.8V
VOL=VSSI</td><td>VOH=1.8V
VOL=VSSI</td></tr>
</table>
The input voltage range for VSEL pin:
<table>
<tr><th>Input Voltage Level</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>Logic High level input voltage</td><td>0.88</td><td>VDDI</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
If not used, please connect to VDDI.</td></tr>
<tr><td>GPO[3:0]</td><td>O</td><td>General purpose output pins. The output voltage swing is VDDI to VSSI.
If not used, please open these pins.</td></tr>
<tr><td>VGSW[3:0]</td><td>I</td><td>Input pin to select the different application.</td></tr>
<tr><td>EXB1T</td><td>I</td><td>Input pin to select the external AVDD DC/DC voltage.
<table>
<tr><th>EXB1T</th><th>AVDD Voltage</th></tr>
<tr><td>0</td><td>Use internal DC/DC for AVDD</td></tr>
<tr><td>1</td><td>Use external DC/DC for AVDD</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>Input pin to select the voltage sequence of V0 ~ V255.
<table>
<tr><th>NBWSEL</th><th>V0 ~ V255 voltage sequence</th></tr>
<tr><td>0</td><td>$V_{(00h)}>V_{(01h)}>\ldots>V_{(FEh)}>V_{(FFh)}$ (Normally White)</td></tr>
<tr><td>1</td><td>$V_{(00h)}<V_{(01h)}<\ldots<V_{(FEh)}<V_{(FFh)}$ (Normally Black)</td></tr>
</table></td></tr>
<tr><td>DSTB_SEL</td><td>I</td><td>Input pin to control DIOPWR regulator on/off.
<table>
<tr><th>DSTB_SEL</th><th>DIOPWR Regulator</th><th>VSEL Function</th></tr>
<tr><td>0</td><td>DIOPWR Off</td><td>Invalid</td></tr>
<tr><td>1</td><td>DIOPWR On</td><td>Valid</td></tr>
</table></td></tr>
</table>

NOTE: “1” = VDDI level, “0” = VSSI level.

4.7 Driver Output Pins

Symbol	I/O	Description
S1 ~ S1440	O	Pixel electrode driving output.
GOUT1 ~ GOUT32	O	Gate control signals for panel. The swing voltage level is VGHO to VGLO
SDUM0~3	O	Dummy Source, leave it Open if not used
VGHO	O	High voltage level for gate control signals and gate circuit of panel.
VGLO	O	Low voltage level for gate control signals and gate circuit of panel.
LVGL	O	Low voltage level for gate circuit of panel.
VCOM	O	Regulator output for common voltage of panel. Connect a capacitor for stabilization.

4.8 DC/DC Converter Pins

Symbol	I/O	Description
AVDD	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGLX	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
VGL	I	Substrate voltage for driver IC. Please connect VGL to VGLX.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	O	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	O	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	O	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
VRGH	O	Output voltage generated from AVDD. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG	O	Output voltage generated from VGLX. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
EXTP	O	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device. When not in use, please open this pin.
EXTN	O	PFM2 control output for DC/DC converter to generate AVEE. Connect to gate of external PMOS device. When not in use, please open this pin.
CSP	I	Current sensing input for PFM1 DC/DC converter (generate AVDD). When not in use, please connect to VSSB.
CSN	I	Current sensing input for PFM2 DC/DC converter (generate AVEE). When not in use, please connect to VSSB.
VREF_PWR	O	Regulator output for power voltage. Connect a capacitor for stabilization.
VREFCP	O	Reference voltage for internal voltage generating circuit. Connect capacitor for stabilization.

Symbol	I/O	Description
VGMP	O	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	O	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN	O	Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN	O	Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

4.9 LABC and CABC Control Pins

Symbol	I/O	Description
LEDON	O	This pin is connect to the external LED driver. It is a LED driver control signal which is used for turning ON/OFF the LED backlight. If not used, please open this pin.
LEDPWM	O	This pin is connect to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.

4.10 Test Pins

Symbol	I/O	Description
PADA1 PADA2 PADA3 PADA4 PADB1 PADB2 PADB3 PADB4	I/O	- These test pins for chip attachment detection. PADA1 to PADA4 are output pins and PADB1 to PADB4 are input pins. - For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace. Connect PADA3 and PADB3 together by ITO trace. Connect PADA4 and PADB4 together by ITO trace.
CONTACT1A, CONTACT1B, CONTACT2A, CONTACT2B	I/O	- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B, CONTACT2A with CONTACT2B
AVSS_AVDD	I	Test pin, must be connected to AVSS
AVEE_AVSS	I	Test pin, must be connected to AVEE
VCL_VDDB	I	Test pin, must be connected to VCL
VCL_AVSS	I	Test pin, must be connected to VCL
VGMN_VGMP	I	Test pin, must be connected to VGMN
VGSN_VGSP	I	Test pin, must be connected to VGSN
KBBC	O	Test pin, not accessible to user. Must be left open.
TEST0~7	I/O	Test pin, not accessible to user. Must be left open.
OSC_TEST	I/O	Test pin, not accessible to user, Must left open
VDDI_OPT1~2	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSI_OPT1	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSIDUM0~106	O	-These pins are dummy with VSSI potential (not have any function inside). -Signal traces can't pass through on glass under these pads.

5 FUNCTIONAL DESCRIPTION

5.1 MPU Interface

NT35510 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in ***Table 5.1.1***

Table 5.1.1 Interface Type Selection

IM3	IM2	IM1	IM0	SRAM	Register
0	0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
0	0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
0	0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
0	1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA serial data
0	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
0	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL rising trigger
1	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL falling trigger
0	1	1	1	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N I2C interface, I2C_SDA serial data

Note: "X" = Don't care.

5.1.2 80-series MPU Interface

The MCU uses an 11-wires 8-data or 19-wires 16-data or 27-wires 24-data parallel interface.
The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[23:0] bits are display RAM data or command parameters. When D/C='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM3,IM2, IM1 and IM0.

The interface functions of 80-series parallel interface are given in ***Table 5.1.2.***

Table 5.1.2 Parallel interface function (80-Series)

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	0	0	0	8-bit Parallel	0	1	↑	Write 16-bit command, D[7:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[7:0]
					1	↑	1	Read 16/18/24-bit display data, D[7:0]
					1	↑	1	Read 16-bit parameter or status, D[7:0]
0	0	0	1	16-bit Parallel	0	1	↑	Write 16-bit command, D[7:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[15:0]
					1	↑	1	Read 16/18/24-bit display data, D[15:0]
					1	↑	1	Read 16-bit parameter or status, D[15:0]
0	0	1	0	24-bit Parallel	0	1	↑	Write 16-bit command, D[23:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[23:0]
					1	↑	1	Read 16/18/24-bit display data, D[23:0]
					1	↑	1	Read 16-bit parameter or status, D[23:0]

5.1.2.1 WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[23:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

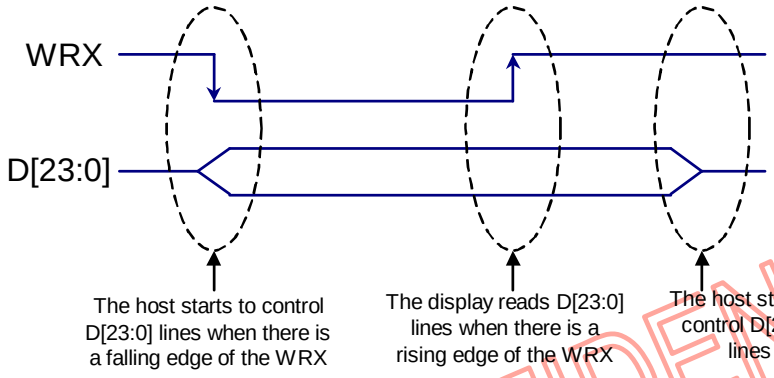


Fig. 5.1.1 80-Series WRX protocol

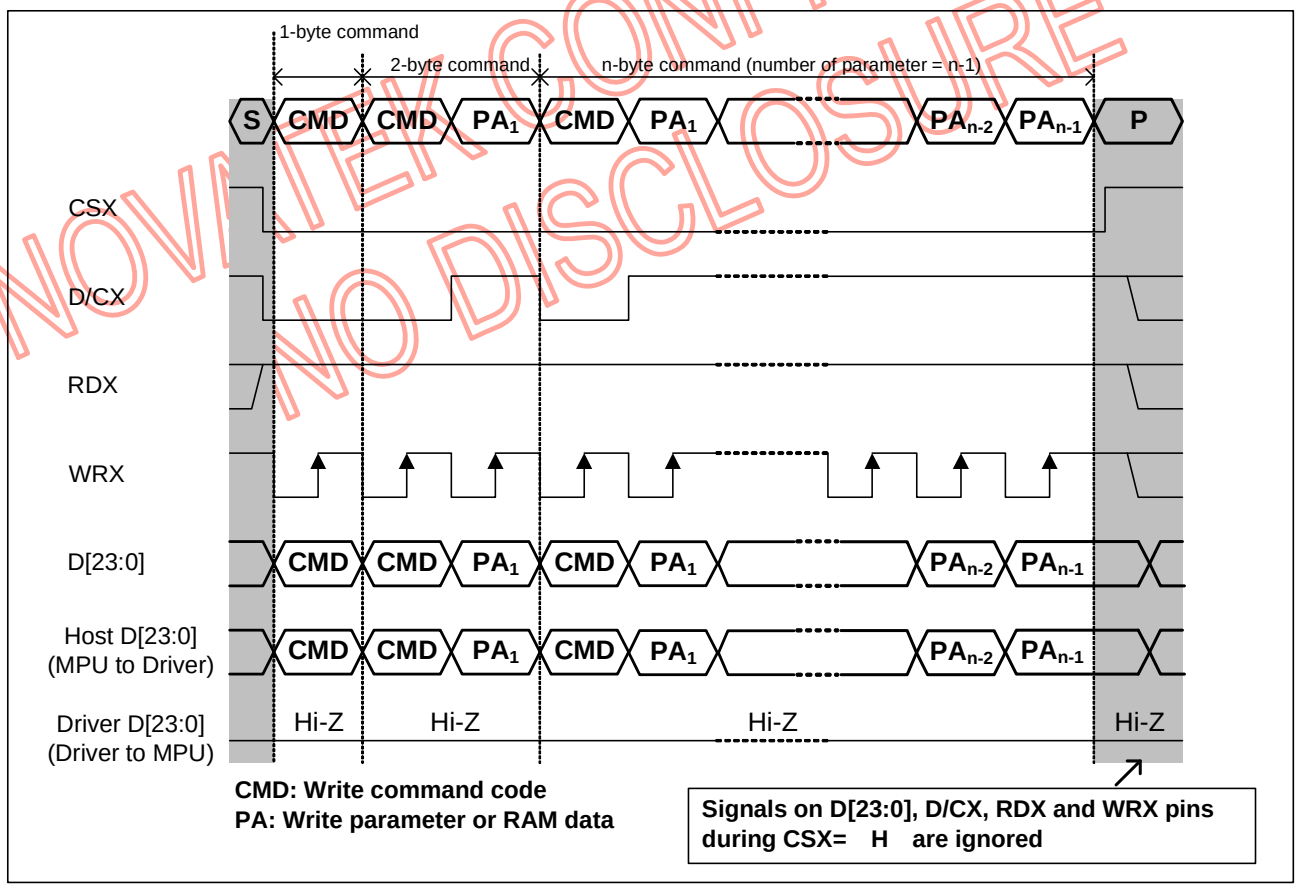


Fig. 5.1.2 80-Series parallel bus protocol, write to register or display RAM

5.1.2.2 READ CYCLE SEQUENCE

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

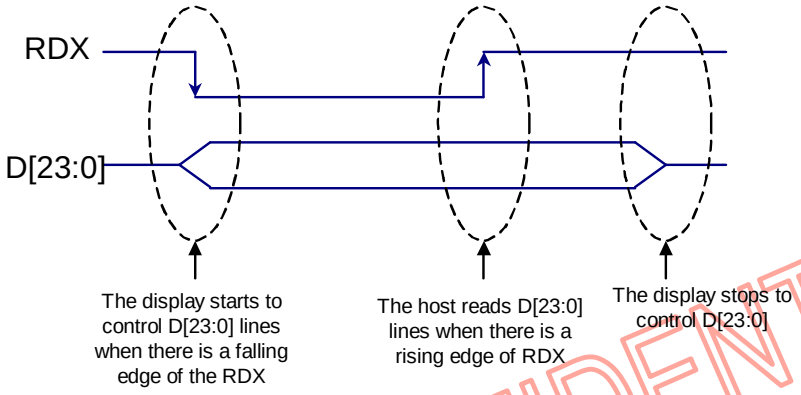


Fig. 5.1.3 80-Series RDX protocol

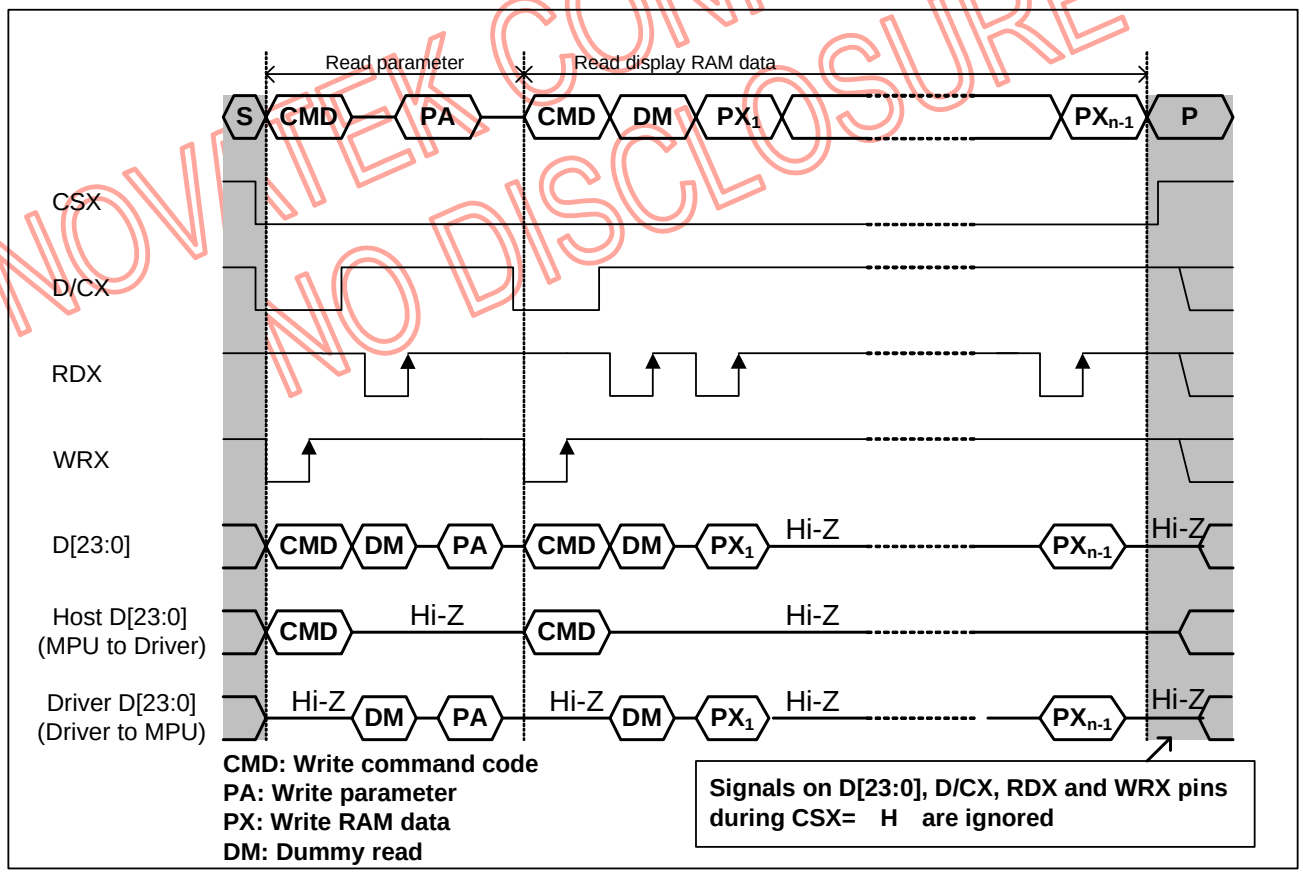


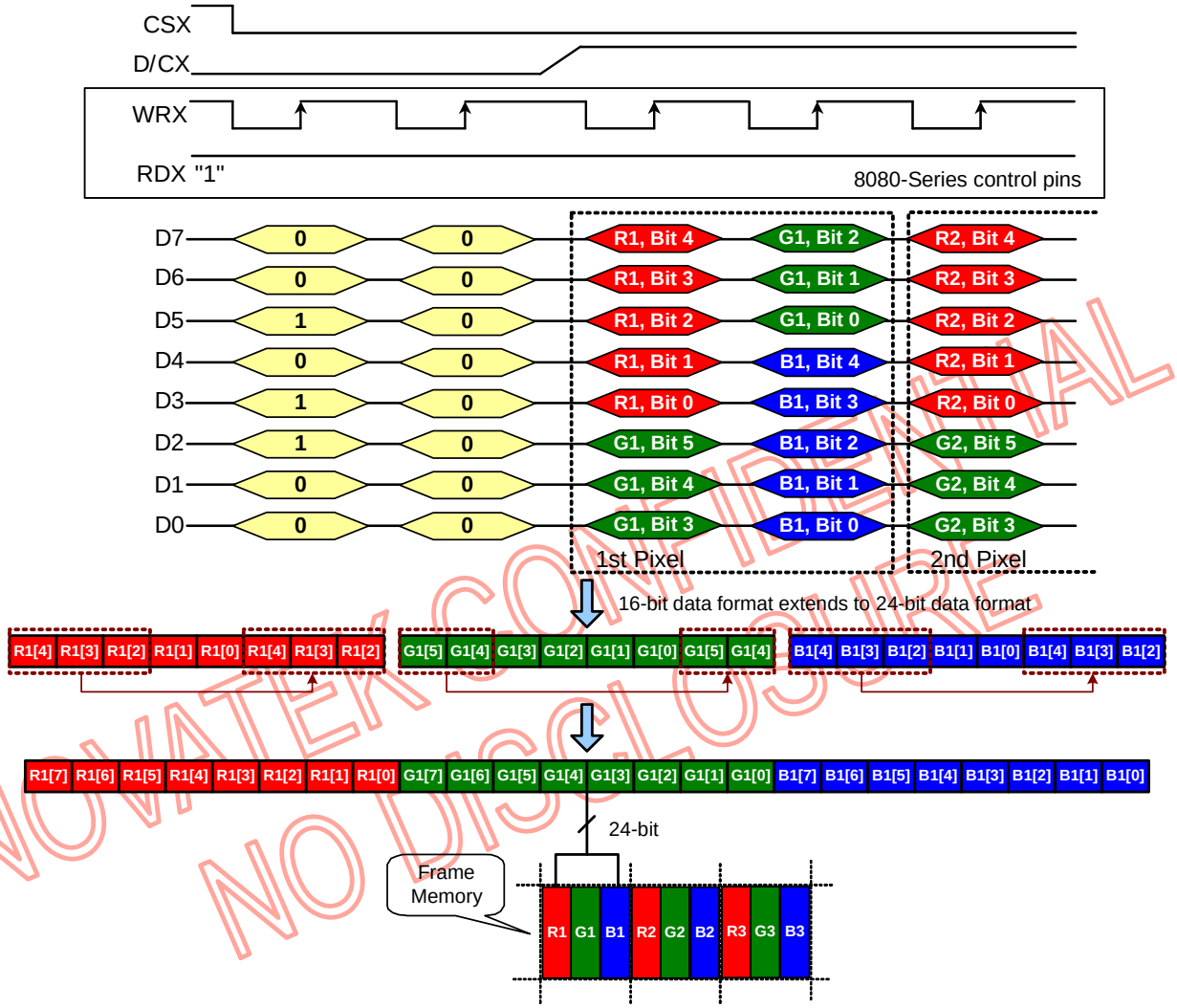
Fig. 5.1.4 80-Series parallel bus protocol, read from register or display RAM

5.1.2.3 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
0006h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
0007h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	

- 65K colors, RGB is 5-6-5-bit pixel data input



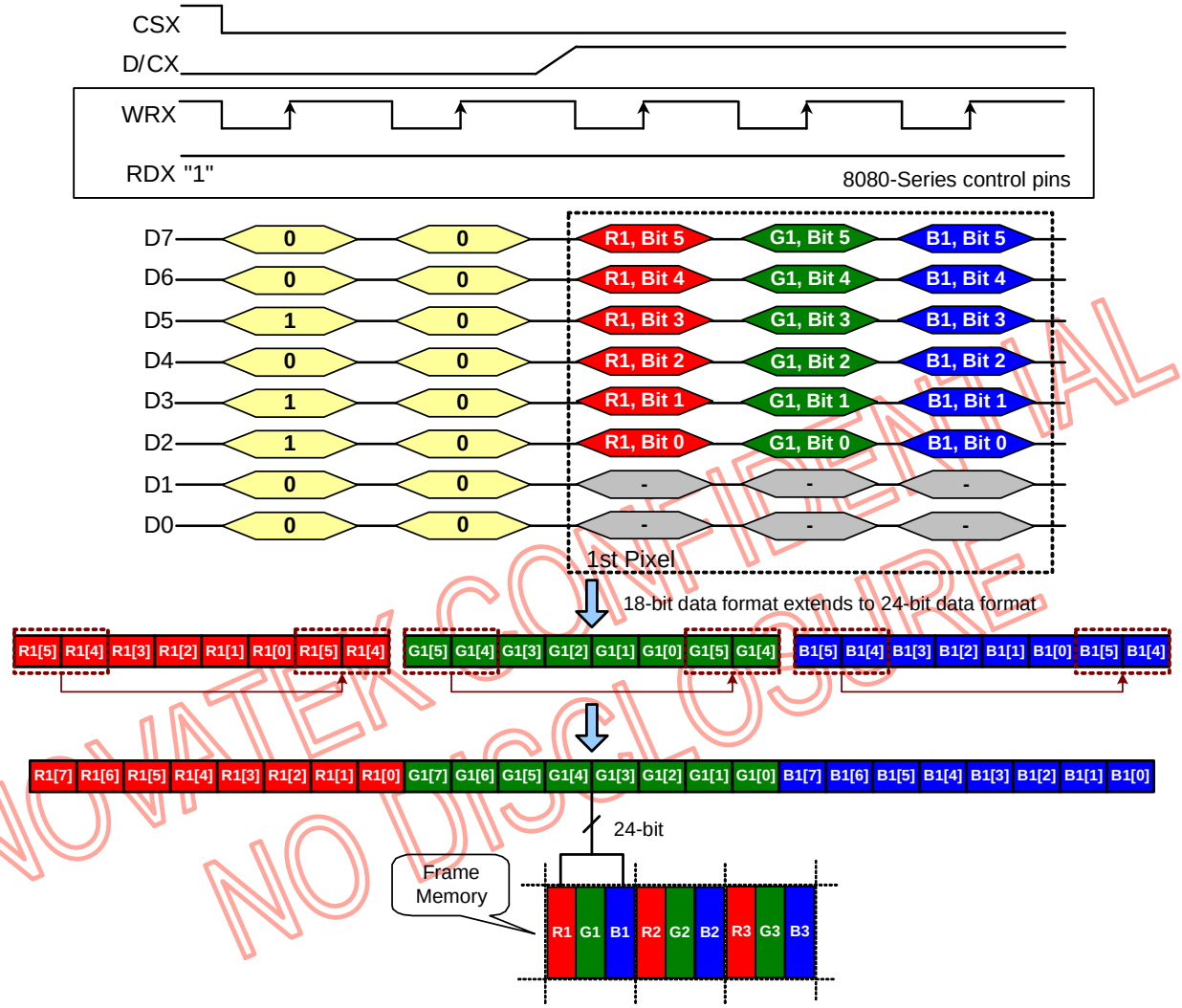
NOTES:

1. 2 times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bit pixel data input



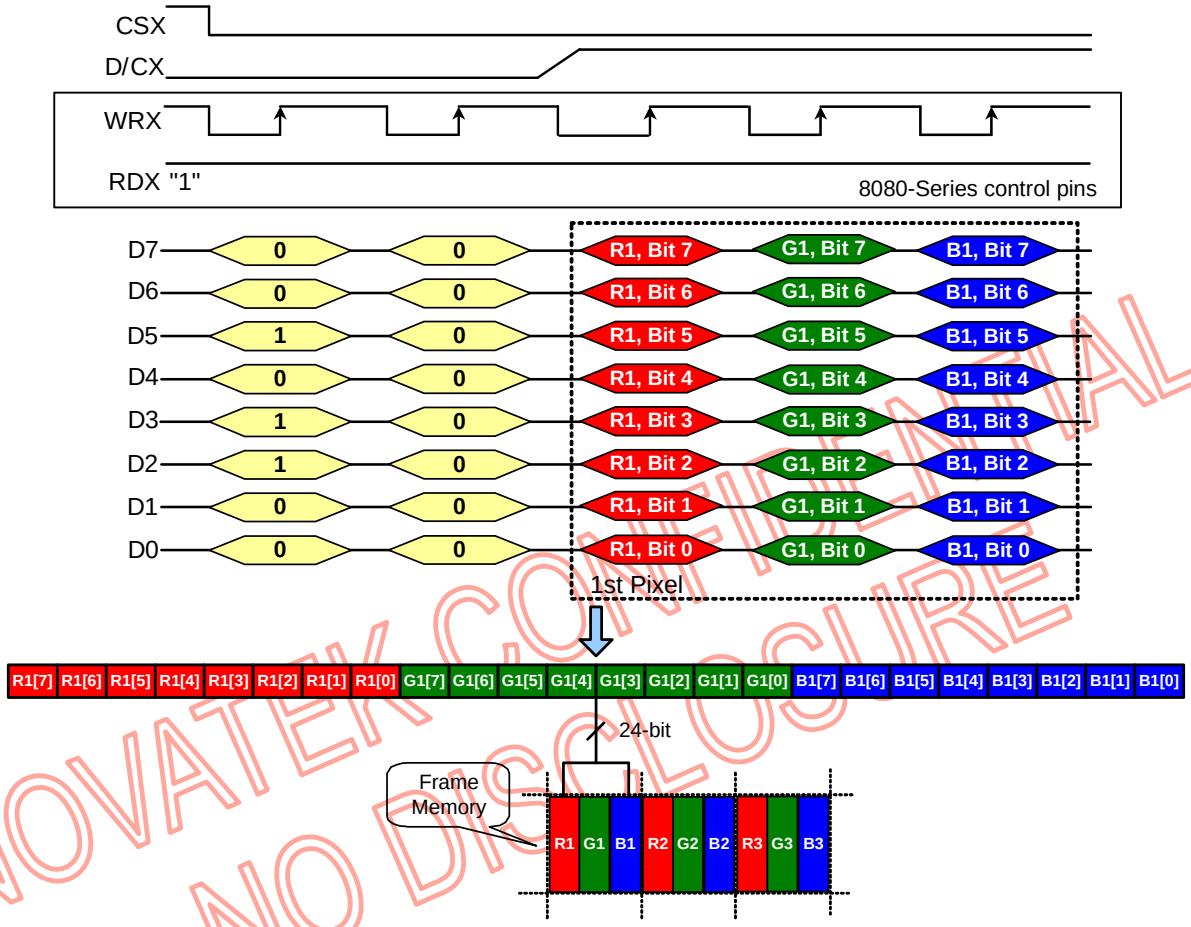
NOTES:

1. 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



NOTES:

1. 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.

2. The most significant bits are Rx7, Gx7 and Bx7.

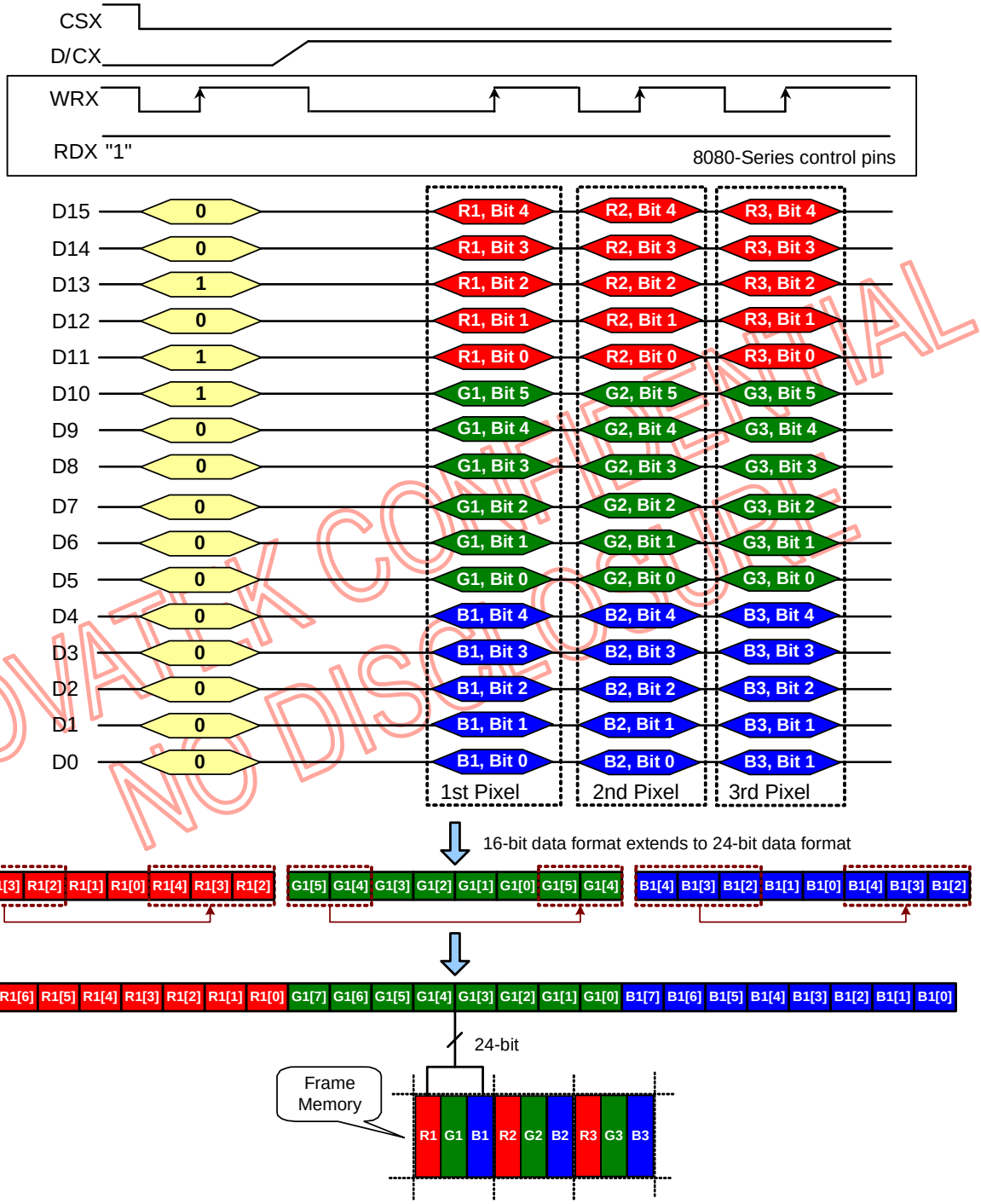
3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.4 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
0006h	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color
	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
0007h	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

- 65K colors, RGB is 5-6-5-bit pixel data input

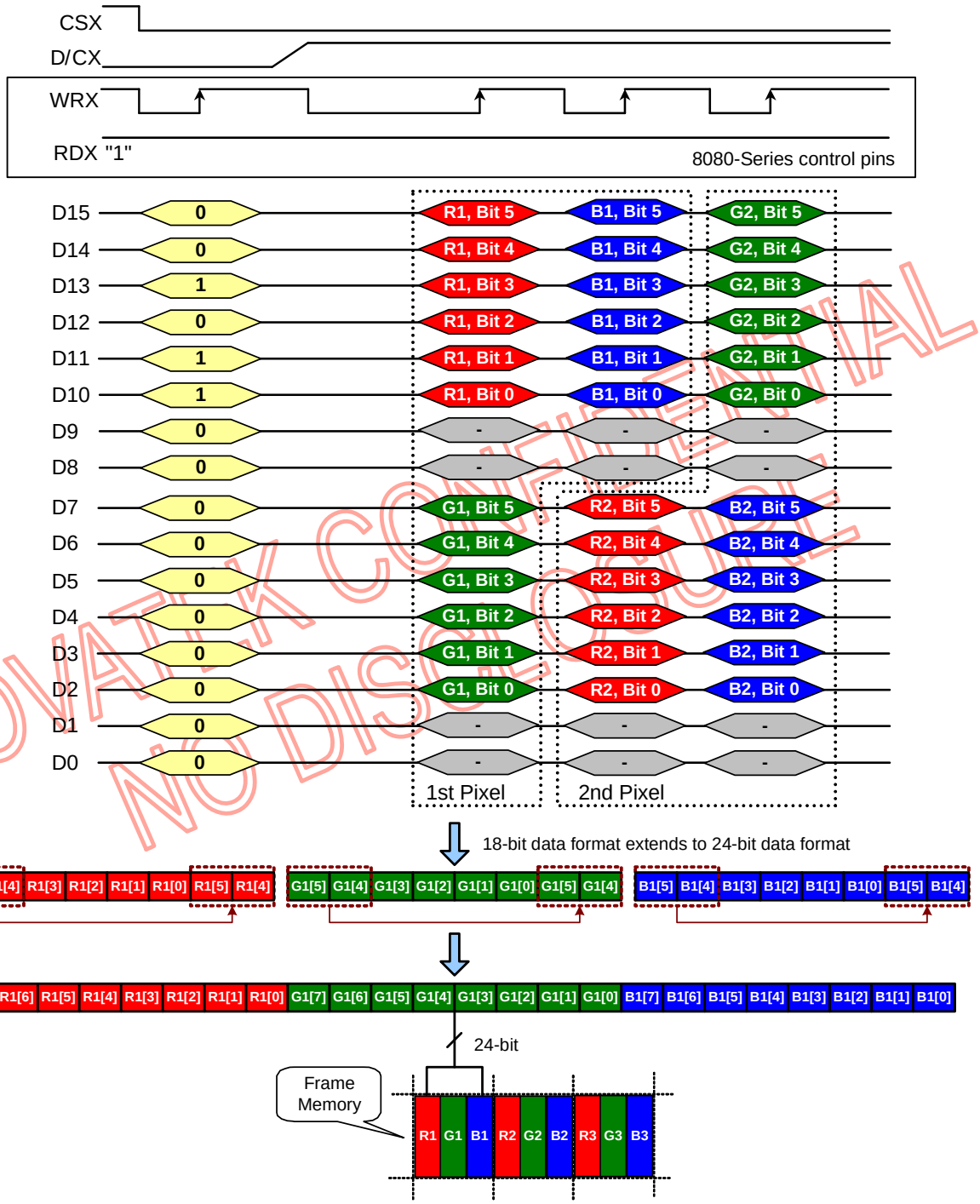


1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bit pixel data input

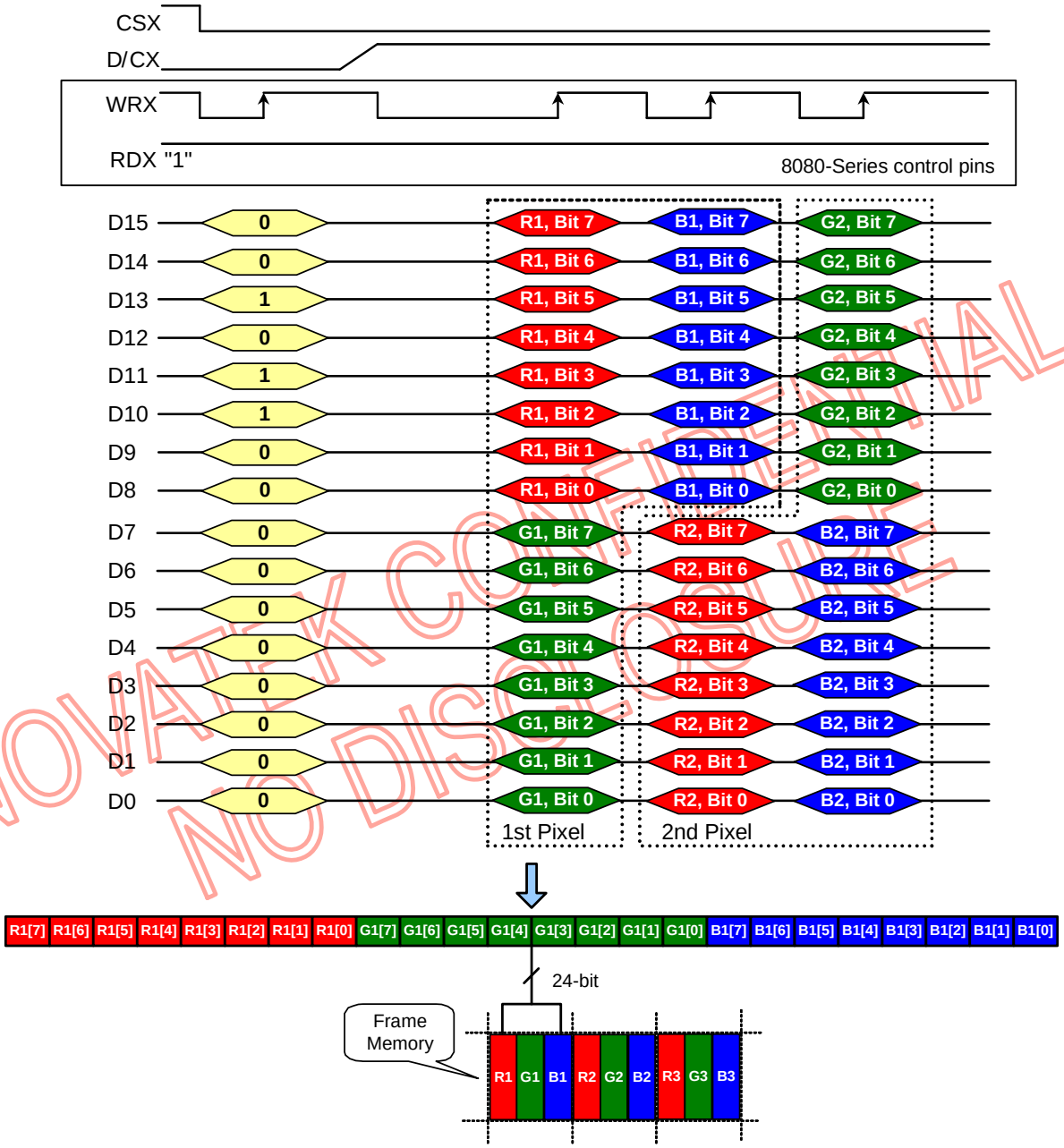


1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.

2. The most significant bits are Rx7, Gx7 and Bx7.

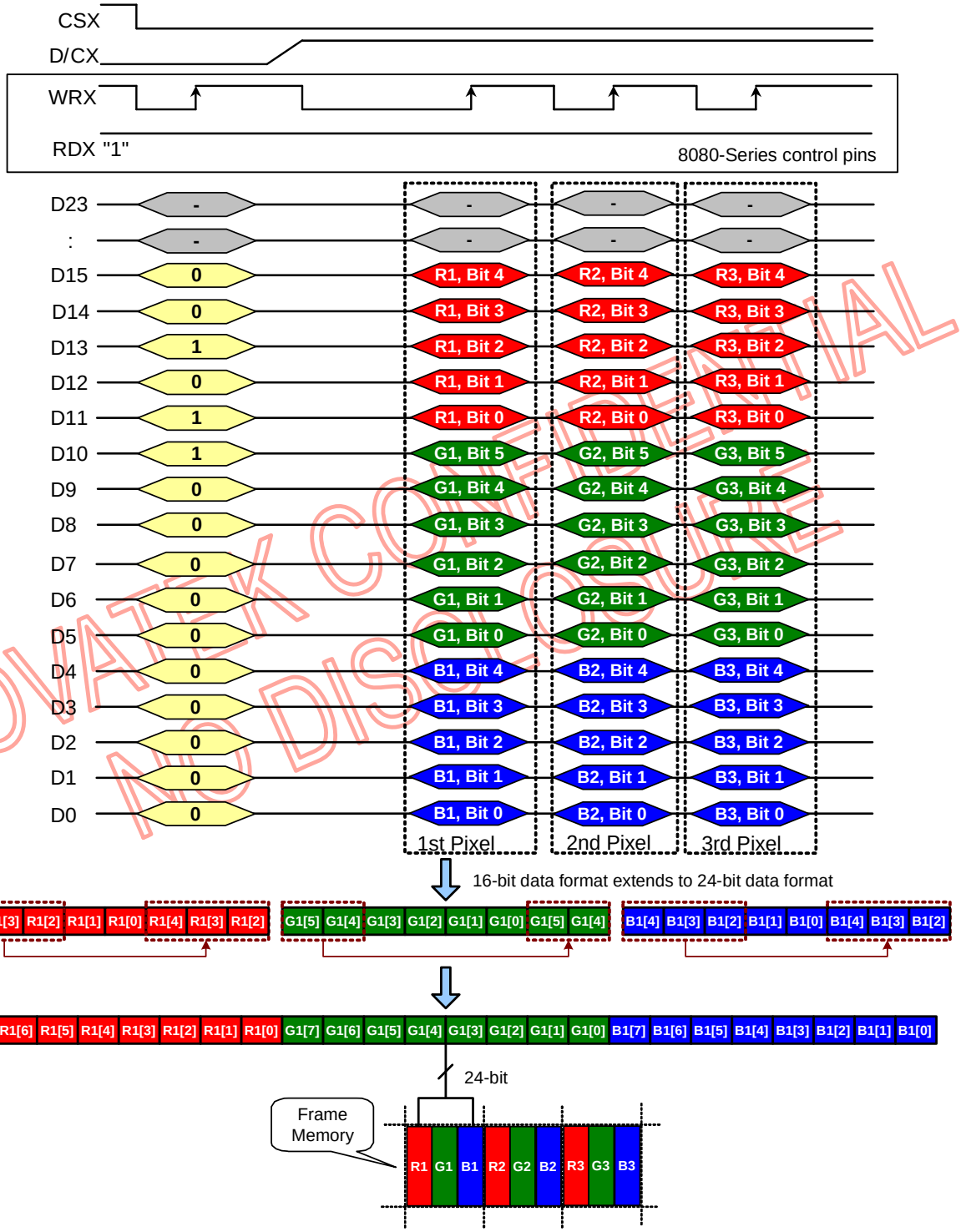
3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.5 24-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
0006h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color
0007h								R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color

- 65K colors, RGB is 5-6-5-bit pixel data input

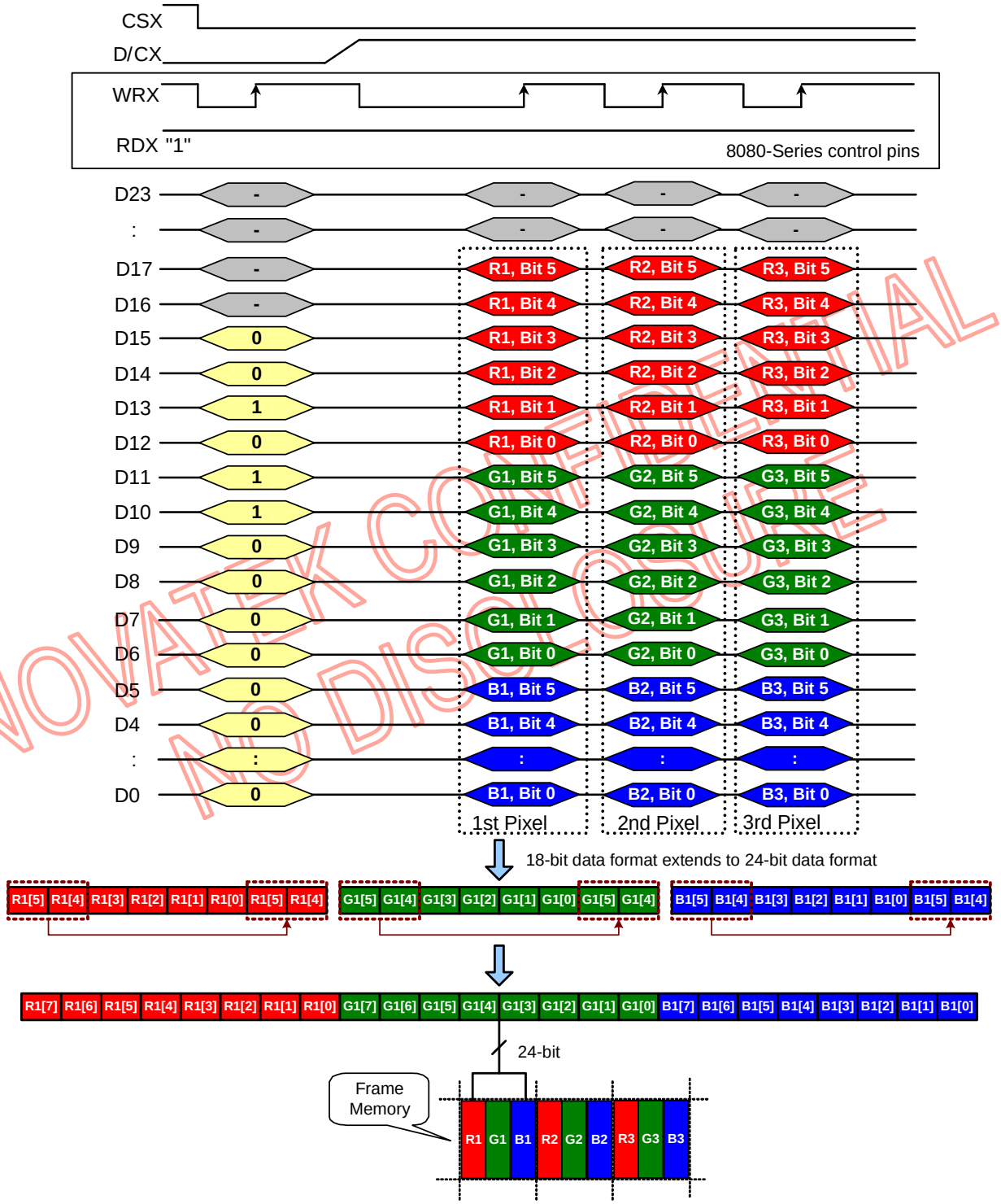


1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bi pixel data t input

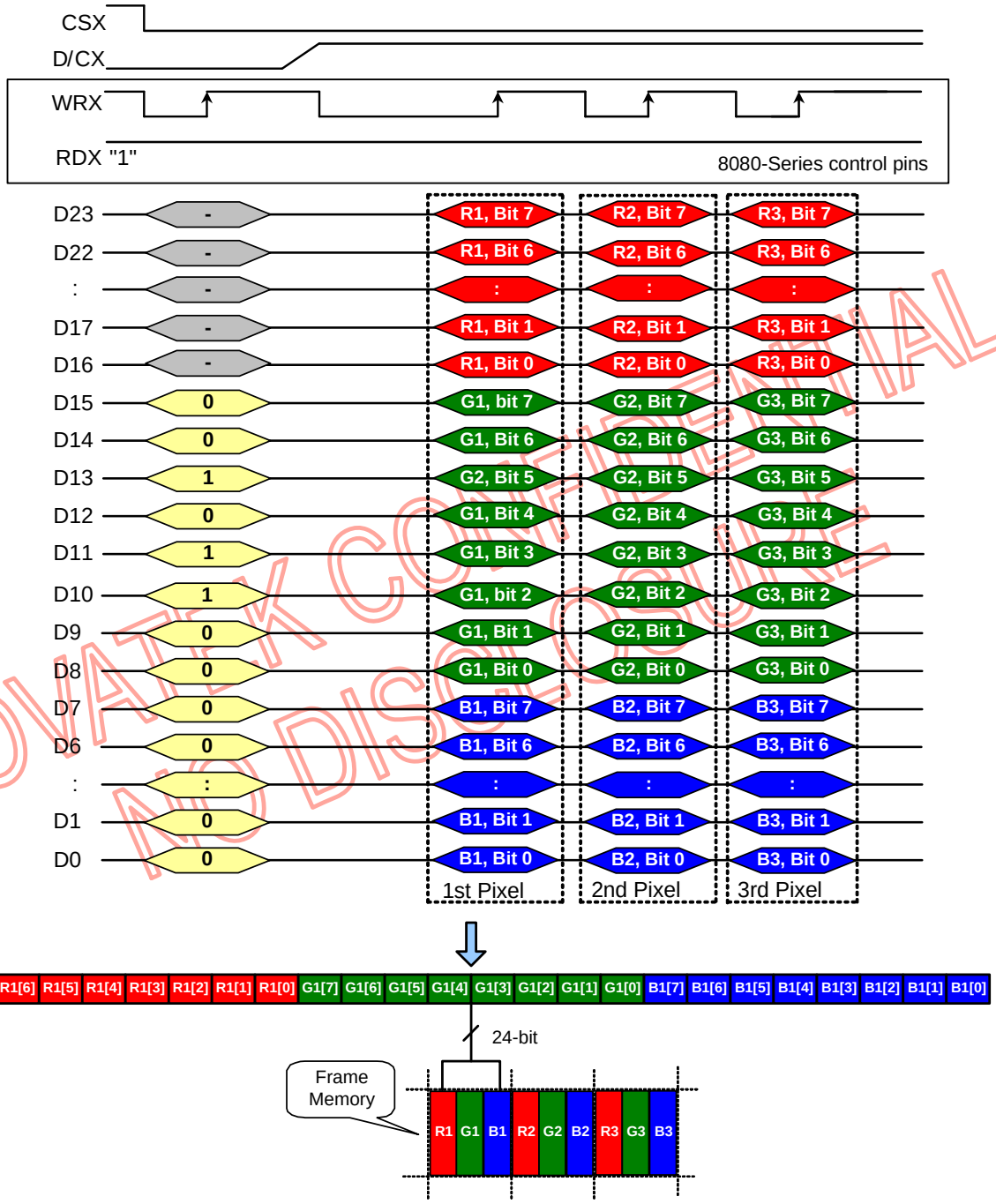


1. In one transfer (D17 to D0), 1 pixel data transmitted with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



1. In one transfer (D23 to D0), 1 pixel data transmitted with the 24-bit color depth information.

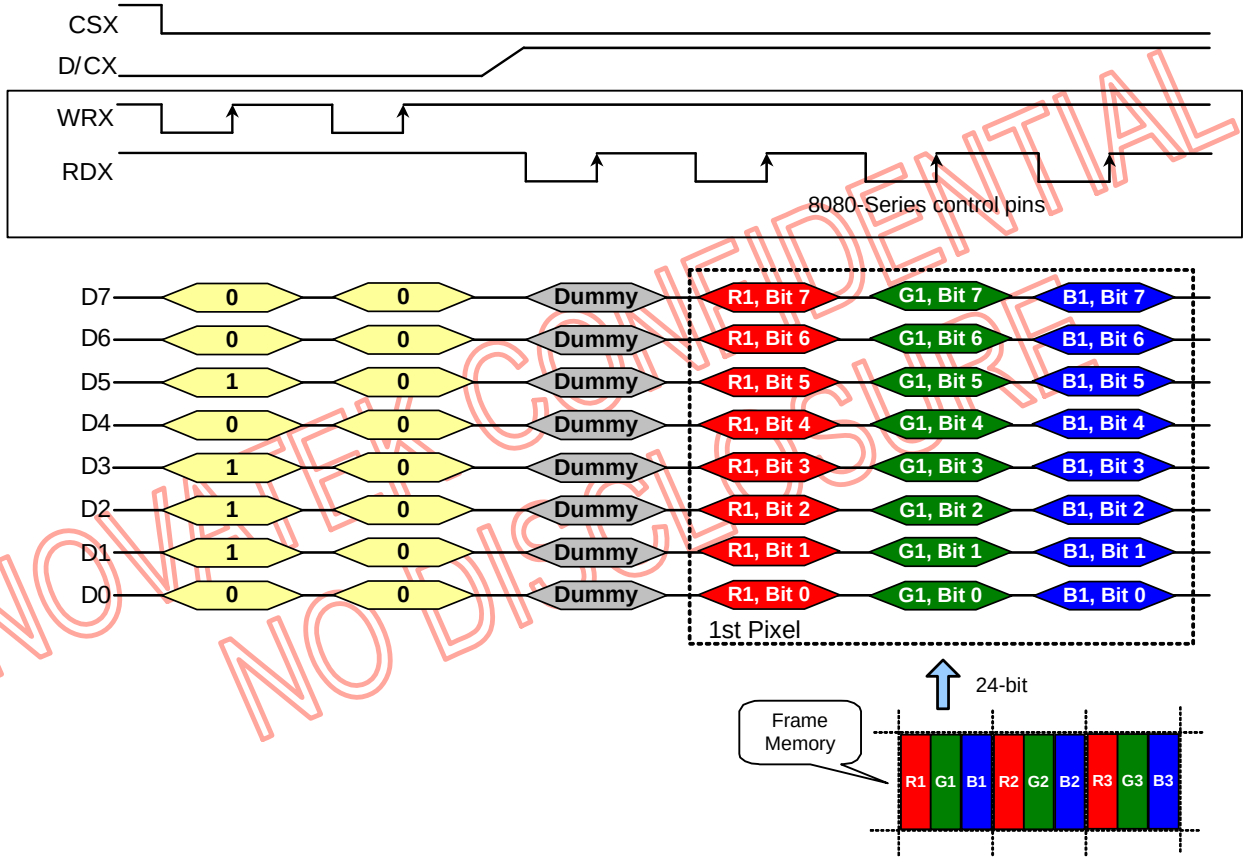
2. The most significant bits are Rx7, Gx7 and Bx7.

3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.6 8-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

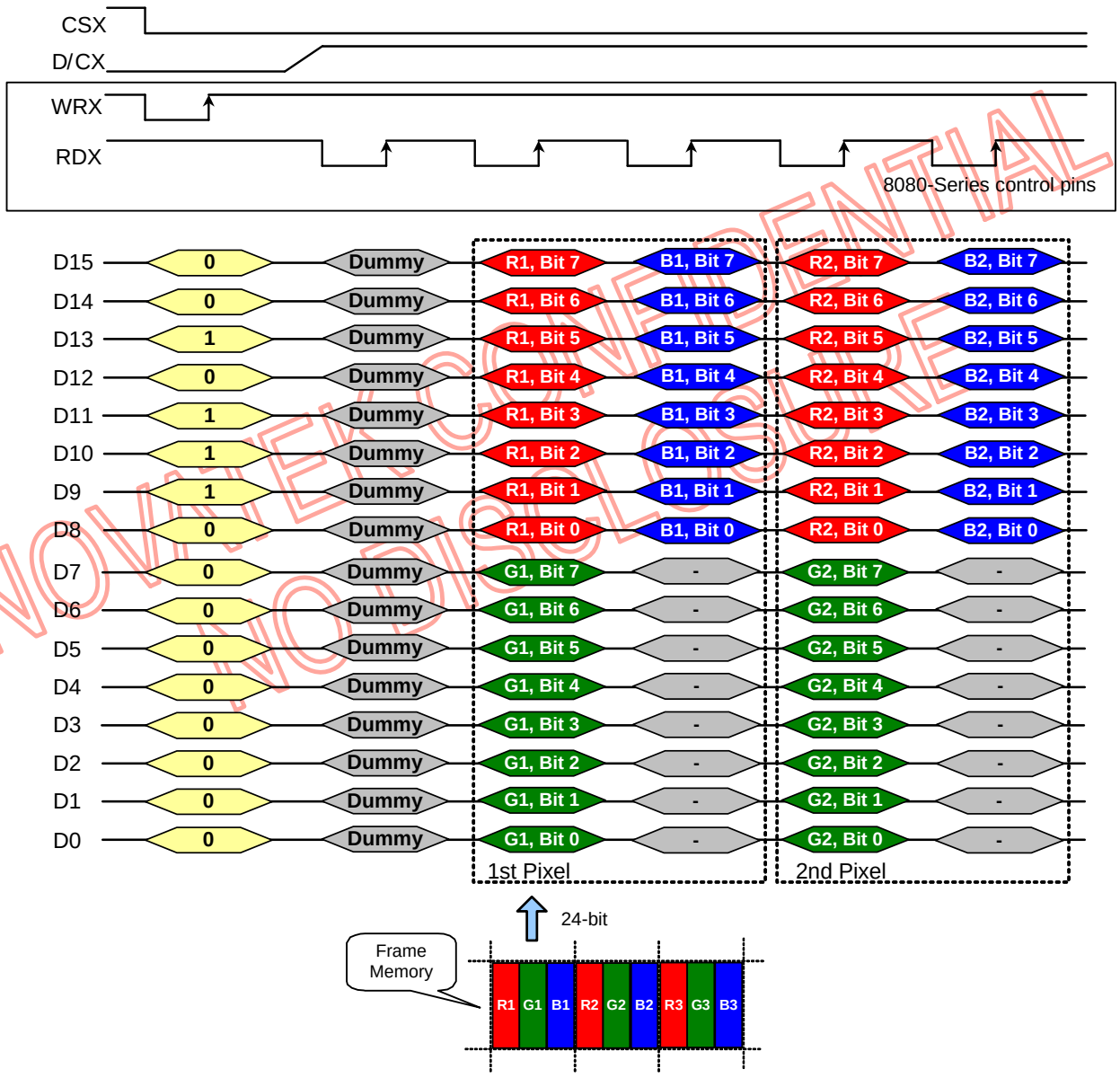
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Register Command	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	00h
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Read Data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	



5.1.2.7 16-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

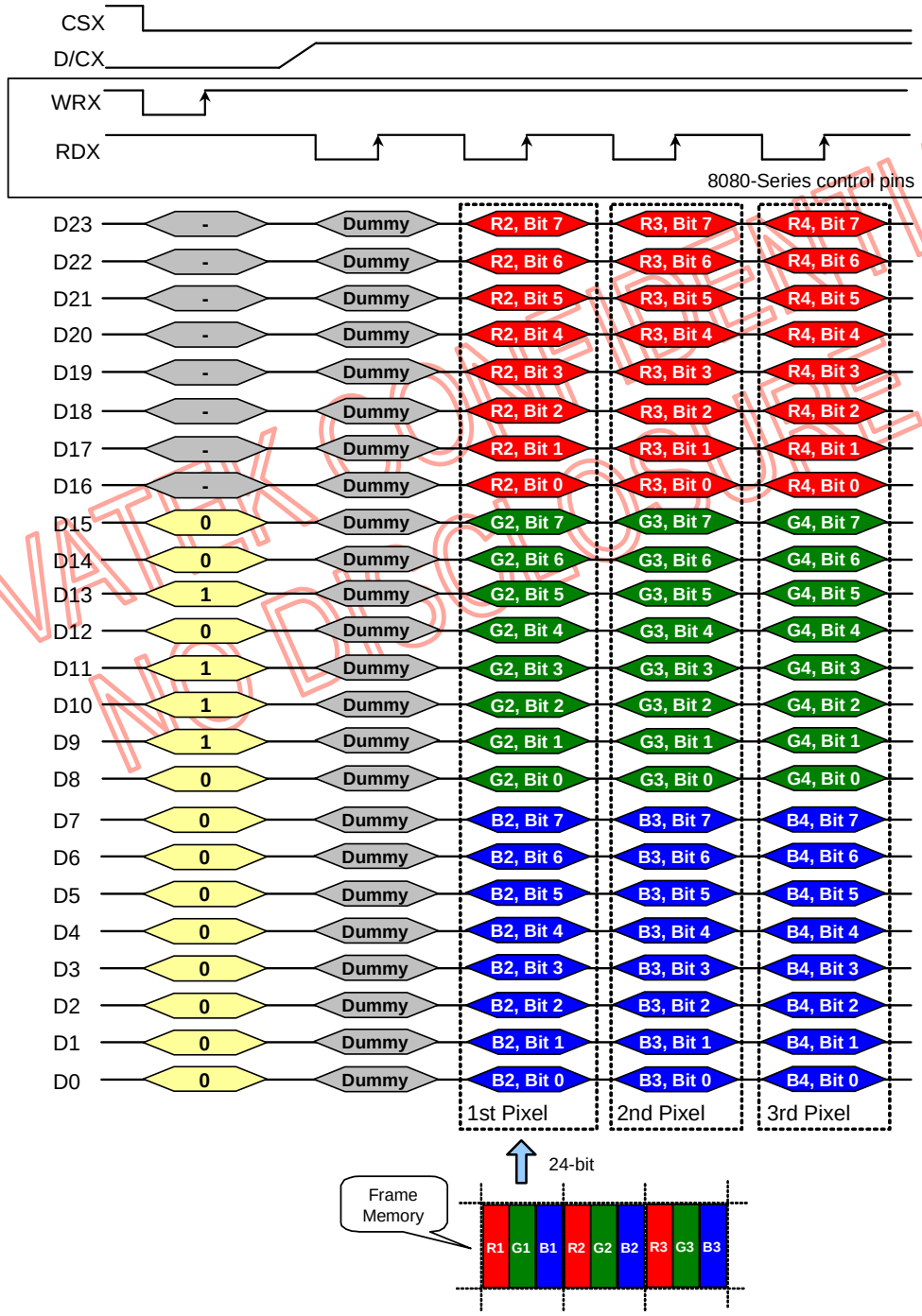
Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read Data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	



5.1.2.8 24-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read Data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
								R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color



5.1.3 Serial Interface

The selection of this interface is done by IM3, IM2, IM1 and IM0.

The serial interface can select IM3 = 0 or 1 to decide the trigger edge of serial clock (SCL) is rising edge or falling edge. The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

5.1.3.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT35510. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see ***Fig. 5.1.5***). SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

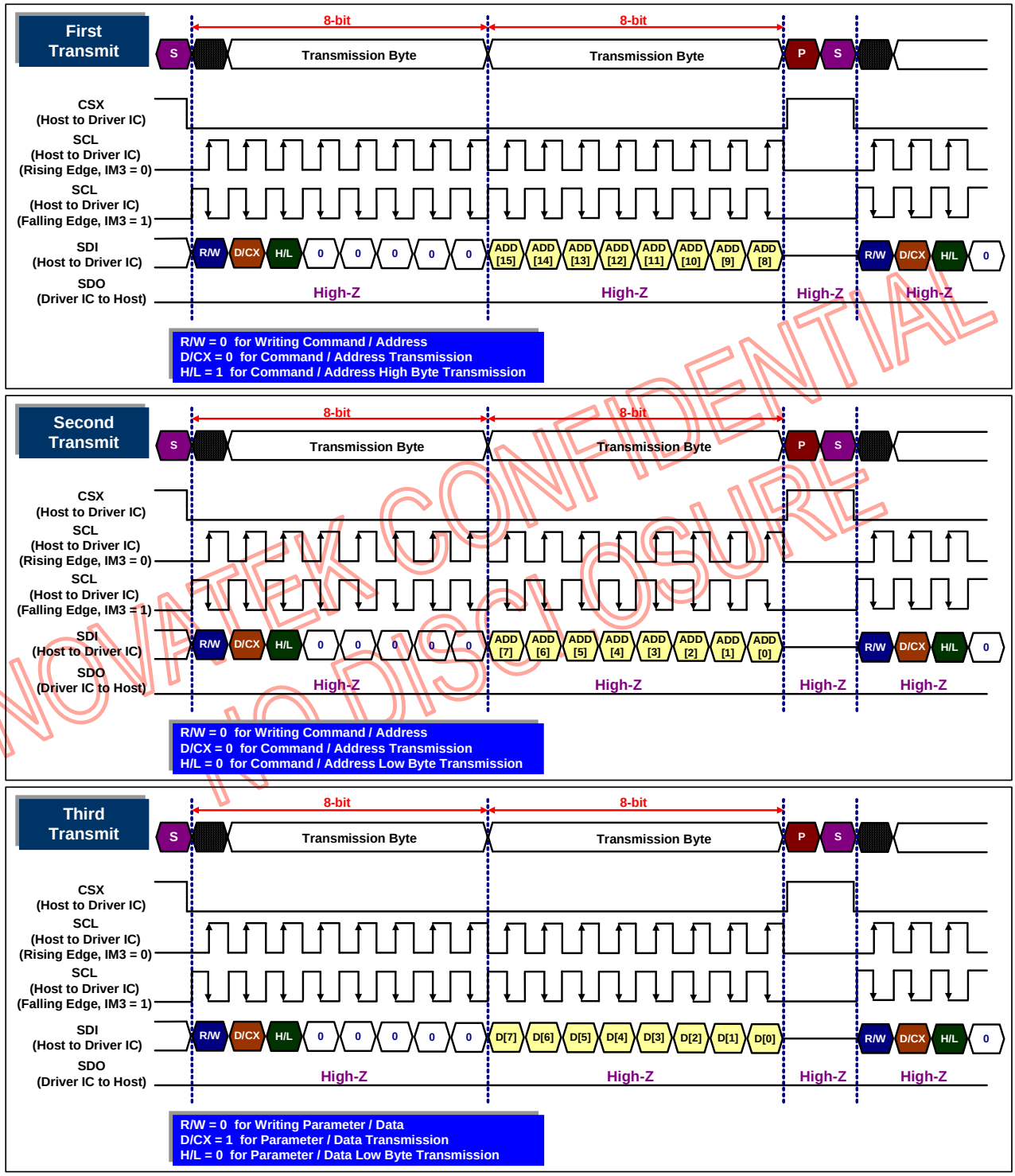


Fig. 5.1.5 Serial bus protocol for register write mode

5.1.3.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT35510. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see ***Fig. 5.1.6***). The NT35510 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (16 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

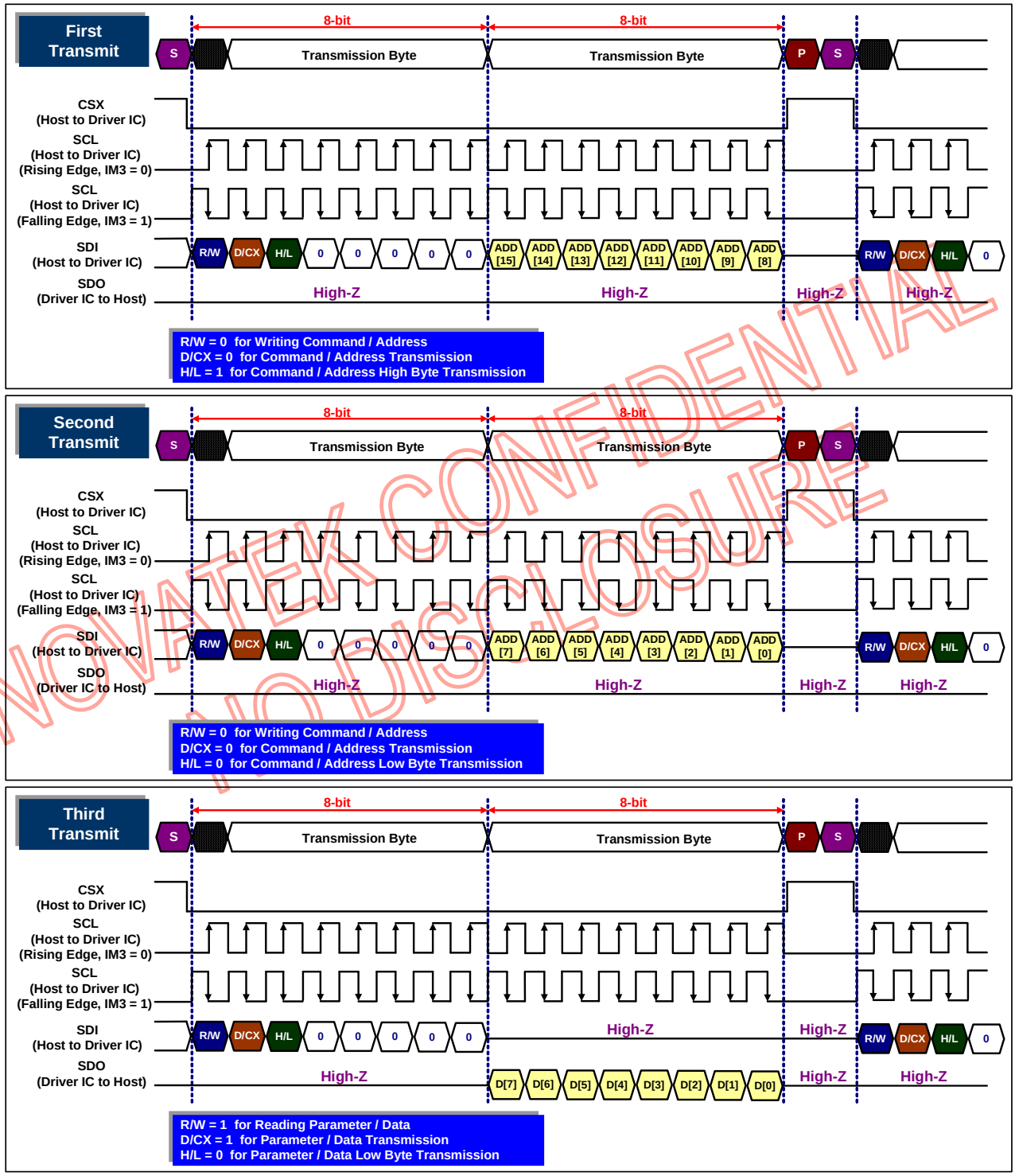
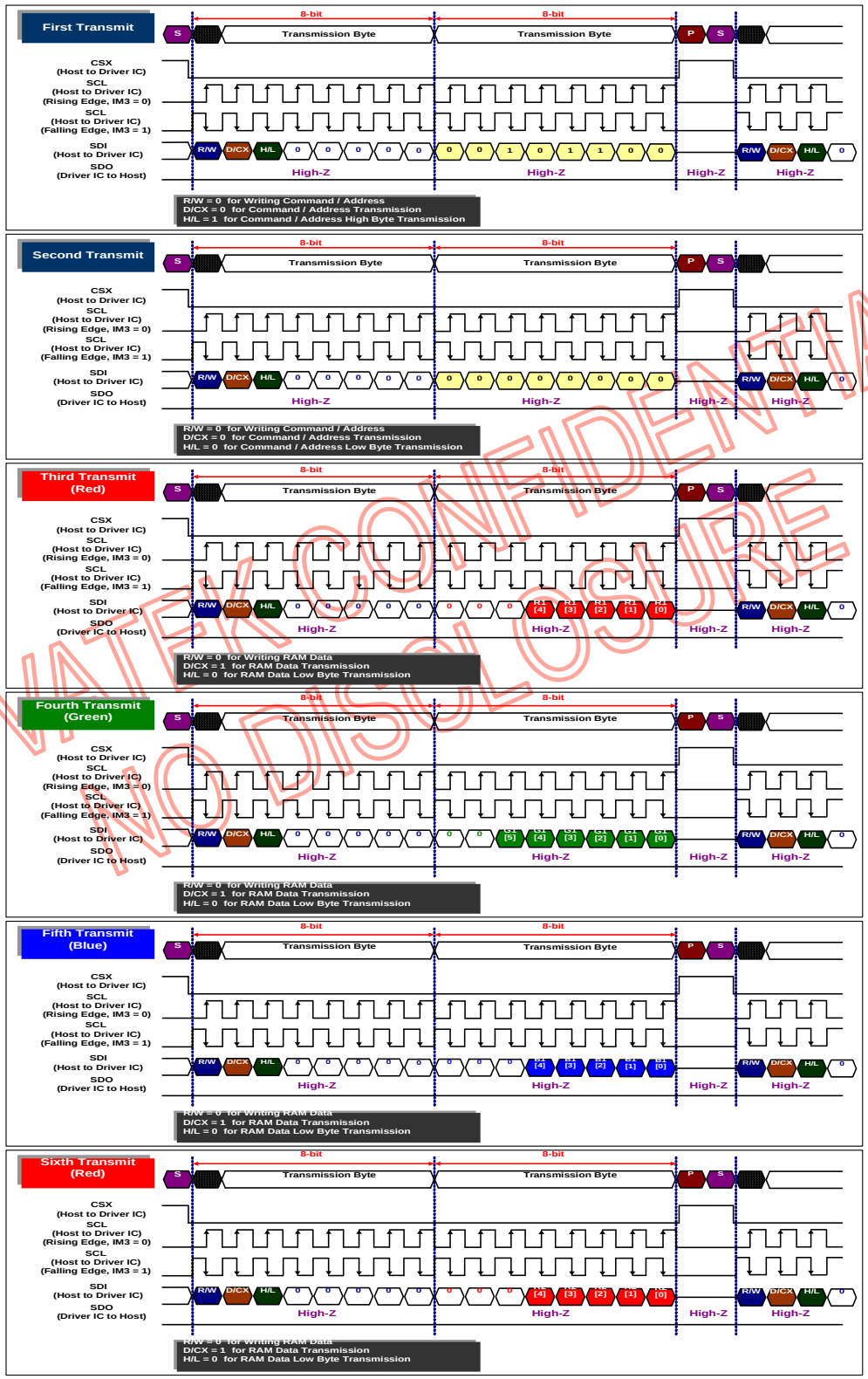


Fig. 5.1.6 Serial bus protocol for register read mode

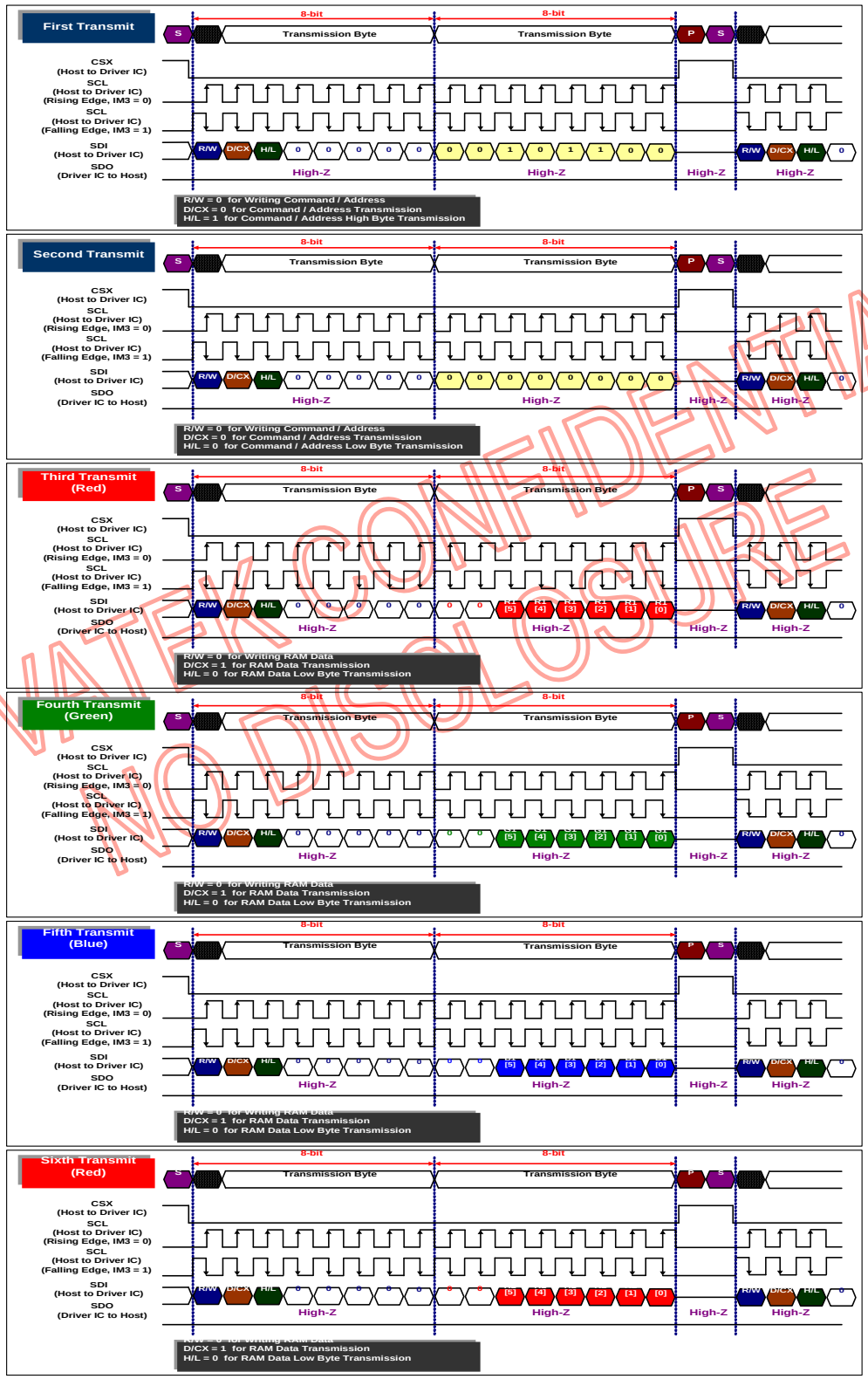
5.1.3.3 SERIAL INTERFACE FOR DATA RAM WRITE

The serial interface is used with RGB interface (IM[2:0]=”011”) or MDDI interface (IM[2:0]=”110”). In RGB+SPI interface, the data RAM write function for SPI is valid when bit ICM=”1” (command B300h of page 0). In MDDI+SPI interface, the data RAM write function for SPI is valid when MDDI is not writing data to RAM. Different display data formats are available for three color depths supported by the LCM listed below:

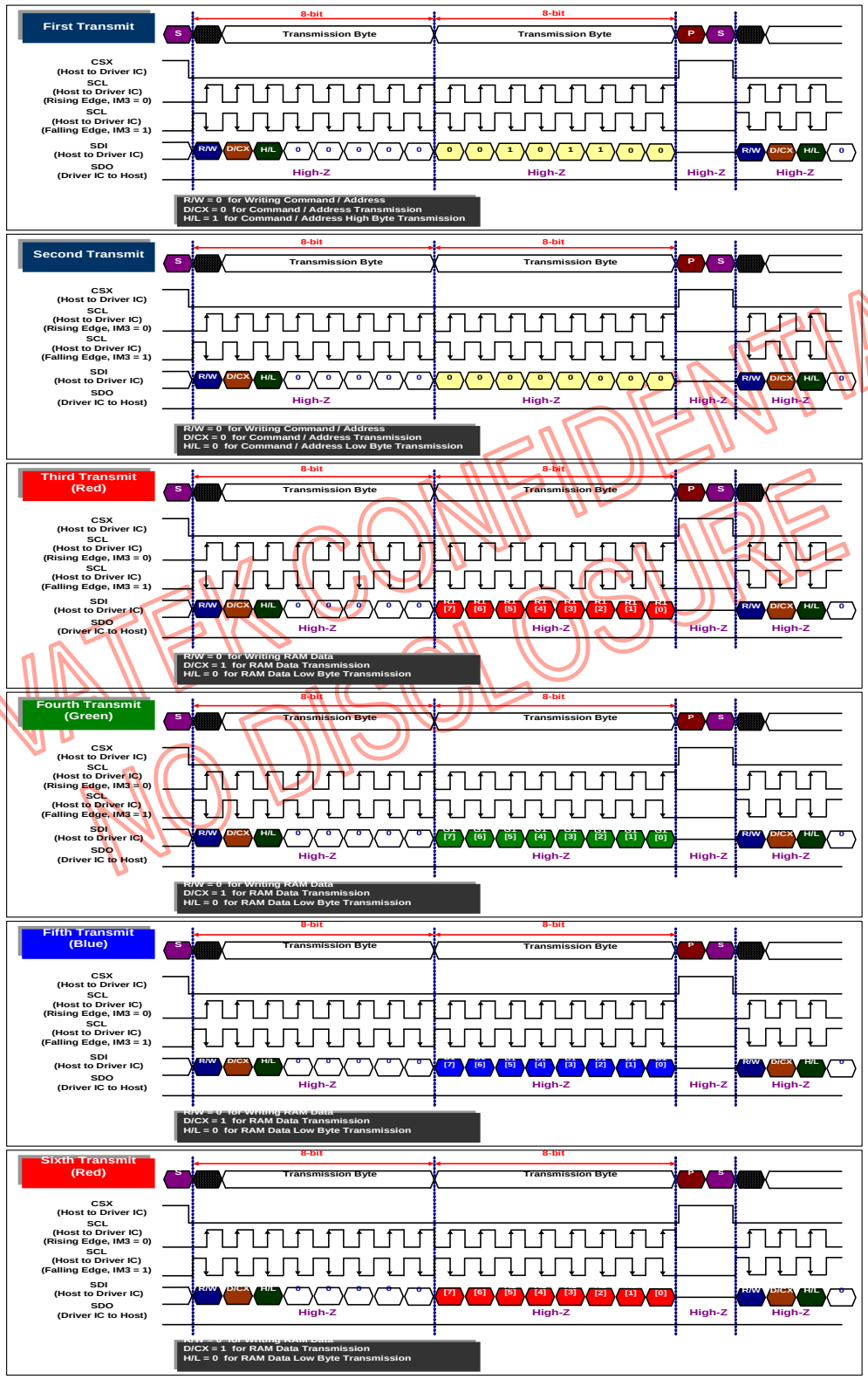
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)



- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006)

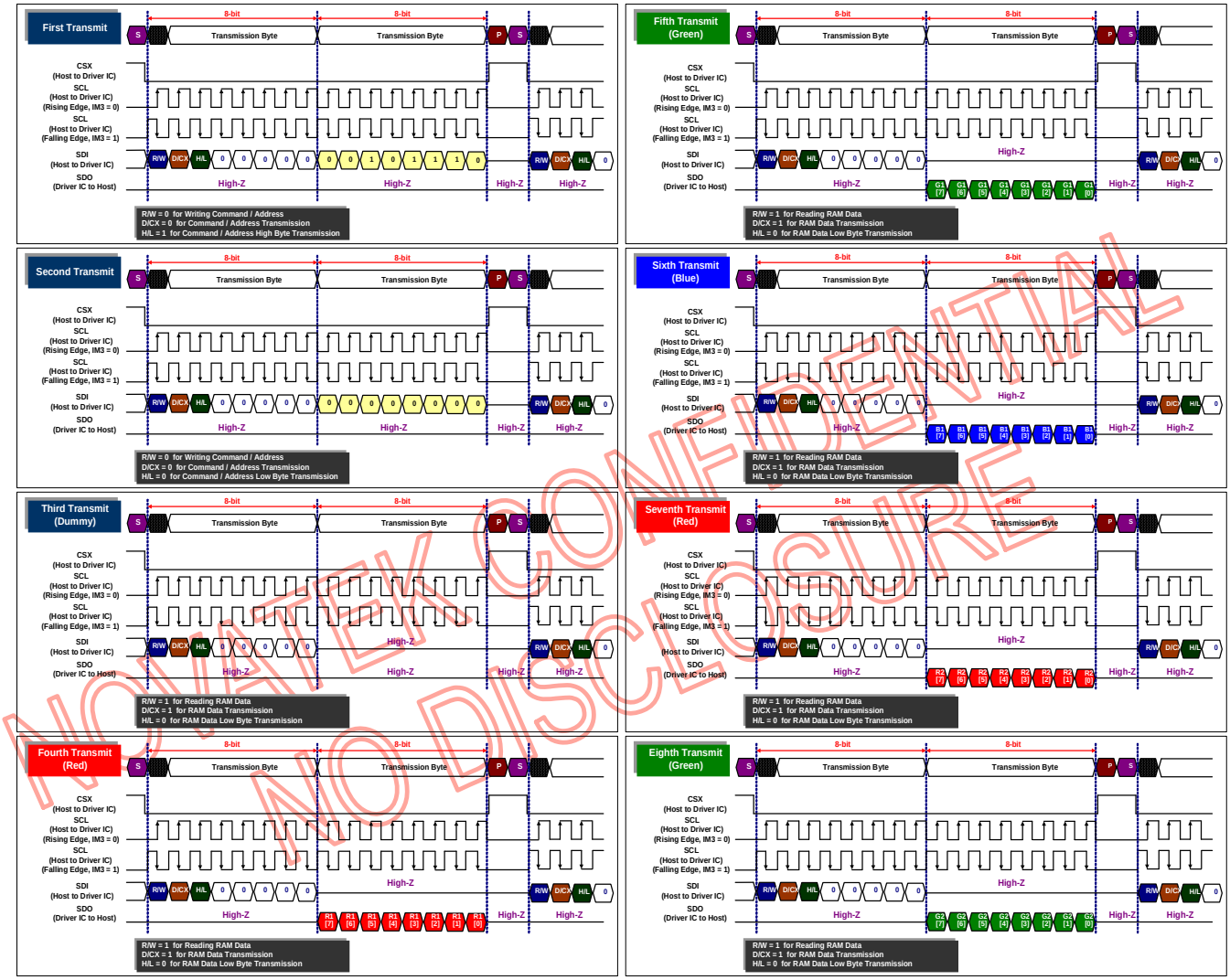


- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)



5.1.3.4 SERIAL INTERFACE FOR DATA RAM READ

The read data RGB is 8-8-8-bit output as below.



5.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I2C-Bus Protocol:
Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

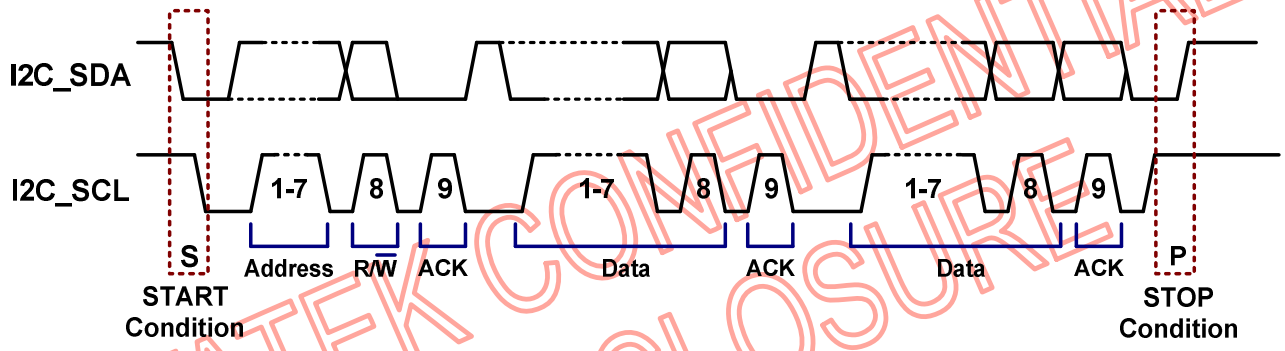


Fig. 5.2.1 Definition of I2C-Bus Protocol

(b) Definitions:
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

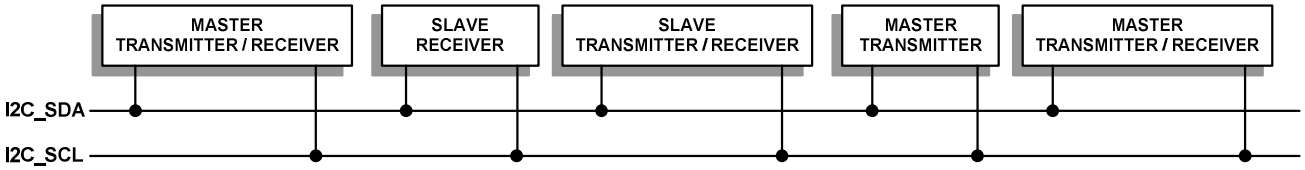


Fig. 5.2.2 System Configuration

5.2.1 Slave Address of I2C

NT35510 supports two slave addresses, 1001100, 1001101 after the START procedure via I2C bus for MCU usage .There are 1 hard pin, I2C_SA0 to determine the difference slave address. The slave address selection is described as the following table. The I2C interface address is selected from the external MPU.

Table 5.2.1 Selection Table of Slave Address

I2C_SA0	Slave Address	Notes
0	1001100	0000xxx and 1111xxx: Reversed
1	1001101	

5.2.2 Register Write Sequence of I2C Interface

NT35510 supports register write sequence via I2C-bus transfer. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in Fig.5.2.2.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "zero" for WRITE.
(3) The slave issues an ACK to master.
(4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
(5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter.
(6) A data transfer is always terminated by a STOP condition.

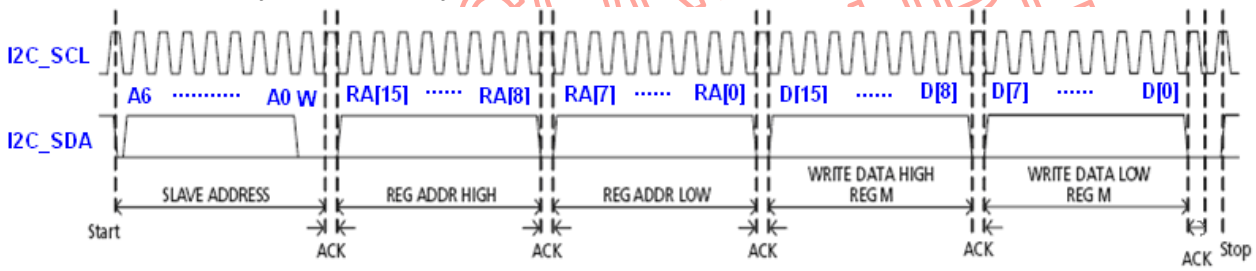


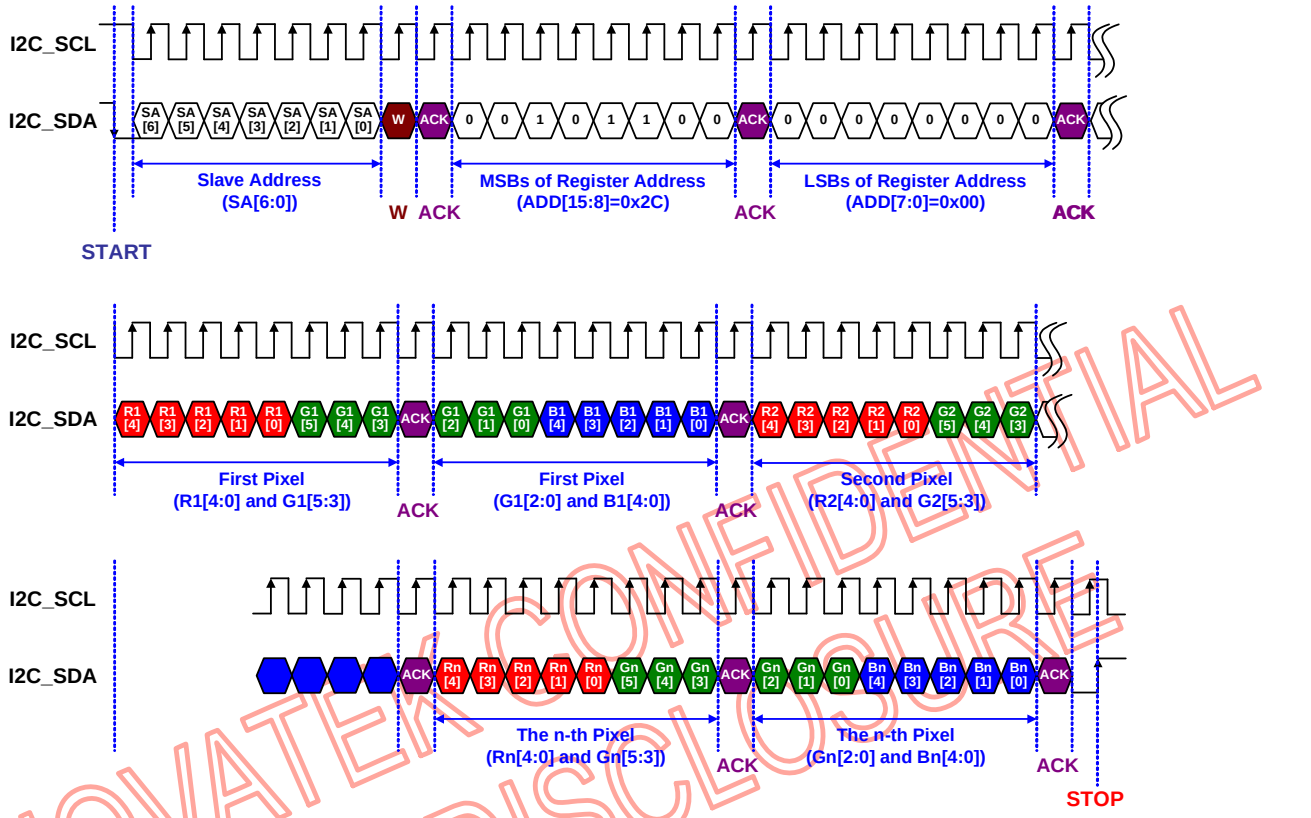
Fig. 5.2.3 Register Writing Timing of I2C Interface

5.2.3 RAM Data Write Sequence of I2C Interface

NT35510 supports sequential RAM data writing via I2C-Bus. NT35510 will increase the RAM address automatic by window address when the Host MCU write the RAM data via this way. The transfer protocol of window address setting can refer to the 5.2.3 Register Write Sequence. Different display data formats are available for three color depths supported by the LCM.

The sequential RAM writing timing is shown in below.

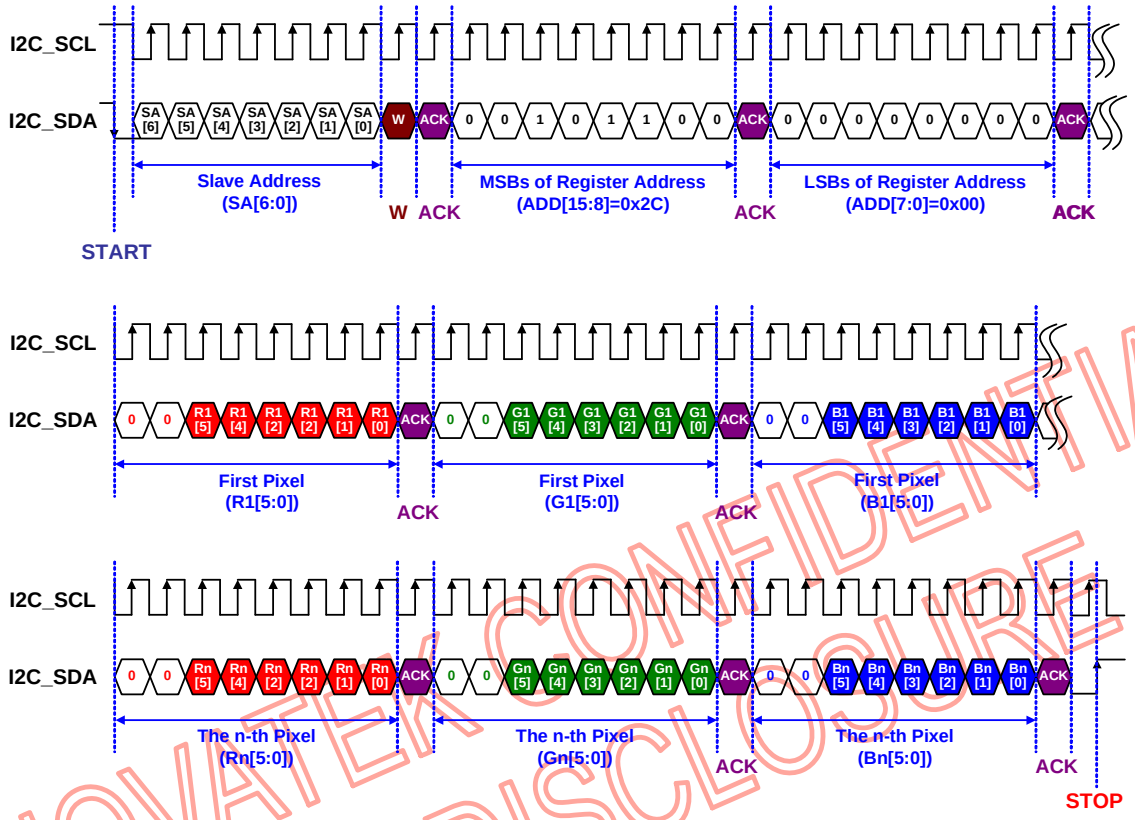
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[4:0], R2[4:0], , Rn[4:0]: The red color data of each pixel
G1[5:0], G2[5:0], , Gn[5:0]: The green color data of each pixel
B1[4:0], B2[4:0], , Bn[4:0]: The blue color data of each pixel

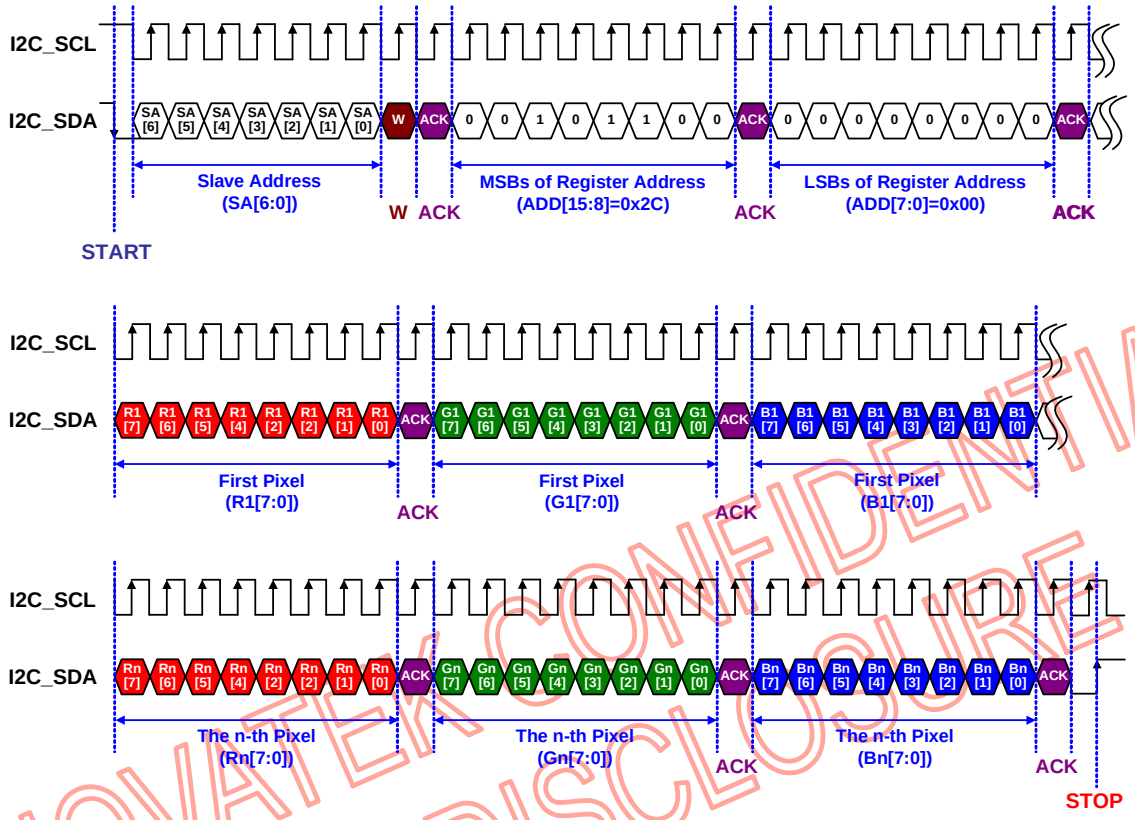
- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[5:0], R2[5:0], , Rn[5:0]: The red color data of each pixel
G1[5:0], G2[5:0], , Gn[5:0]: The green color data of each pixel
B1[5:0], B2[5:0], , Bn[5:0]: The blue color data of each pixel

- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[7:0], R2[7:0], , Rn[7:0]: The red color data of each pixel
G1[7:0], G2[7:0], , Gn[7:0]: The green color data of each pixel
B1[7:0], B2[7:0], , Bn[7:0]: The blue color data of each pixel

5.2.4 Register Read Sequence of I2C Interface

NT35510 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in Fig.5.2.4.

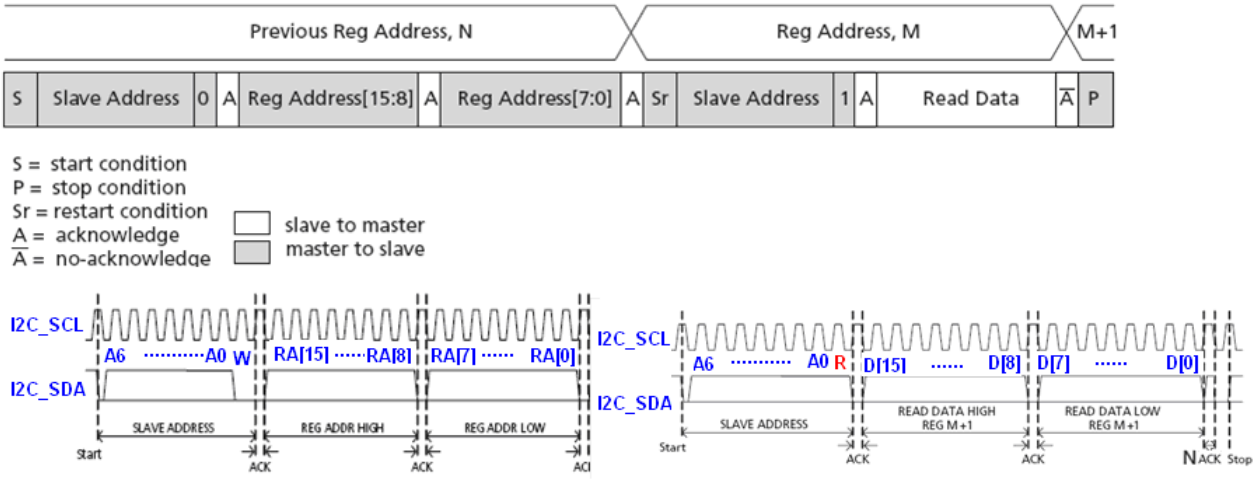


Fig. 5.2.4 Register Reading Timing of I2C Interface

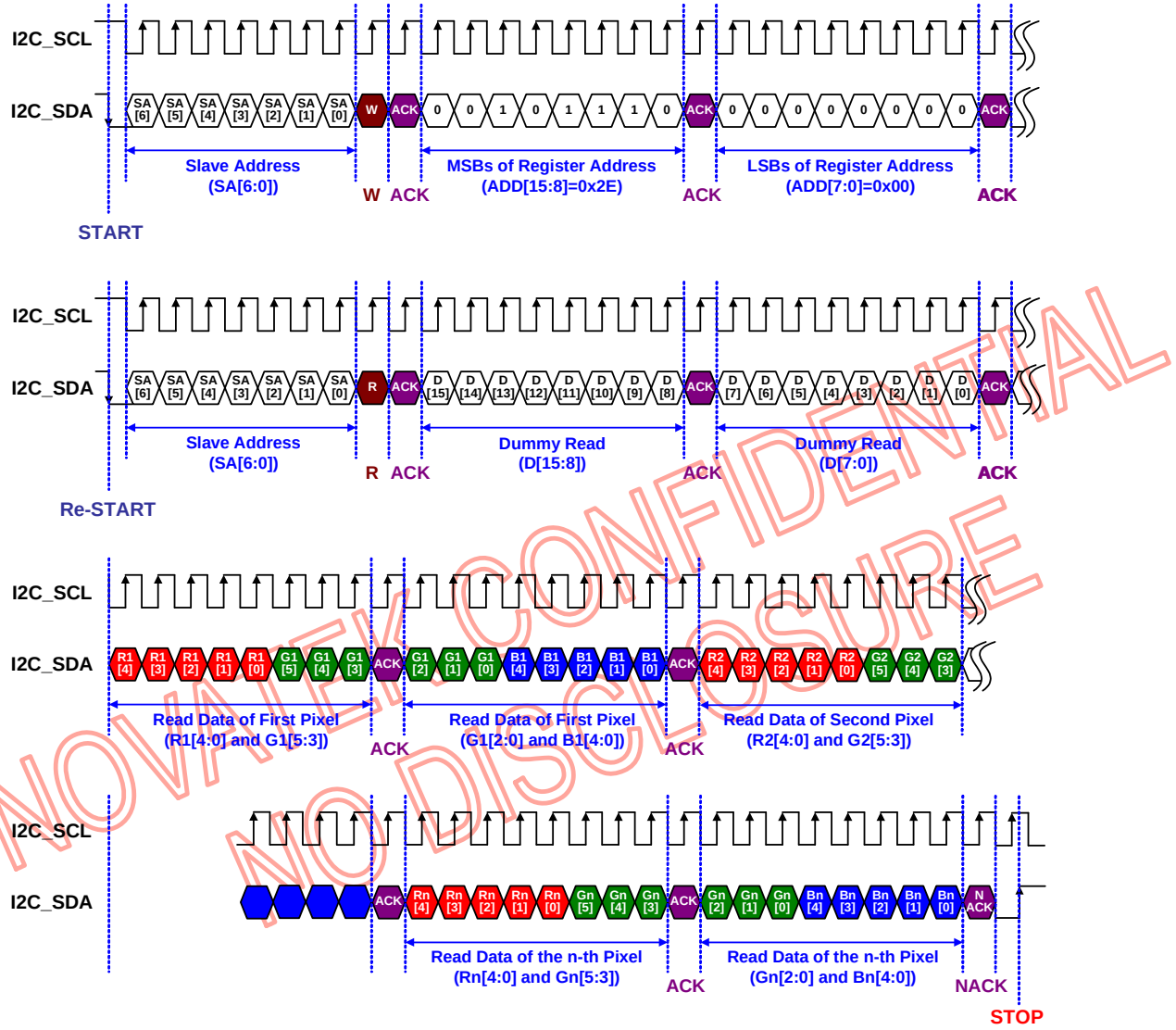
5.2.5 RAM Data Read Sequence of I2C Interface

NT35510 supports RAM data read function for I2C interface.

The master MCU need to send the RAM address of reading first and transfer protocol can refer to the 5.2.3 Register Write Sequence. Then the master MCU need to send the RAM data read register "2E00h" to NT35510. And finally, the MCU can send the following RAM data reading timing to feedback single RAM data value by one complete I2C packet.

The RAM data reading timing is shown in below.

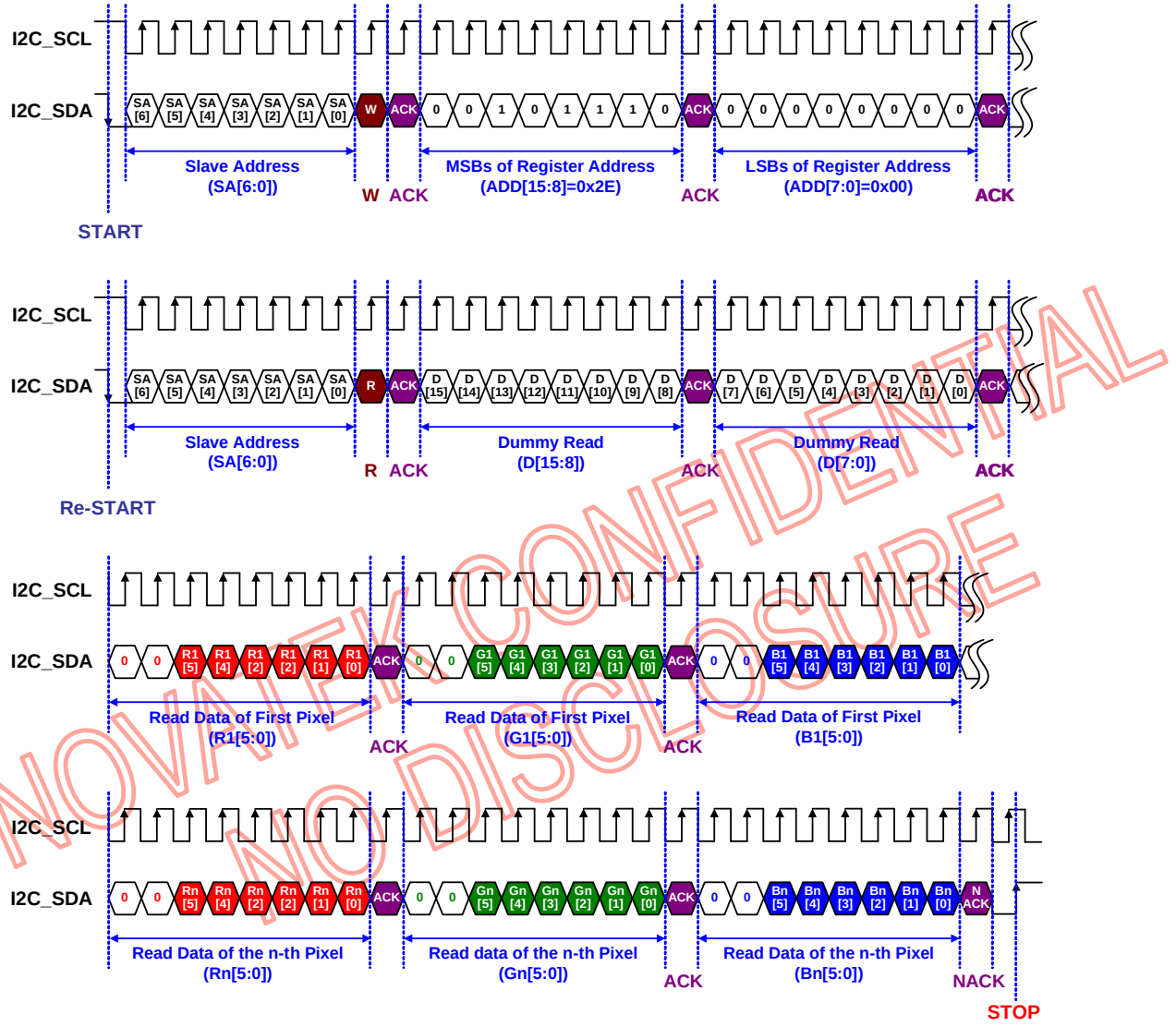
- 65K colors, RGB is 5-6-5-bit pixel data output (parameter of command 3A00h is 0x0005)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[4:0], R2[4:0], , Rn[4:0]: The red color data of each pixel
G1[5:0], G2[5:0], , Gn[5:0]: The green color data of each pixel
B1[4:0], B2[4:0], , Bn[4:0]: The blue color data of each pixel

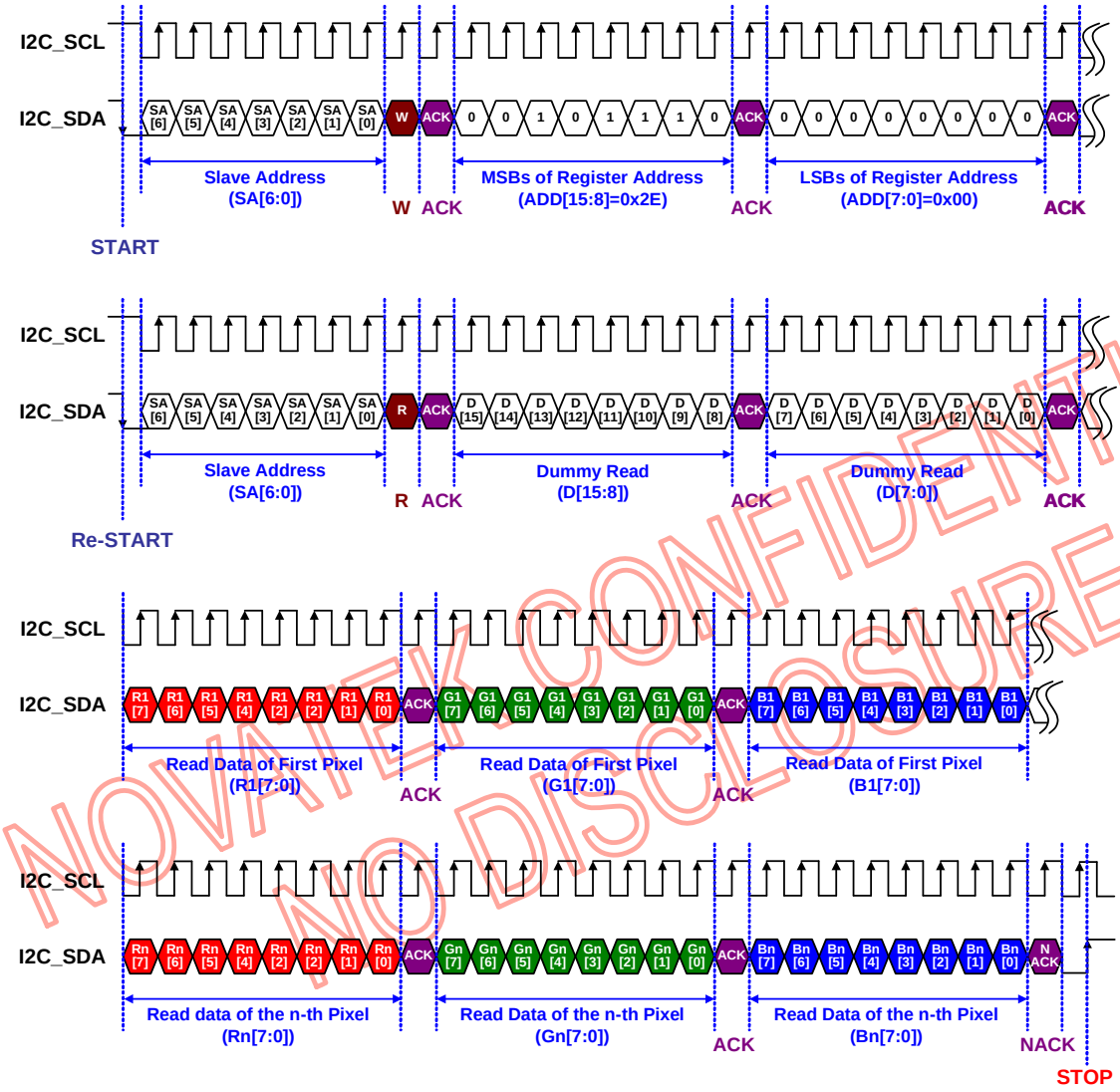
- 262K colors, RGB is 6-6-6-bit pixel data output (parameter of command 3A00h is 0x0006)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[5:0], R2[5:0], , Rn[5:0]: The red color data of each pixel
G1[5:0], G2[5:0], , Gn[5:0]: The green color data of each pixel
B1[5:0], B2[5:0], , Bn[5:0]: The blue color data of each pixel

- 16.7M colors, RGB is 8-8-8-bit pixel data output (parameter of command 3A00h is 0x0007)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[7:0], R2[7:0], , Rn[7:0]: The red color data of each pixel
G1[7:0], G2[7:0], , Gn[7:0]: The green color data of each pixel
B1[7:0], B2[7:0], , Bn[7:0]: The blue color data of each pixel

5.3 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

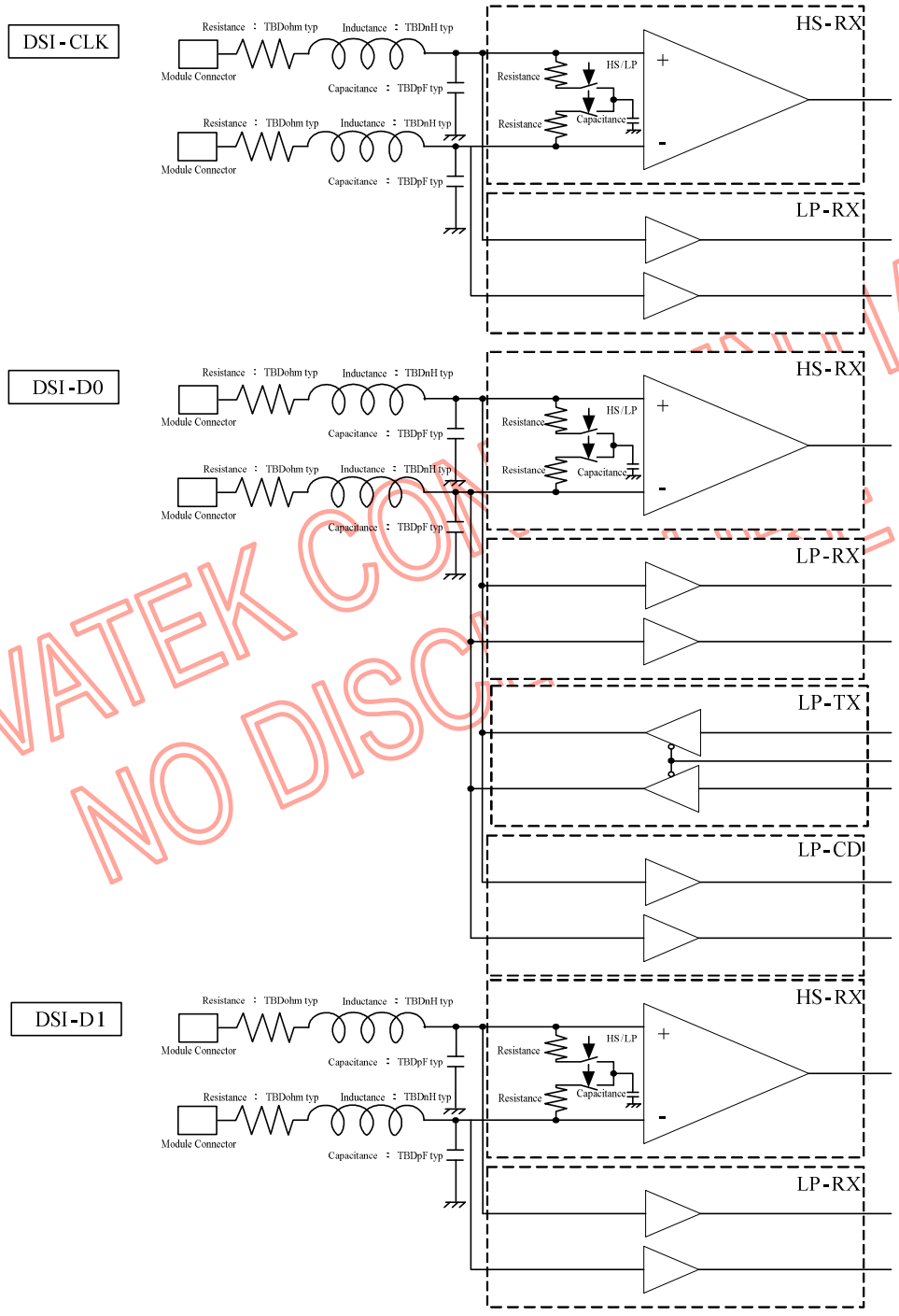
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1	Unidirectional Lane ■ Forward High-Speed ■ Escape Mode (ULPM only) ■ No LPDT

5.3.1 Display Module Pin Configuration for DSI



5.3.2 Display Serial Interface (DSI)

5.3.2.1 GENERAL DESCRIPTION

Communication sequences between the MCU and the display module are described on chapter “5.3.2.3.3 Communication Sequences”.

The communication can be separated 2 different levels between the MCU and the display module:

- Low level communication what is done on the interface level
- High level communication what is done on the packet level

5.3.2.2 INTERFACE LEVEL COMMUNICATION

5.3.2.2.1 GENERAL

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dn+ -line	Dn- -line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

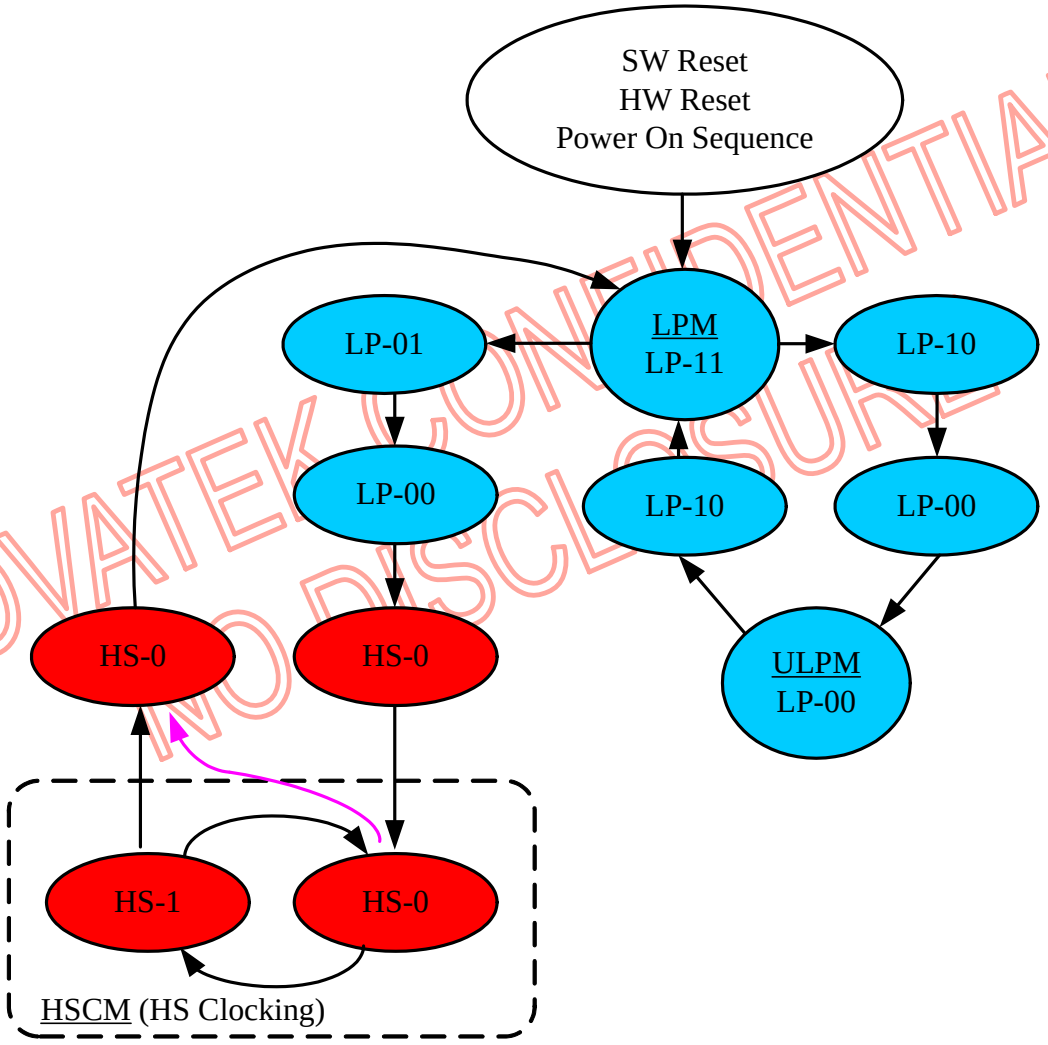
NOTES:

1. *Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.*
2. *If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.*

5.3.2.2.2 DSI-CLK LANES

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principle flow chart of the different clock lanes power modes is illustrated below.

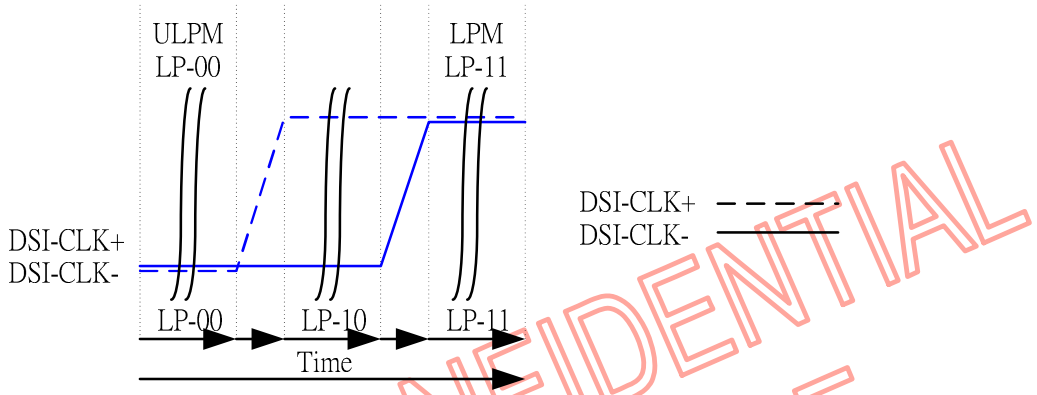


Clock Lanes Power Mode

5.3.2.2.2.1 LOW POWER MODE (LPM)

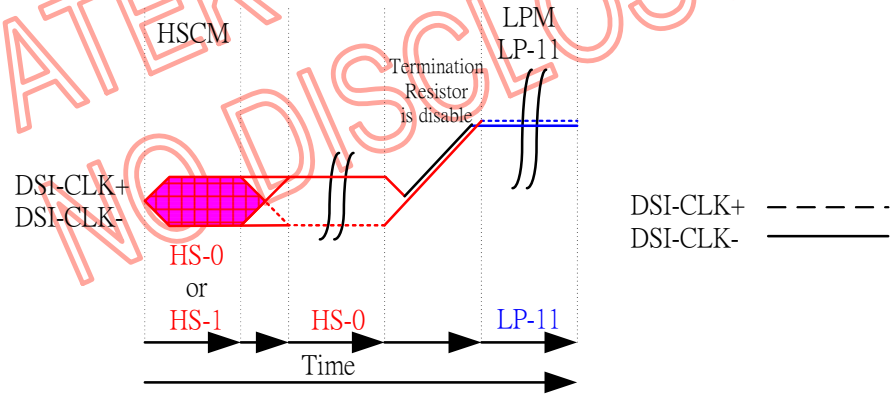
DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11
2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



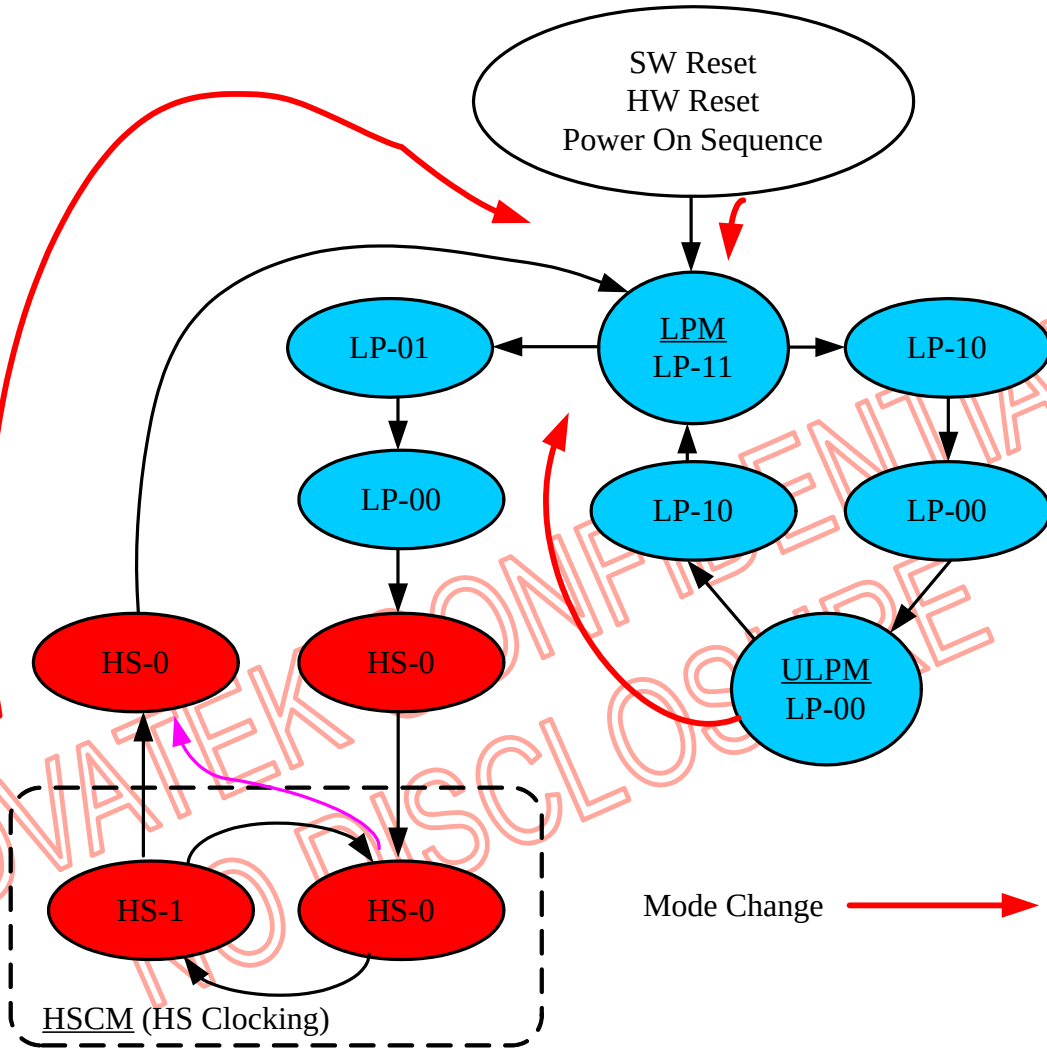
From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.



From High Speed Clock Mode (HSCM) to LPM

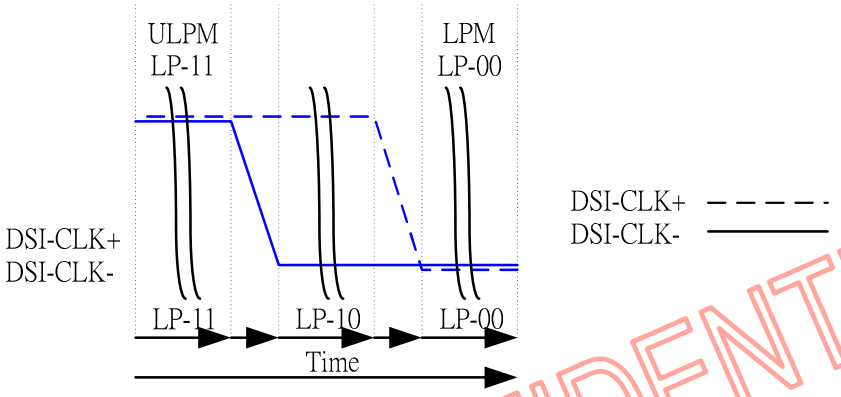
All three mode changes are illustrated a flow chart below.



All Three Mode Change to LPM on the Flow Chart

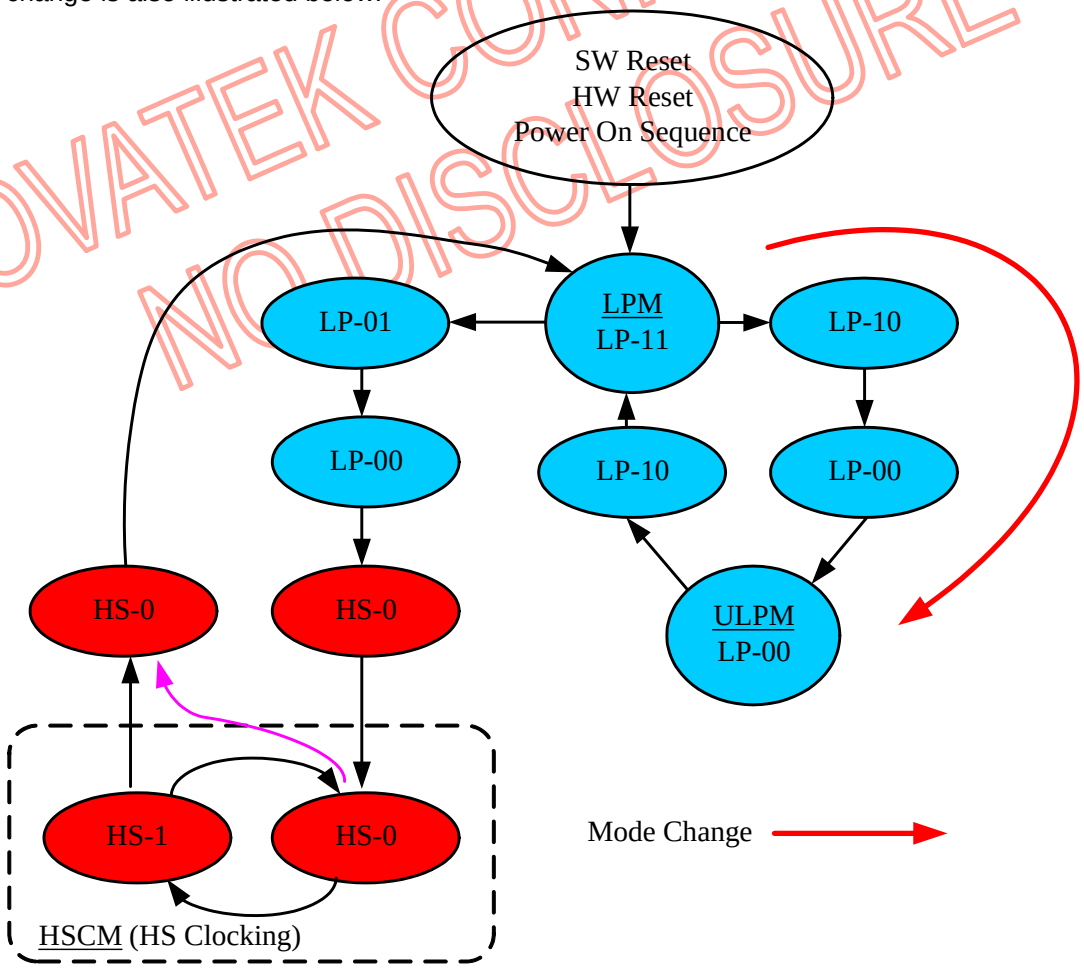
5.3.2.2.2.2 ULTRA LOW POWER MODE (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.



From LPM to ULPM

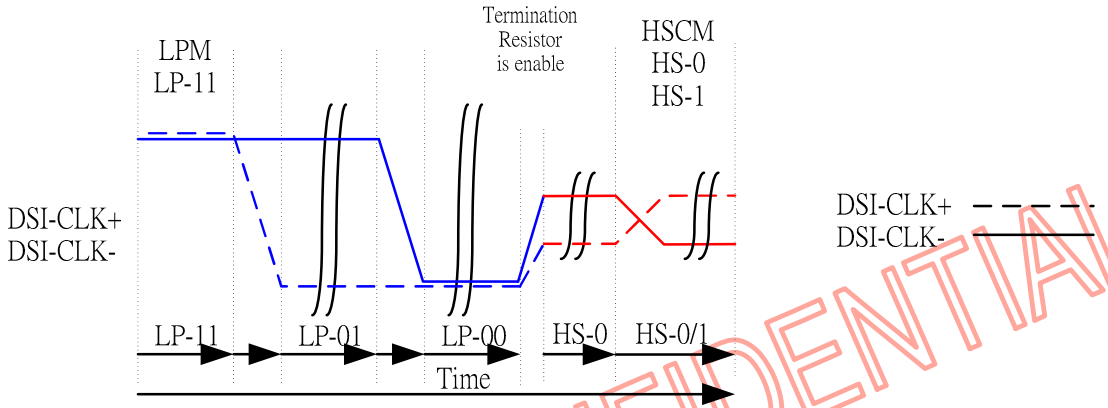
The mode change is also illustrated below.



Mode Change from LPM to ULPM on the Flow Chart

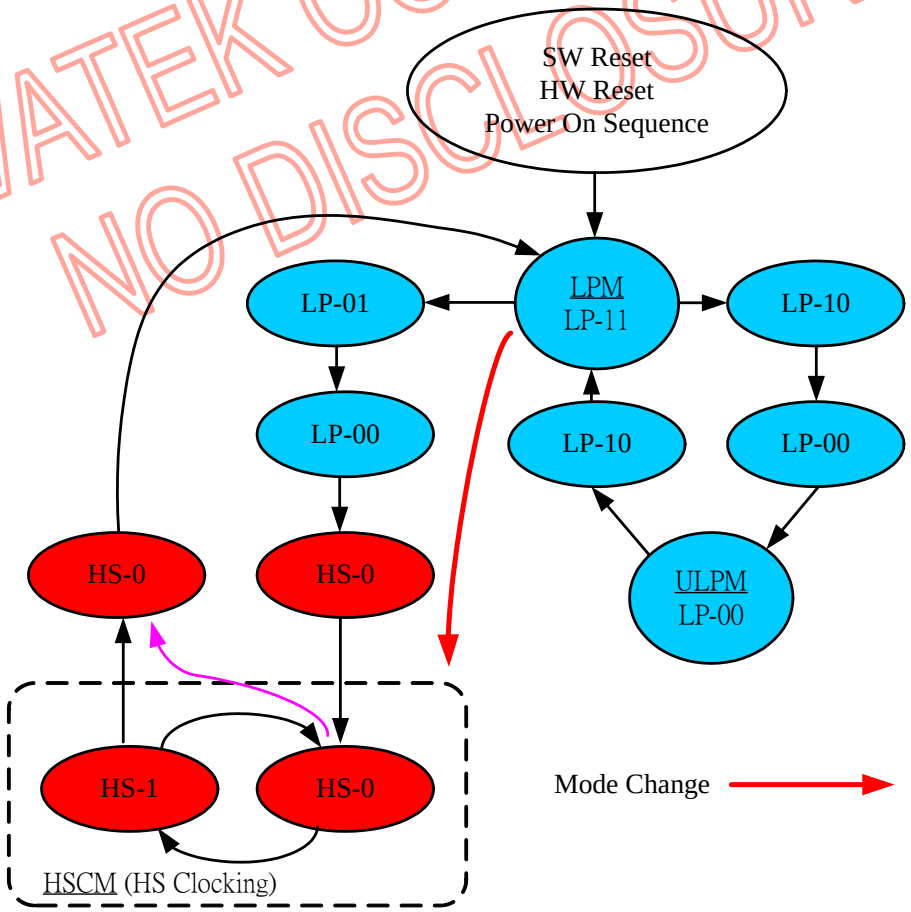
5.3.2.2.2.3 HIGH SPEED CLOCK MODE (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



From LPM to HSCM

The mode change is also illustrated below.

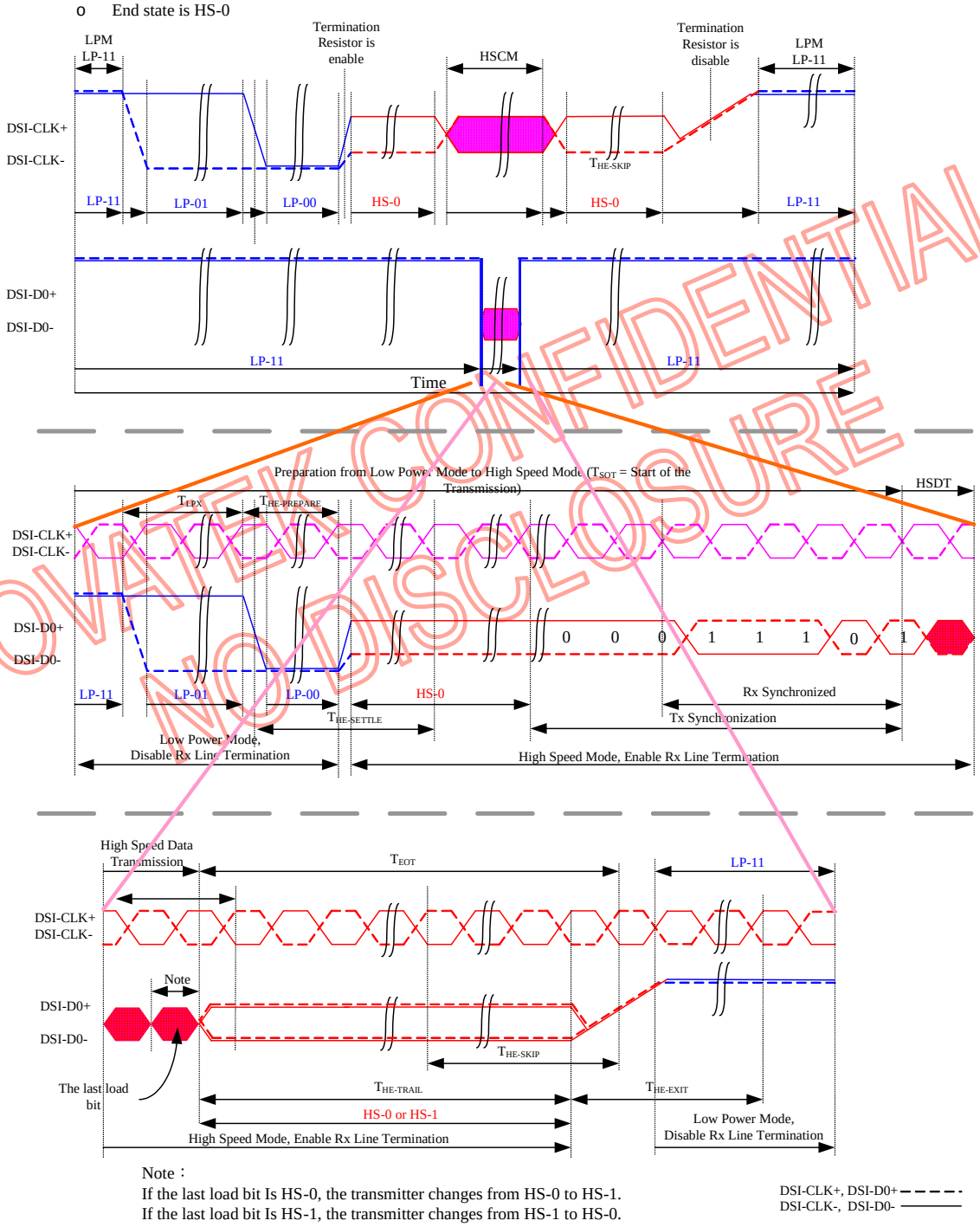


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of：

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note：
If the last load bit Is HS-0, the transmitter changes from HS-0 to HS-1.
If the last load bit Is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-D0+ – – – –
DSI-CLK-, DSI-D0- ————

High Speed Clock Burst

5.3.2.2.3 DSI-DATA LANES

5.3.2.2.3.1 GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Notes:

1. DSI-D0+/- data lanes are used.

2. More information on section "Bus Turnaround (BTA)"

5.3.2.2.3.2 ESCAPE MODES

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

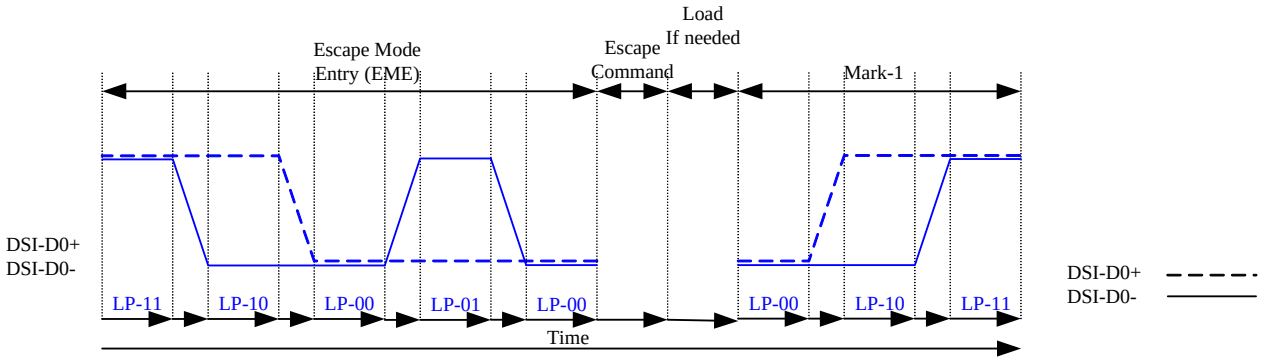
These Escape Modes are used to:

- Send "Low-Power Data Transmission" (LPDT) e.g. from the MCU to the display module
- Drive data lanes to "Ultra-Low Power State" (ULPS)
- Indicate "Remote Application Reset" (RAR), which is reset the display module
- Indicate "Tearing Effect" (TEE), which is used for a TE trigger event from the display module to the MCU
- Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	$1110\ 0001_{bin}$		X
Ultra-Low Power Mode	Mode	$0001\ 1110_{bin}$	X	X
Underfined-1, Note 1	Mode	$1001\ 1111_{bin}$	-	-
Underfined-2, Note 1	Mode	$1101\ 1110_{bin}$	-	-
Remote Application Reset	Trigger	$0110\ 0010_{bin}$	-	X
Tearing Effect	Trigger	$0101\ 1101_{bin}$	-	X
Acknowledge	Trigger	$0010\ 0001_{bin}$	-	X
Unknow-5, Note 1	Trigger	$1010\ 0000_{bin}$	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "X"=Supported

4. "-"=Not Supported

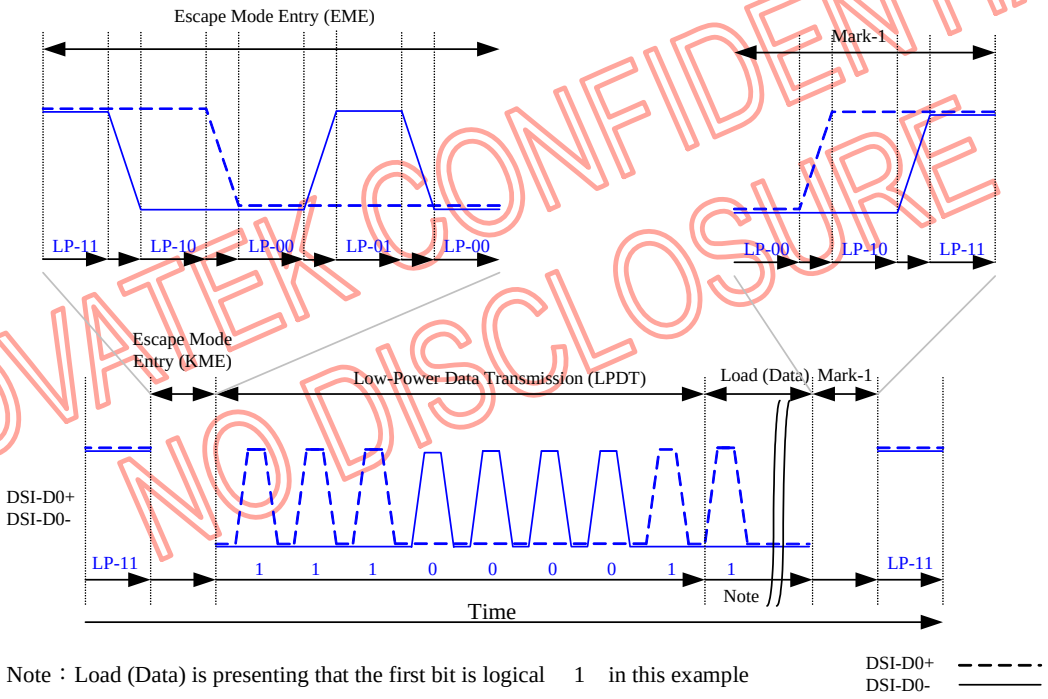
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

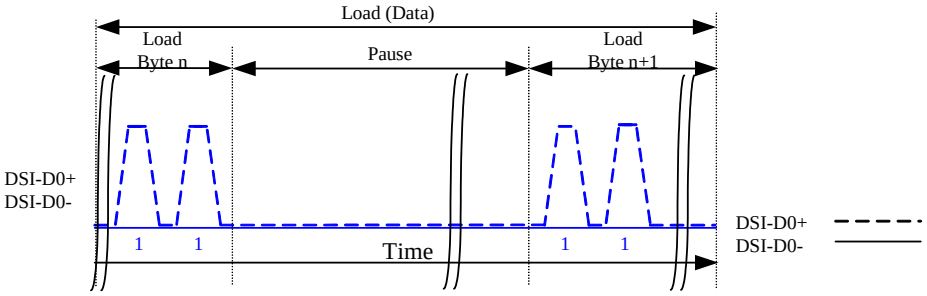
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
    - One or more bytes (8 bit)
    - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Low-Power Data Transmission (LPDT)



Pause (Example)

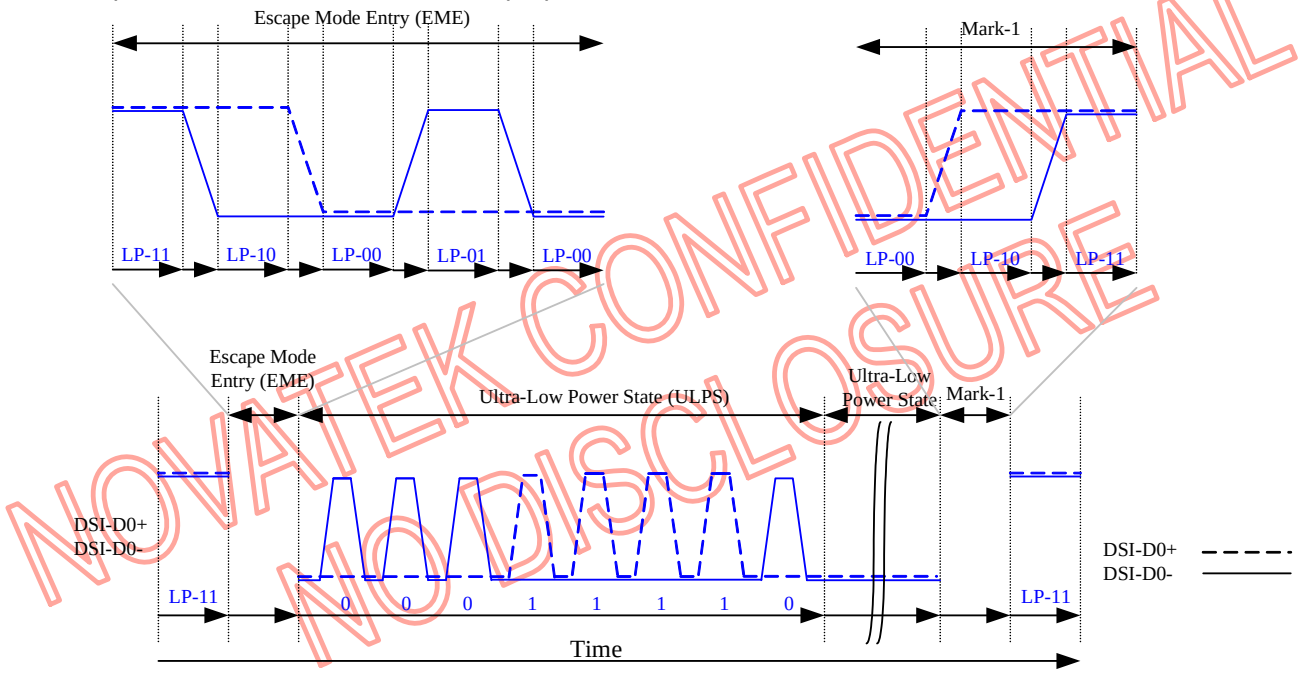
Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

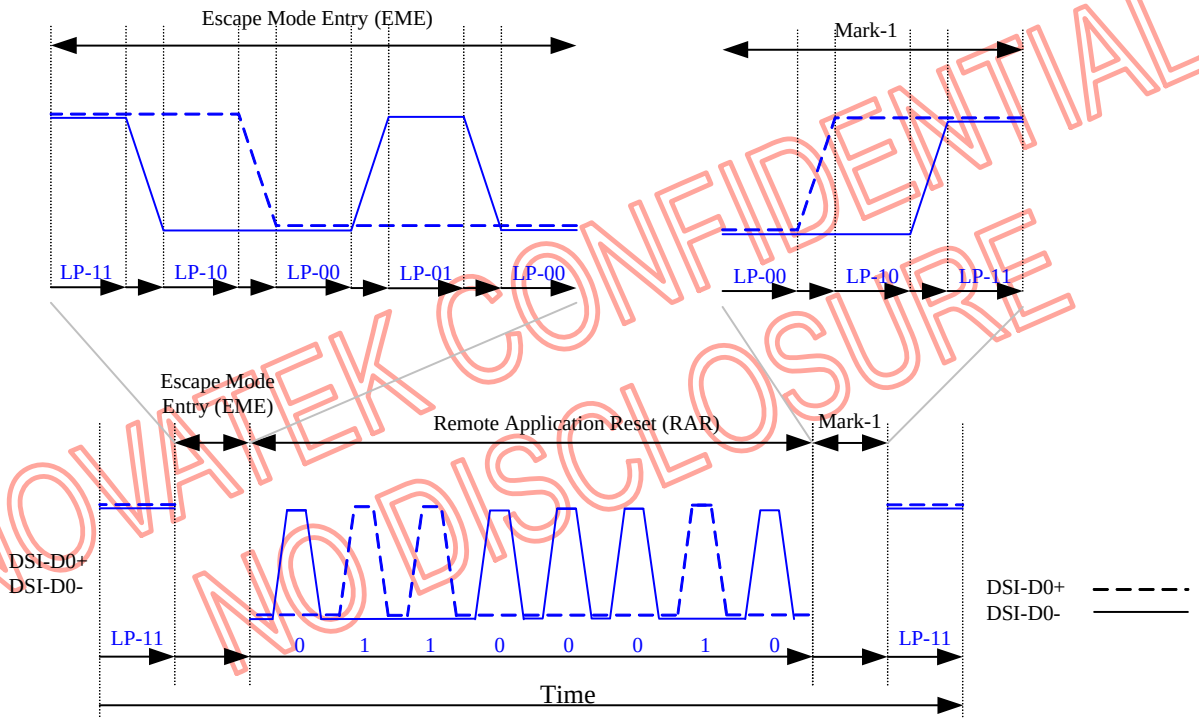
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

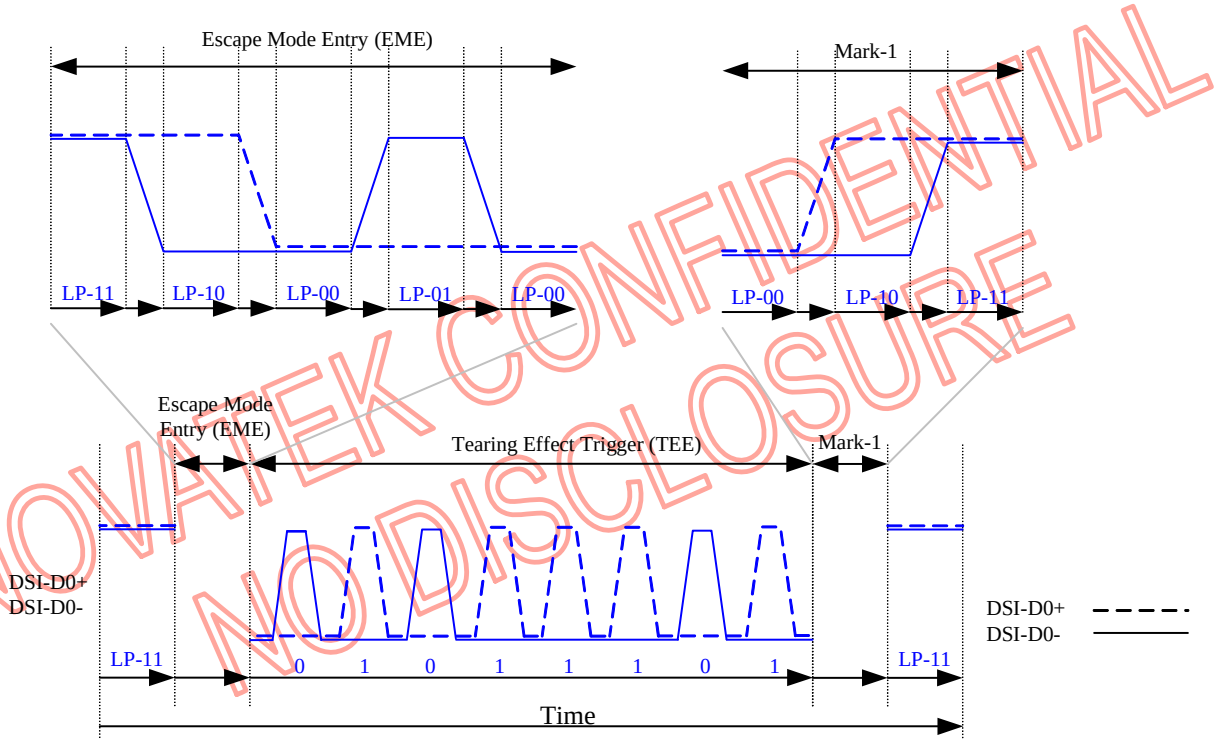
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

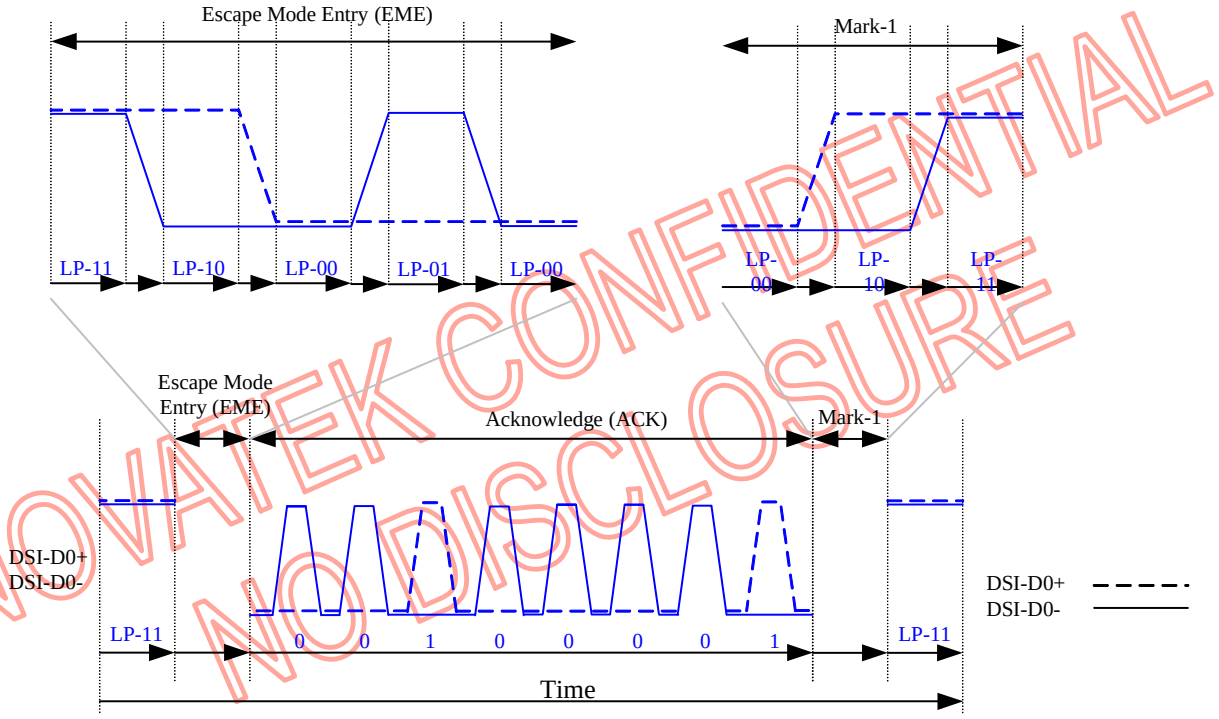
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

5.3.2.2.3.3 HIGH SPEED DATA TRANSMISSION (HSDT)

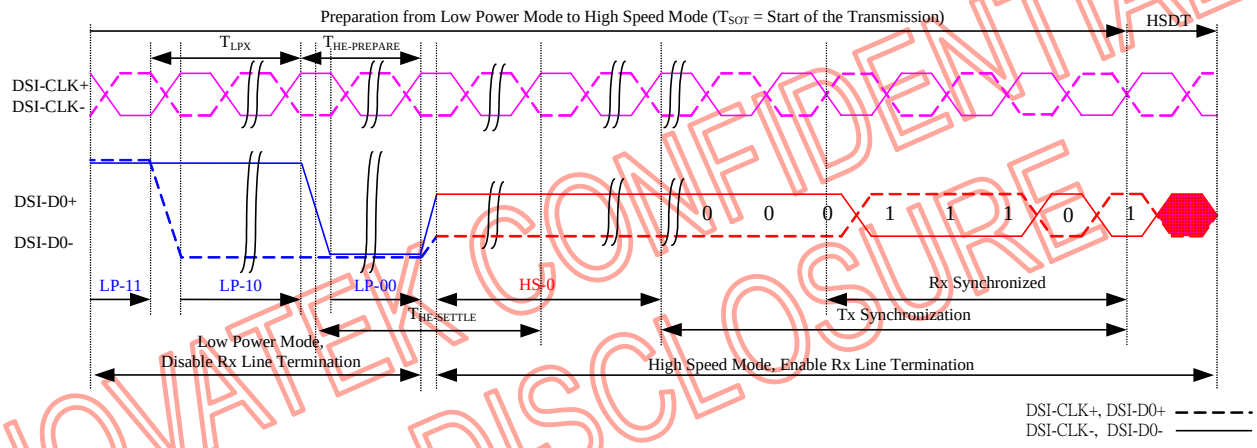
Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "5.3.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

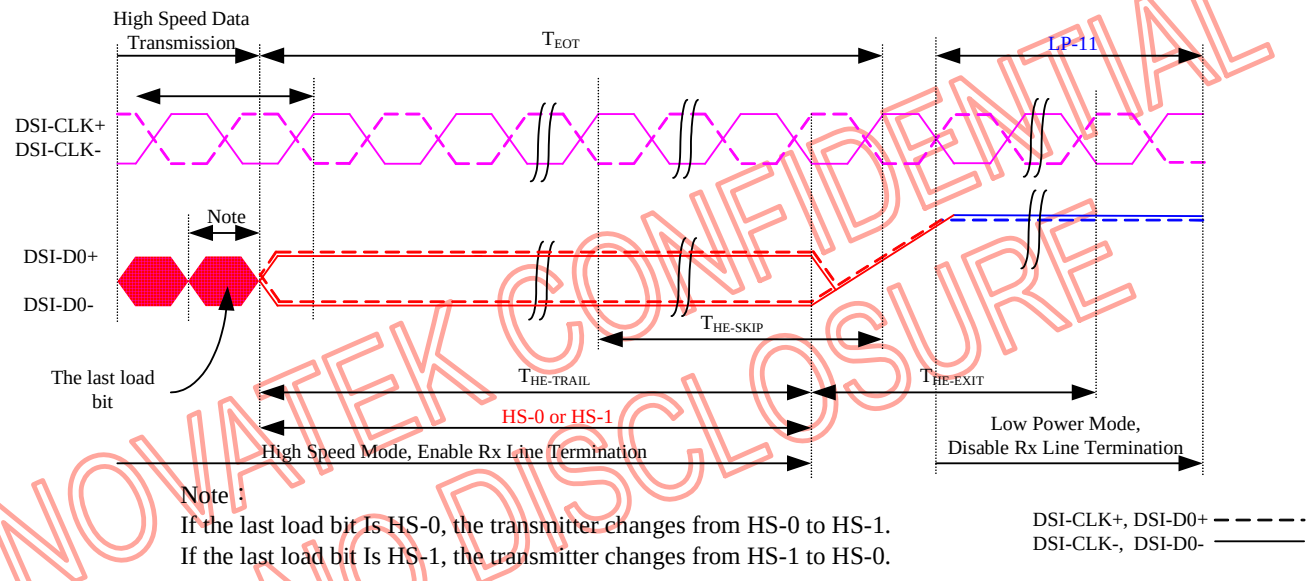
Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “5.3.2.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



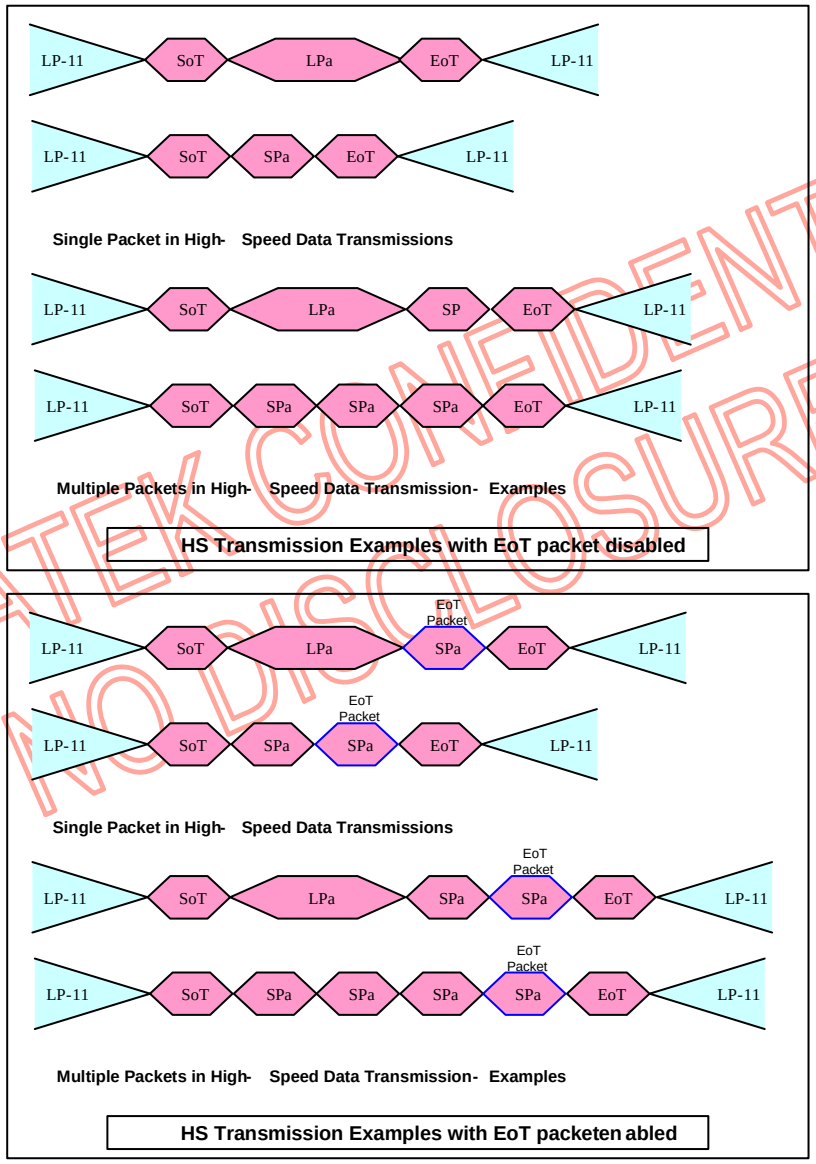
Note：
If the last load bit Is HS-0, the transmitter changes from HS-0 to HS-1.
If the last load bit Is HS-1, the transmitter changes from HS-1 to HS-0.

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “5.1.9.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are’1’s (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

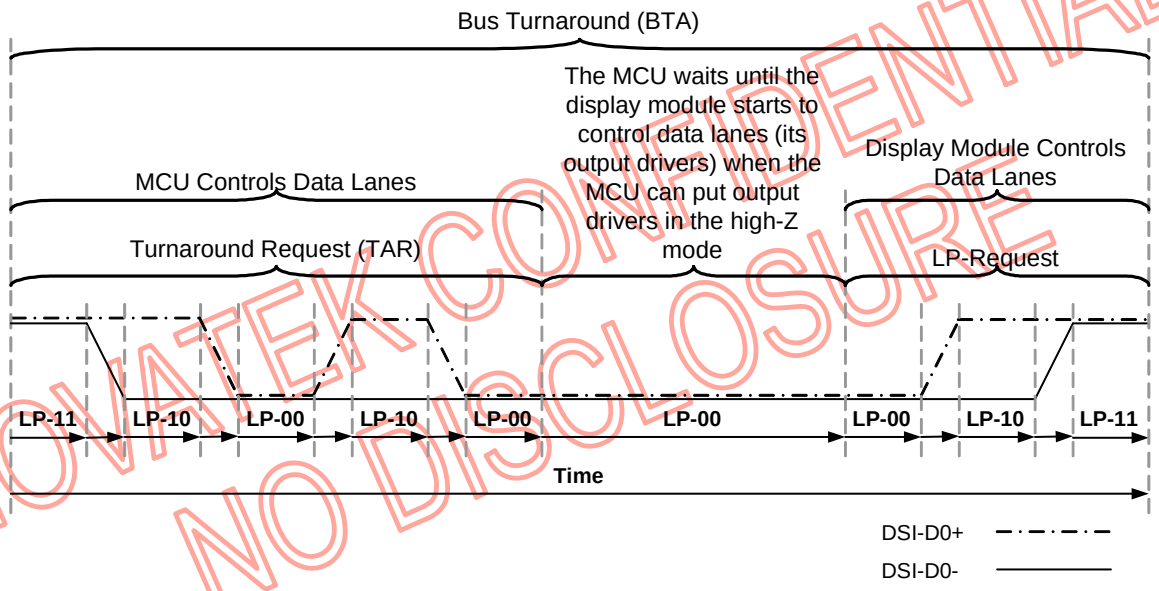
Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

- Start (MCU):LP-11
- Turnaround Request (MCU): LP-11 → LP-10 → LP-00 → LP-10 → LP-00
- The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)
- The display module changes to the stop mode: LP-00 → LP-10 → LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

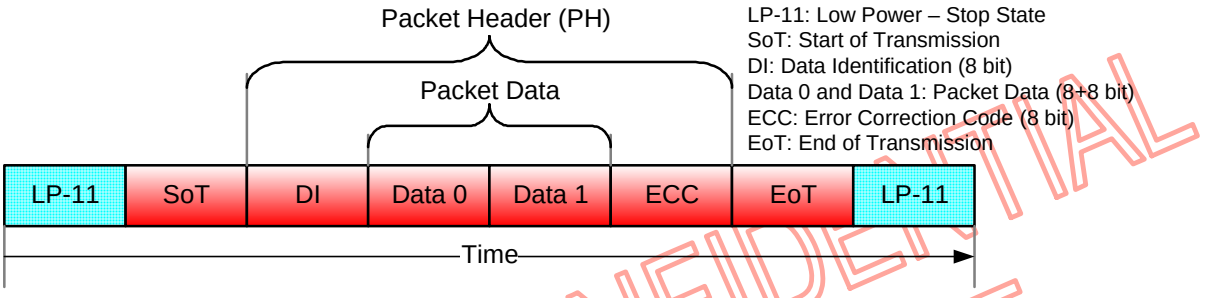
5.3.2.3 PACKET LEVEL COMMUNICATION

5.3.2.3.1 SHORT PACKET (SPa) AND LONE PACKET (LPa) STRUCTURE

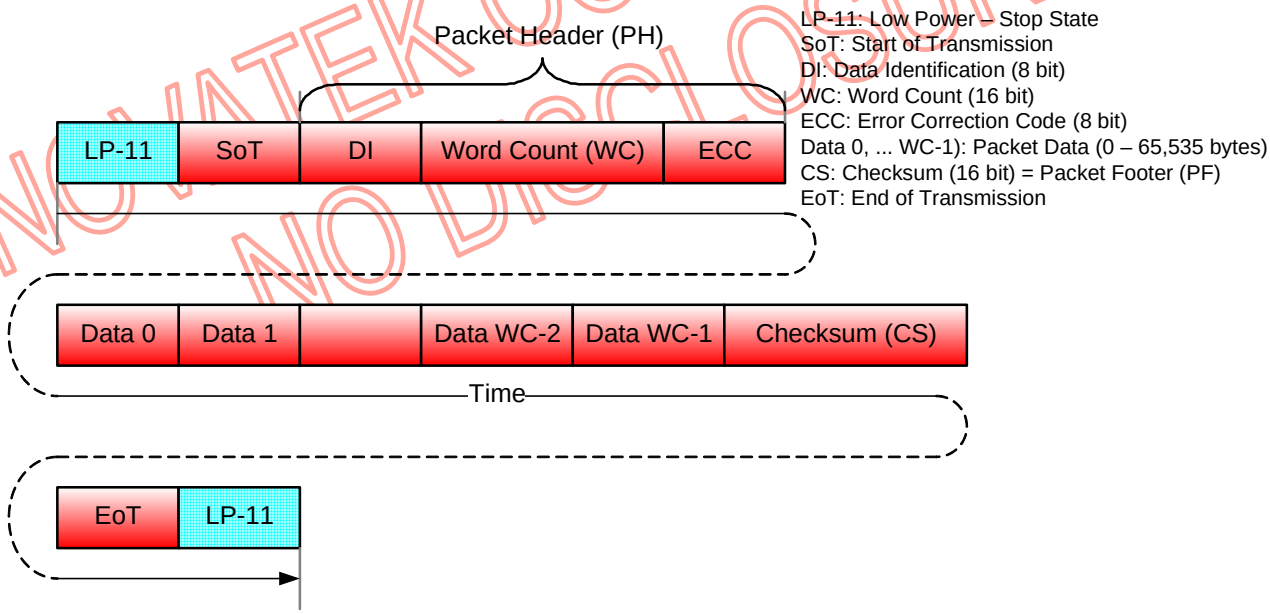
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Short Packet (SPa) Structure



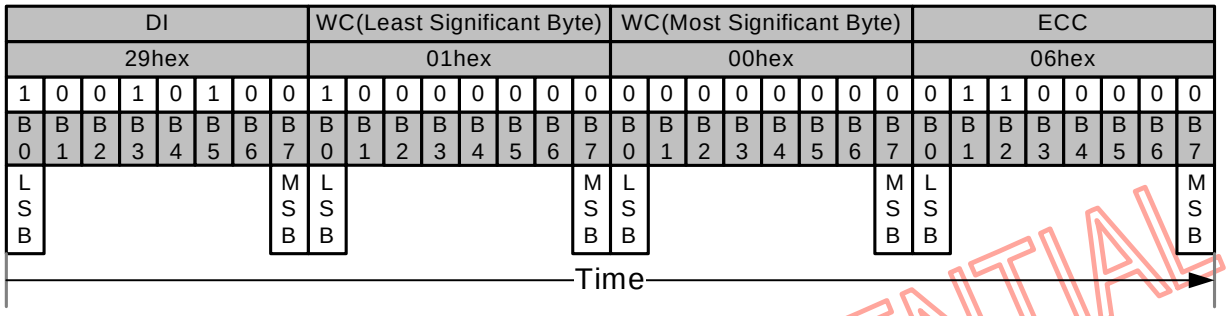
Long Packet (LPa) Structure

Note:
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.
* LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
* LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
* LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.3.2.3.1.1 BIT ORDER OF THE BYTE ON PACKETS

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

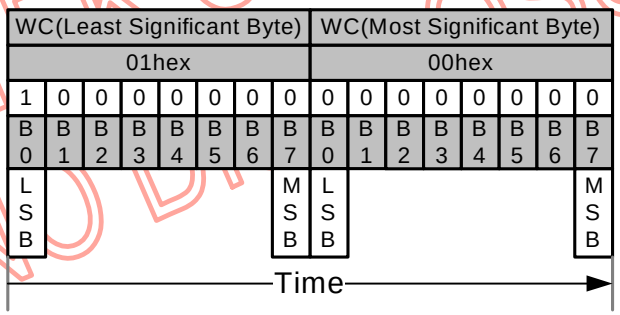


Bit Order of the Byte on Packets

5.3.2.3.1.2 BIT ORDER OF THE MULTIPLE BYTE INFORMATION ON PACKETS

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.



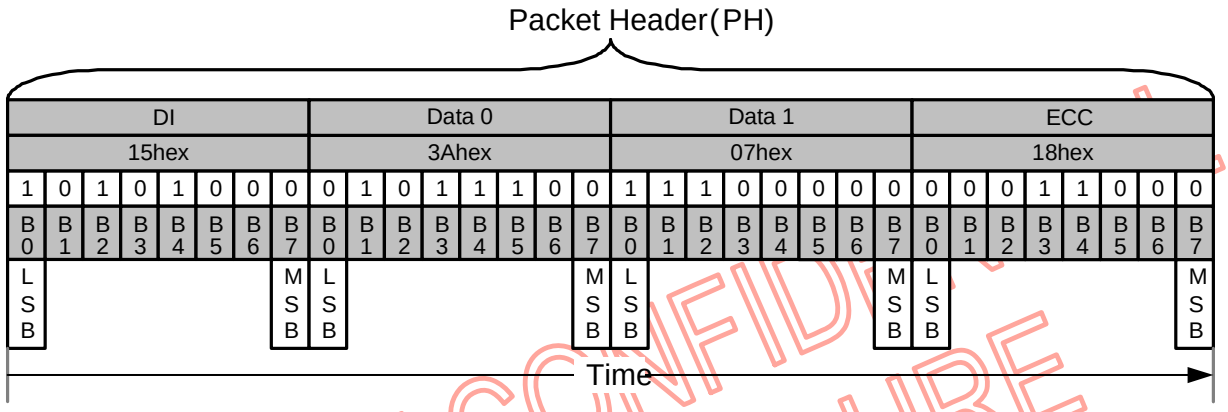
Byte Order of the Multiple Byte on Packets

5.3.2.3.1.3 PACKET HEADER (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

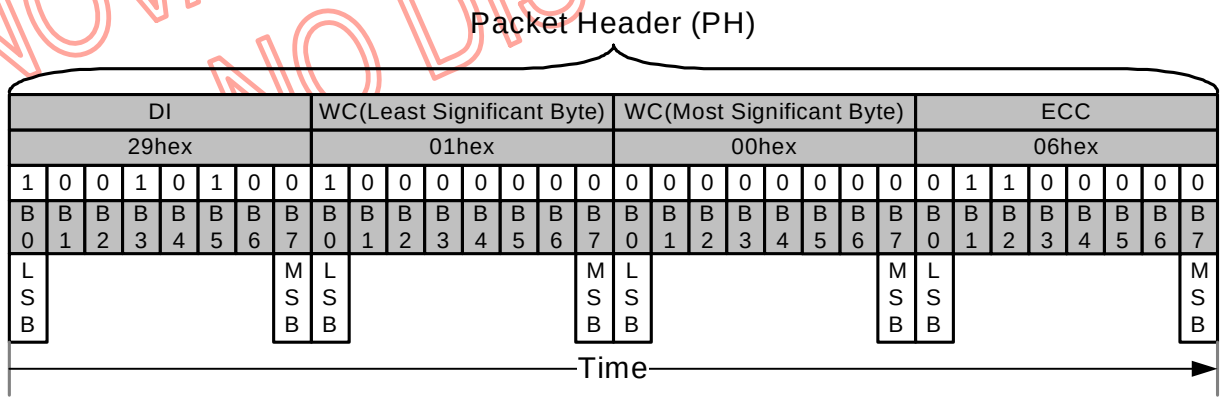
- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

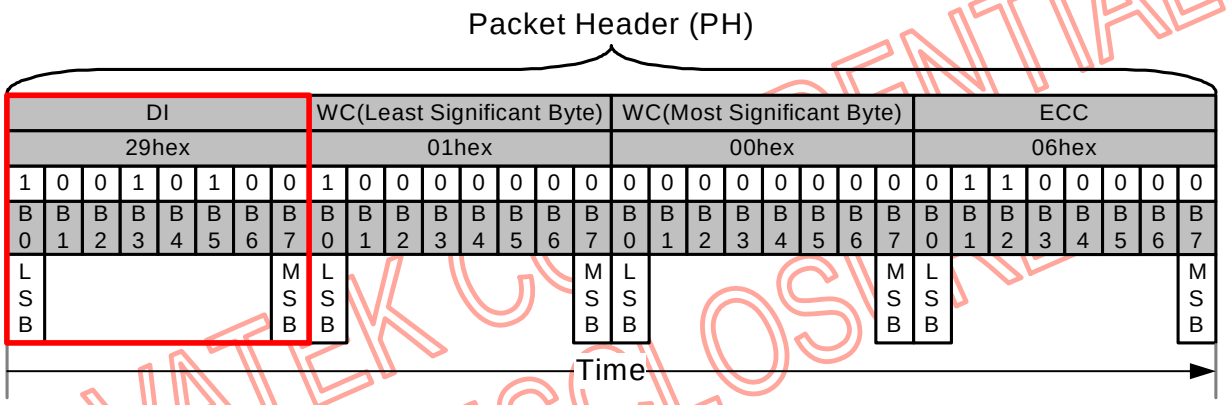
Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:
- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

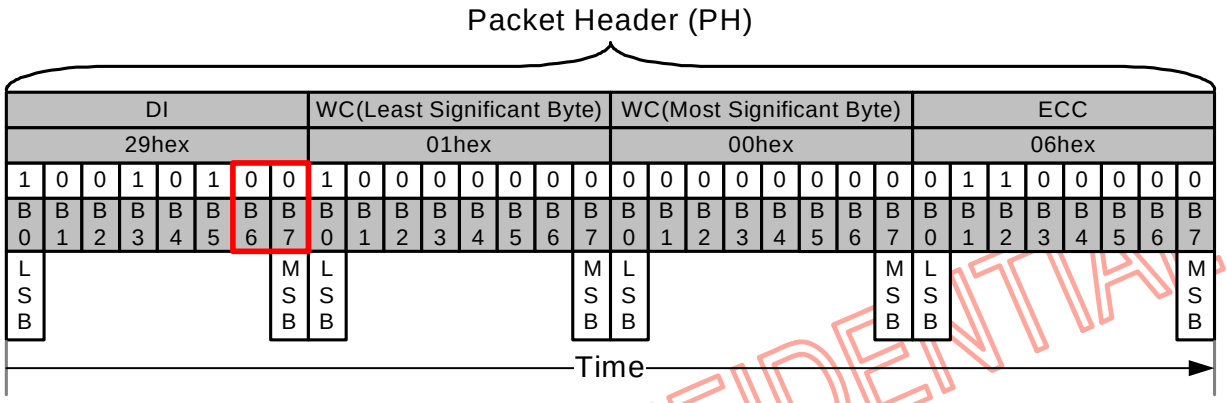


Data Identification (DI) on the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

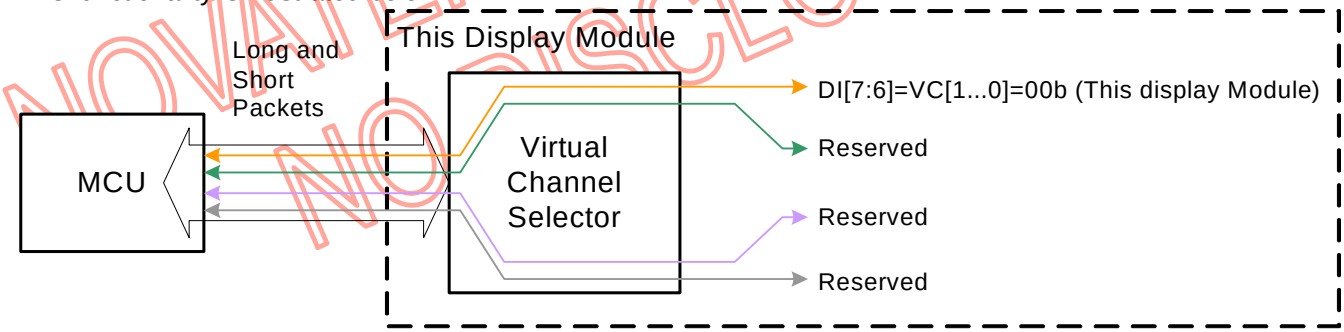


Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration

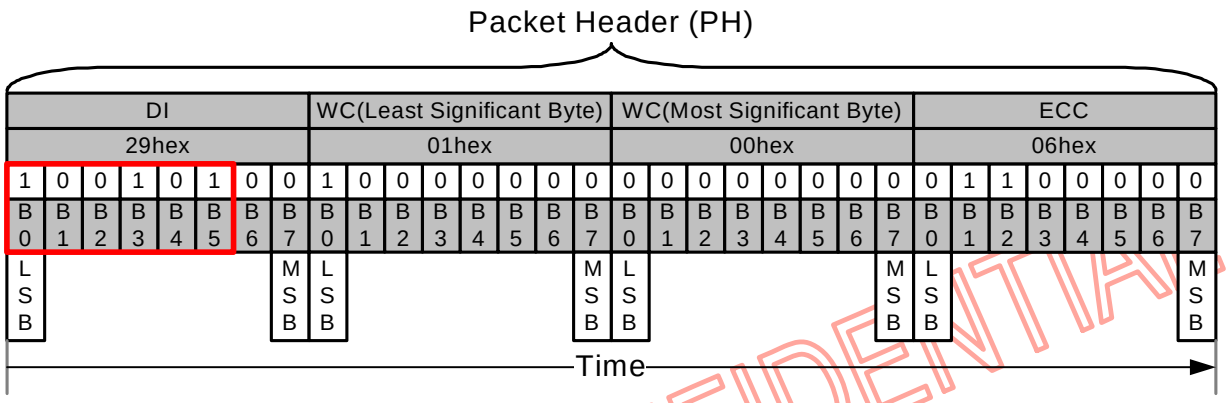
Virtual Channel (VC) always 0 (D[7...6]=VC[1…0]000b) when the MCU is sending “End of Transmission Packet” to the display module. See section “End of Transmission Packet (EoTP)

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1…0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type Hex	Data Type Binary	Description	Packet Size	Note
08h	00 1000	End of Transmission packet	Short	1
05h	00 0101	DCS WRITE, no parameters	Short	
15h	01 0101	DCS WRITE, 1 parameter	Short	
06h	00 0110	DCS READ, no parameters	Short	
37h	11 0111	Set Maximum Return Packet Size	Short	
09h	00 1001	Null Packet, no data	Long	2
19h	01 1001	Blanking Packet, no data	Long	2
39h	11 1001	DCS Long Write/Write_LUT Command Packet	Long	
01h	00 0001	Sync Event, V Sync Start	Short	7
11h	01 0001	Sync Event, V Sync End	Short	7
21h	10 0001	Sync Event, H Sync Start	Short	7
31h	11 0001	Sync Event, H Sync End	Short	7
02h	00 0010	Color mode (CM) Off Command	Short	7
12h	01 0010	Color mode (CM) On Command	Short	7
22h	10 0010	Shut Down Peripheral Command	Short	7
32h	11 0010	Turn On Peripheral Command	Short	7
13h	01 0011	Generic Short Write, 1 parameter	Short	3,4,8
23h	10 0011	Generic Short Write, 2 parameter	Short	3,5,8
29h	10 1001	Generic Long Write	Long	3,8
14h	01 0100	Generic Read, 1 parameter	Short	3,4,8
0Eh	00 1110	Packed Pixel Stream,16-bit RGB, 5-6-5 Format	Long	7
1Eh	01 1110	Packed Pixel Stream,18-bit RGB, 6-6-6 Format	Long	7
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB, 6-6-6 Format	Long	7
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long	7

Notes:

1. *This can be used when the MCU wants to secure that there is the end of transmission in High Speed Data Transmission (HSDT) mode.*
2. *This can be used when the data lanes are wanted to keep in High Speed Data Transmission (HSDT) mode.*
3. *The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).*
4. *Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.*
5. *Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.*
6. *The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.*
7. *The data type for Video Mode Communication: 01h, 11h, 21h, 31h, 02h,12h 22h, 32h, 0Eh, 1Eh, 2Eh, 3Eh will be disable (ignored packet) if bit DSIM of command B100h is set to "0".*
8. *The data type for Generic write/read: 13h, 23h, 29h, 14h will be disable (ignored packet) if bit DSIG of command B100h is set to "0".*

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU										
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Short/Lng Packet	Abbreviation	Note
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER	
1Ch	0	1	1	1	0	0	DCS Read Long Response	Long	DCSRR-L	
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1-S	
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2-S	
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L	Note
11h	0	1	0	0	0	1	Generic Read Short Response, 1 byte returned	Short	GENRR1-S	Note
12h	0	1	0	0	1	0	Generic Read Short Response, 2 byte returned	Short	GENRR2-S	Note

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Note: The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG of command B100h is set to “0”.

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

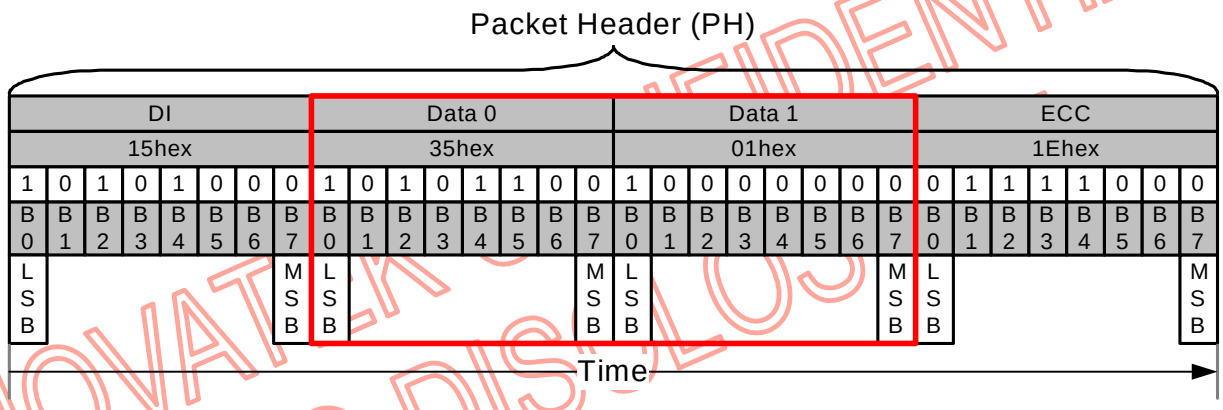
Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

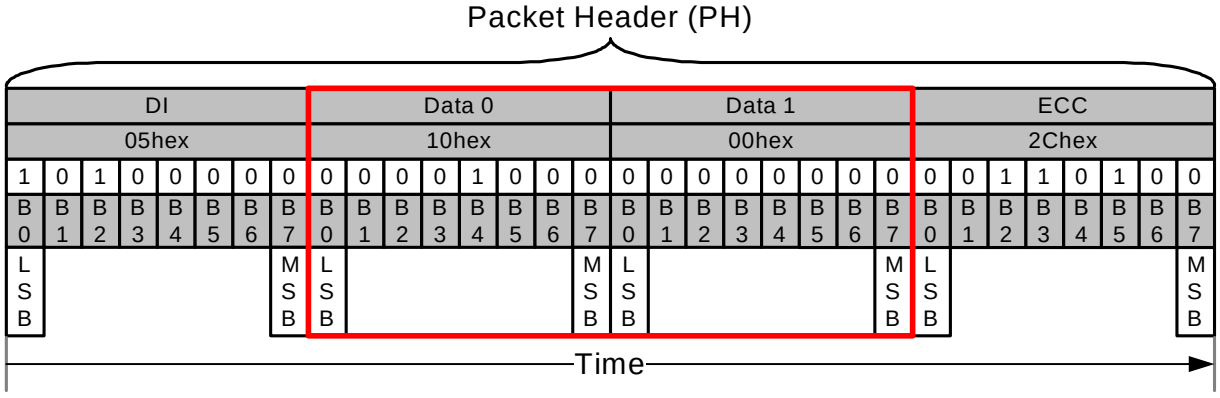
Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:
• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
• Data 1: 01hex (DCS's parameter)



Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:
• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
• Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

Word Count (WC) on the Long Packet (LPa)

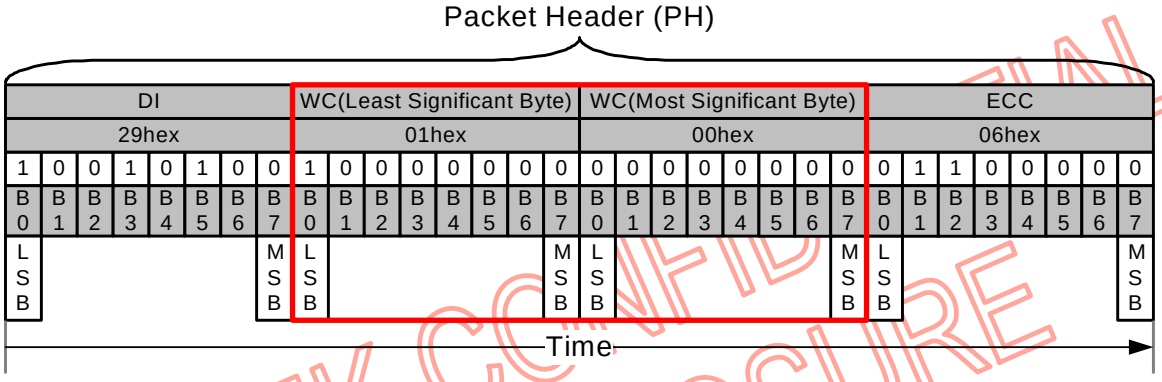
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

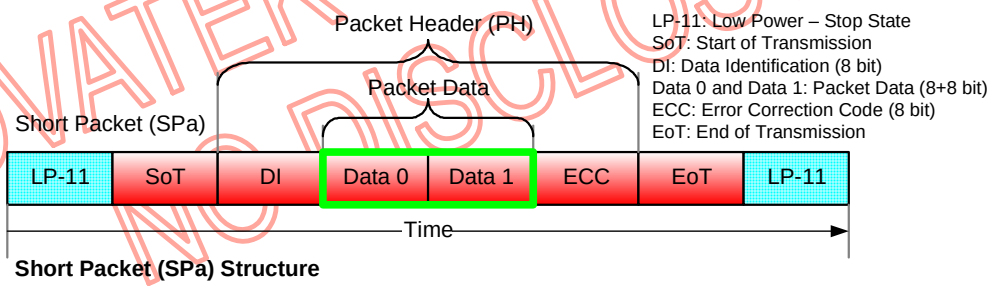
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

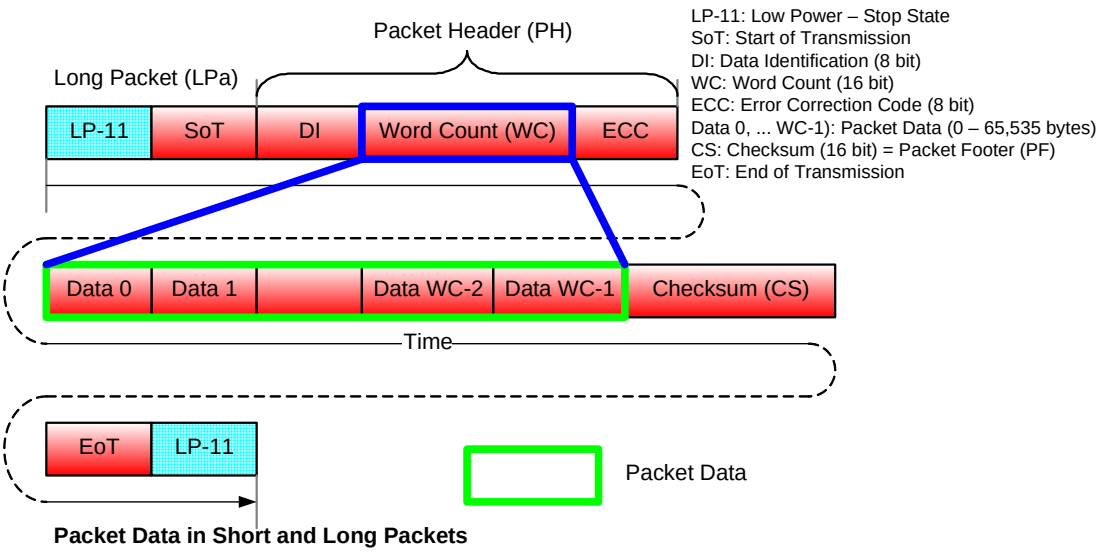
Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



Word Count (WC) on the Long Packet (LPa)



Short Packet (SPa) Structure



Packet Data in Short and Long Packets

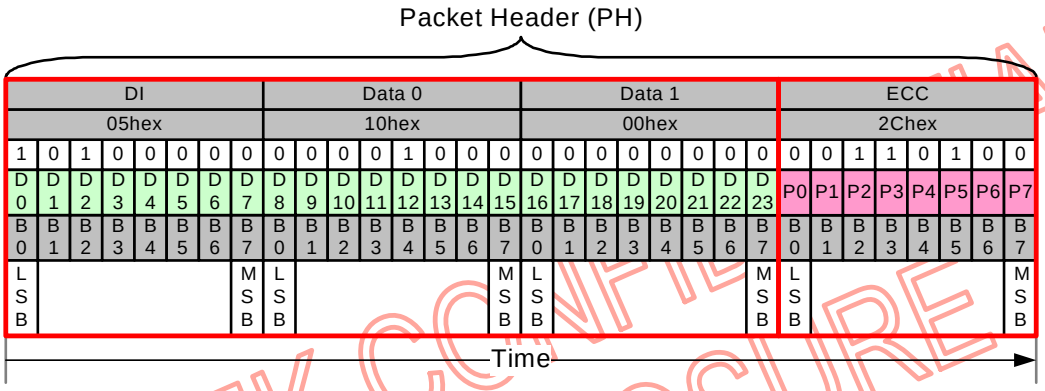
Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

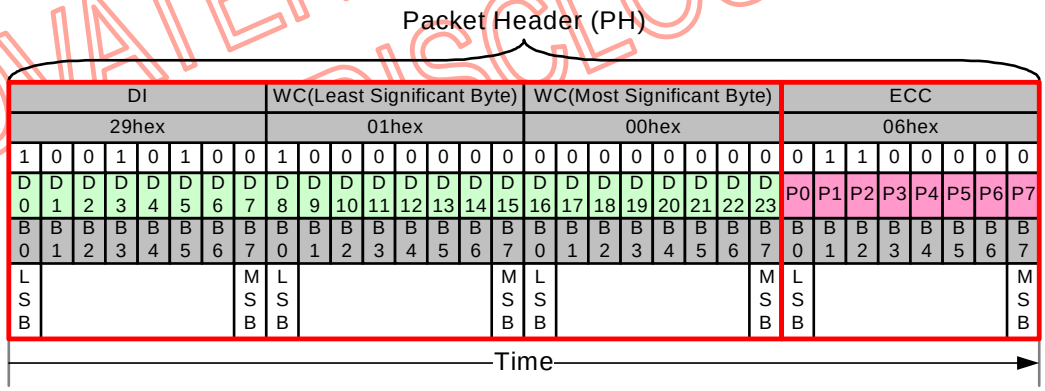
The ECC protects the following field"

- Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.



D[23…0] and P[7…0] on the Short Packet (SPa)



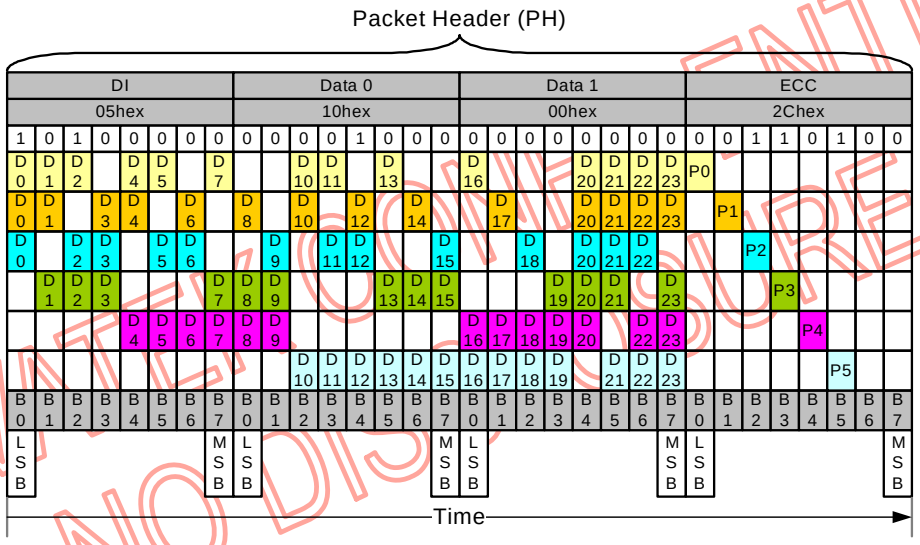
D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

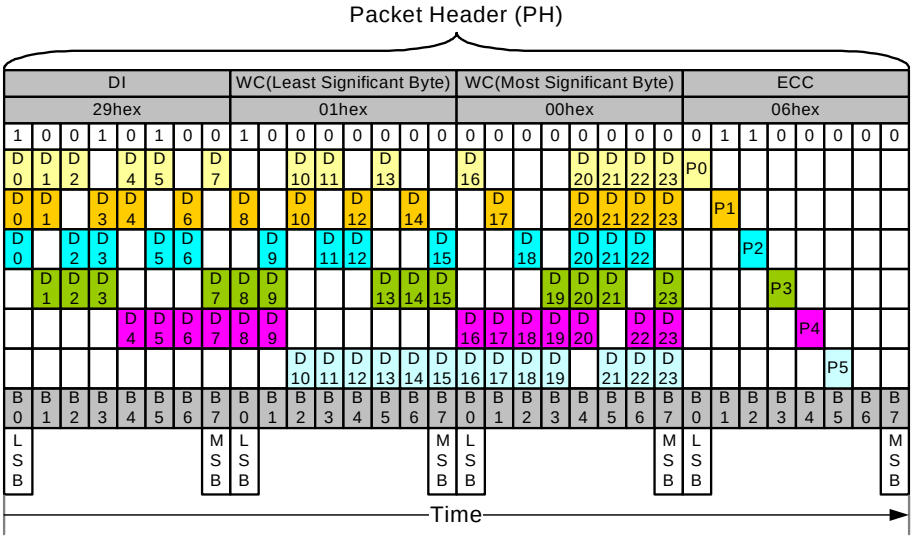
Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



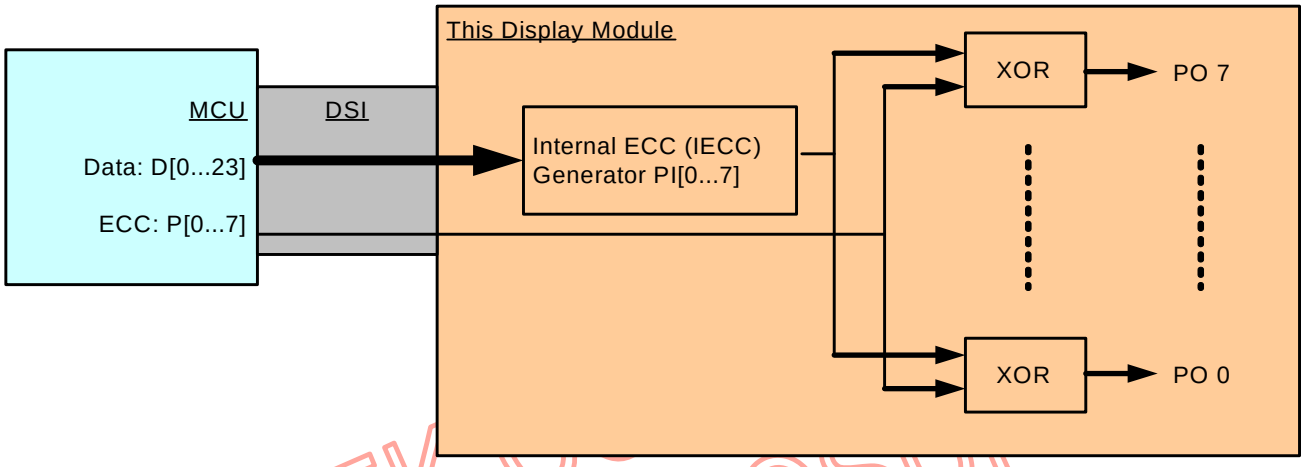
XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h => No Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch => Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

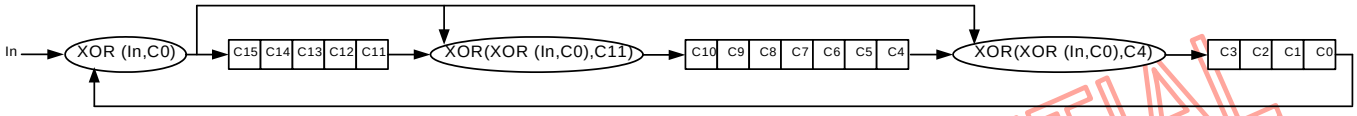
5.3.2.3.1.4 PACKET DATA (PD) ON THE LONG PACKET (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.3.2.3.1.5 PACKET FOOTER (PF) ON THE LONG PACKET (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

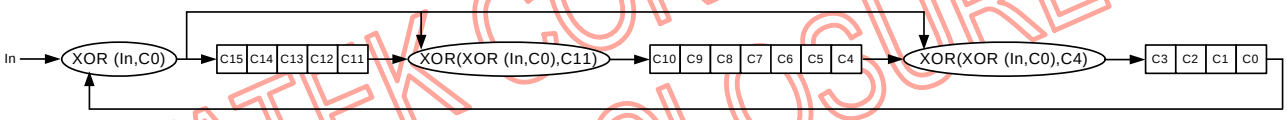
The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.



16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

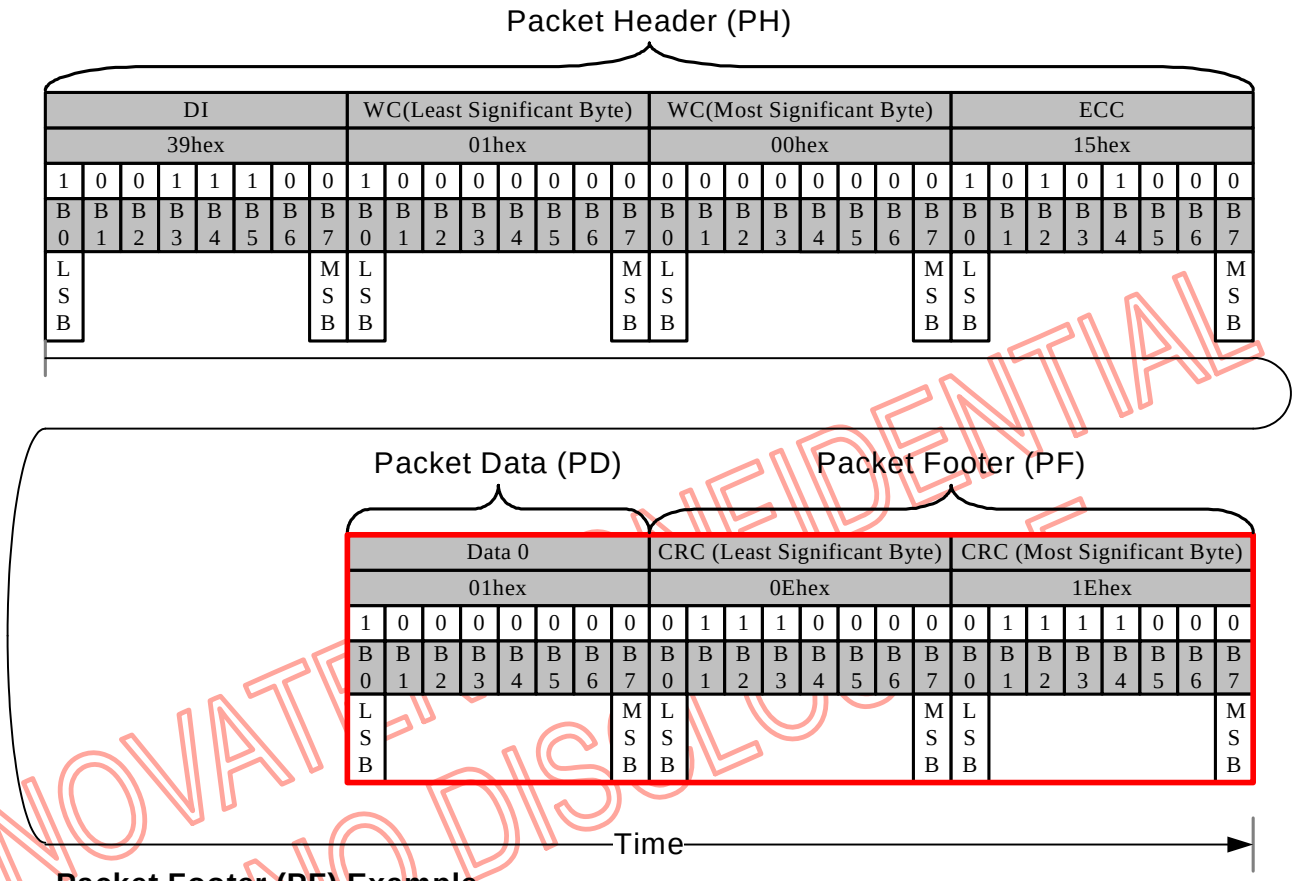
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR (In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR (In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Resoult	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

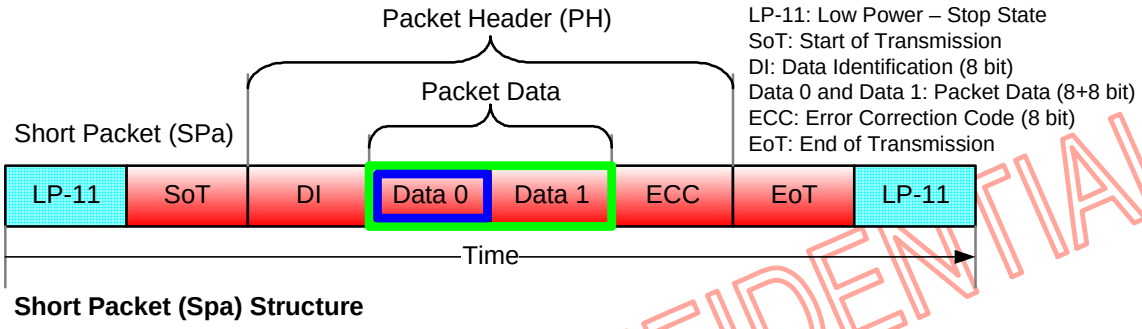
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.3.2.3.2 PACKET TRANSMISSIONS

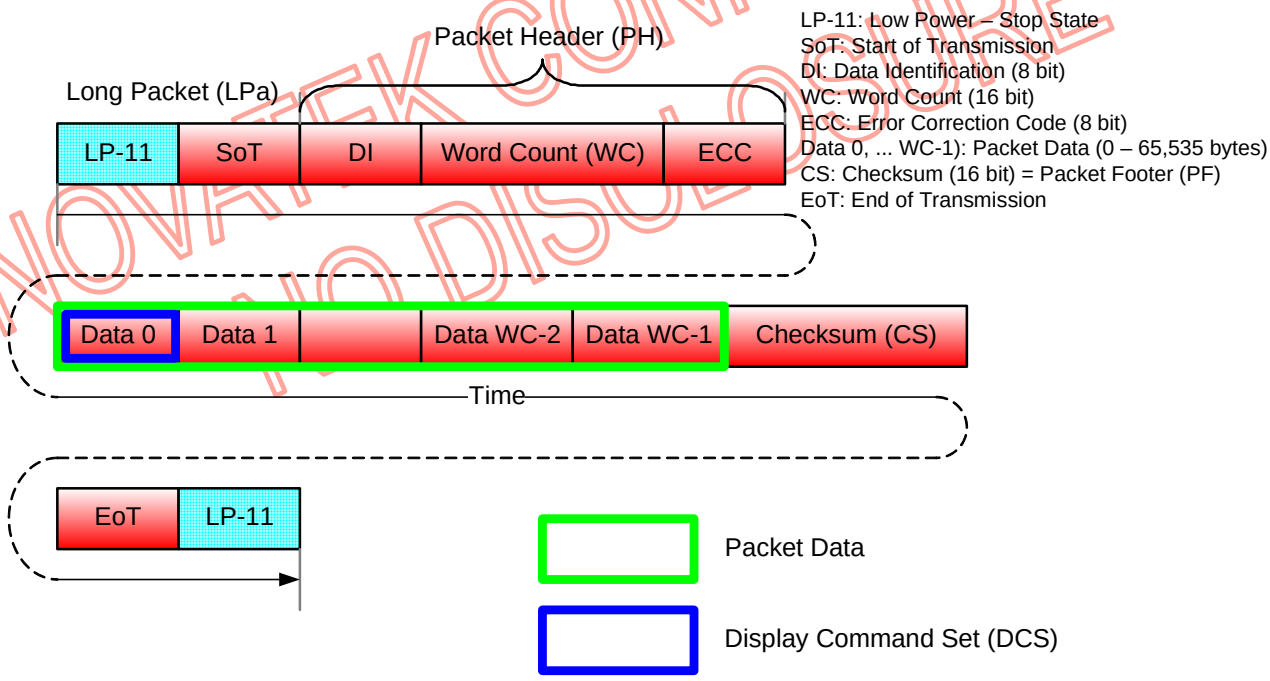
5.3.2.3.2.1 PACKET FROM THE MCU TO THE DISPLAY MODULE

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “6 Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



Short Packet (Spa) Structure



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h. These commands are defined on a table (See chapter "6 Instruction Description") below.

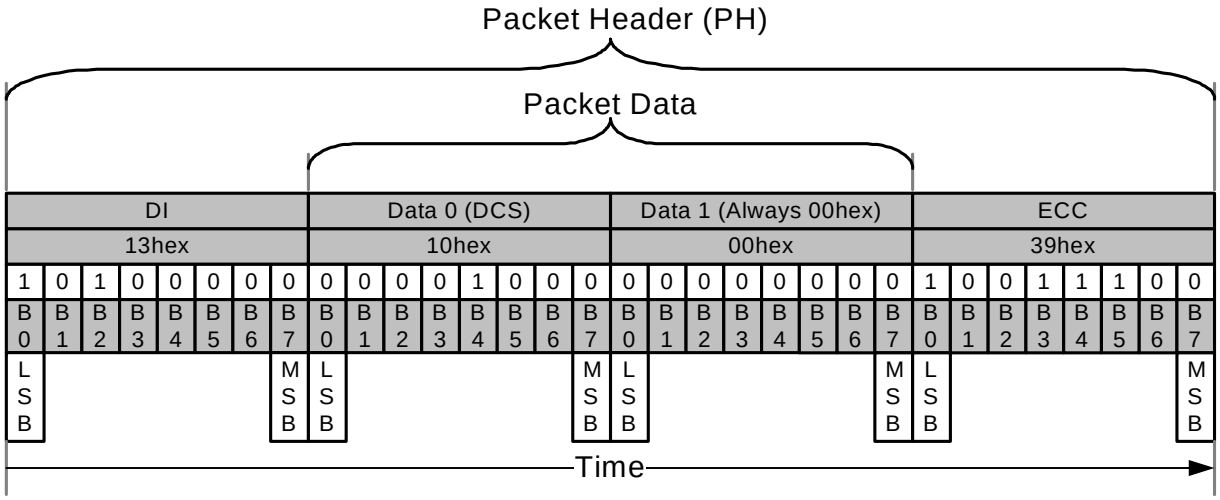
Command
NOP (00h)
SWRESET (01h)
SLPIN (10h)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
Memory Write (2Ch), Note
TEOFF (34h)
IDMOFF (38h)
IDMON (39h)

Note : Subpixel has not been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0011b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 1 Parameter (GENW1-S) - Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and "parameter". These commands are defined on a table (See chapter "6 Instruction Description") below.

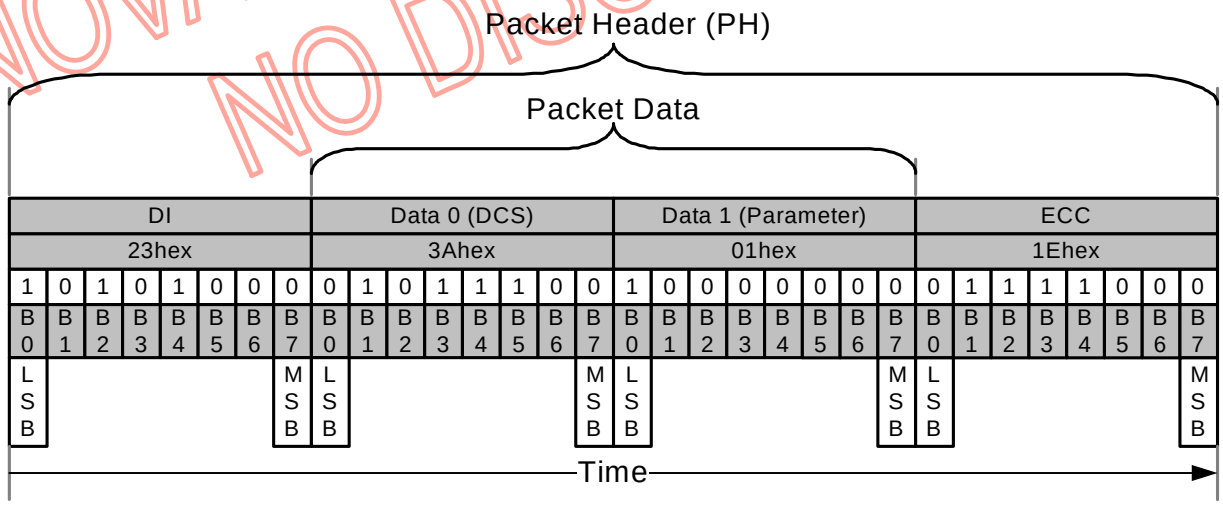
Command
GAMSET (26h)
RAMWR (2Ch), Note
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
RAMWRC (3Ch), Note
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Note：One Subpixel has been written.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0011b
- Packet Data (PD)
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) – Example

Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
PTLON (12h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
ALLPOFF (22h)
ALLPON (23h)
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
CASET (2Ah)
RASET (2Bh)
RAMWR (2Ch) , Note2
RGBSET (2Dh)
PARLINES (30h)
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTR (36h) , Note2
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
RAMWRC (3Ch), Note2
TEARLINE (44h)
WRPFD (50h)
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRHYSTE (57h) ,
WRGAMMSET (58h) ,
WRCABCMB (5Eh)
WRLSLC(65h)

Notes :

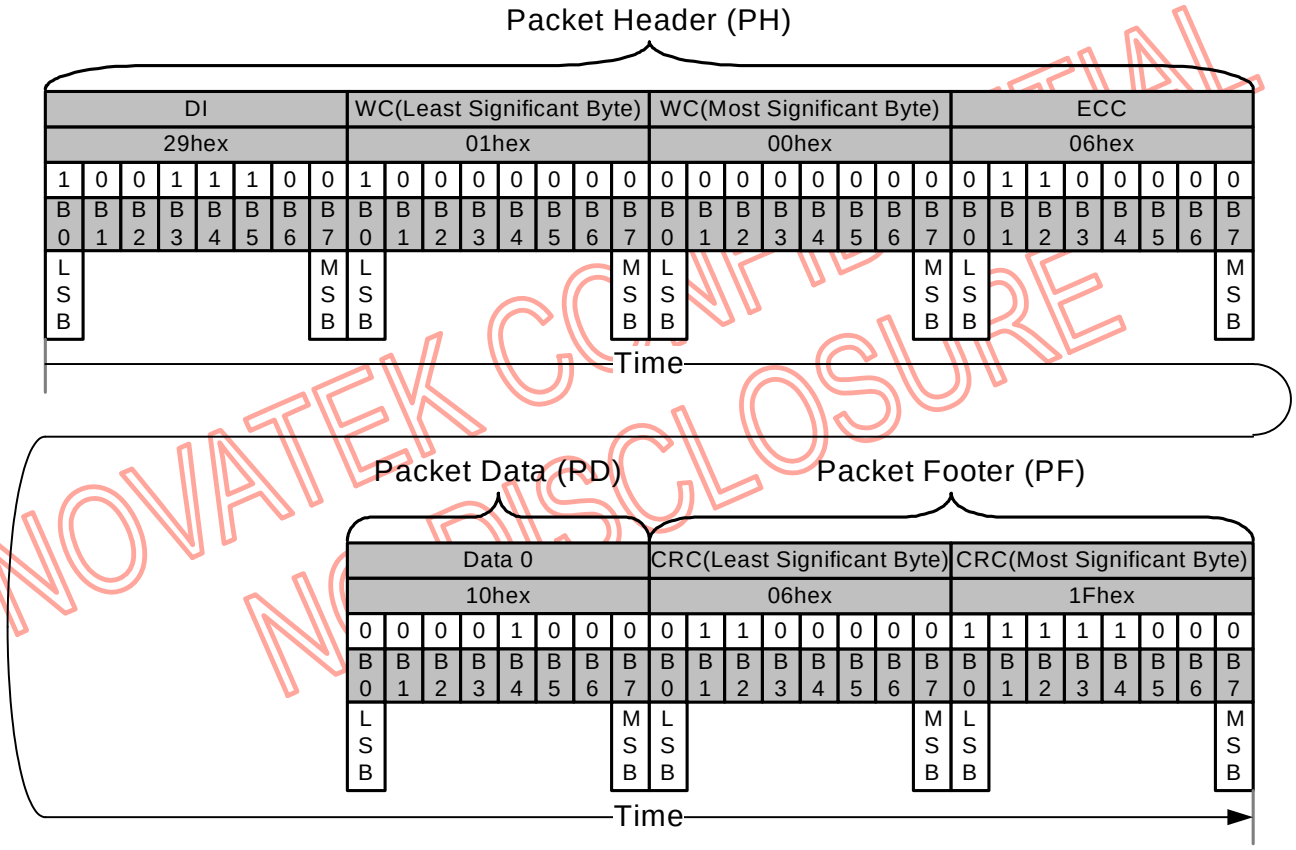
1. Also Short Packet (Spa) can be used; See Generic Write, 1 Parameter.

2. Also Short Packet (Spa) can be used; See Generic Write, 2 Parameter.

Long Packet (Lpa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

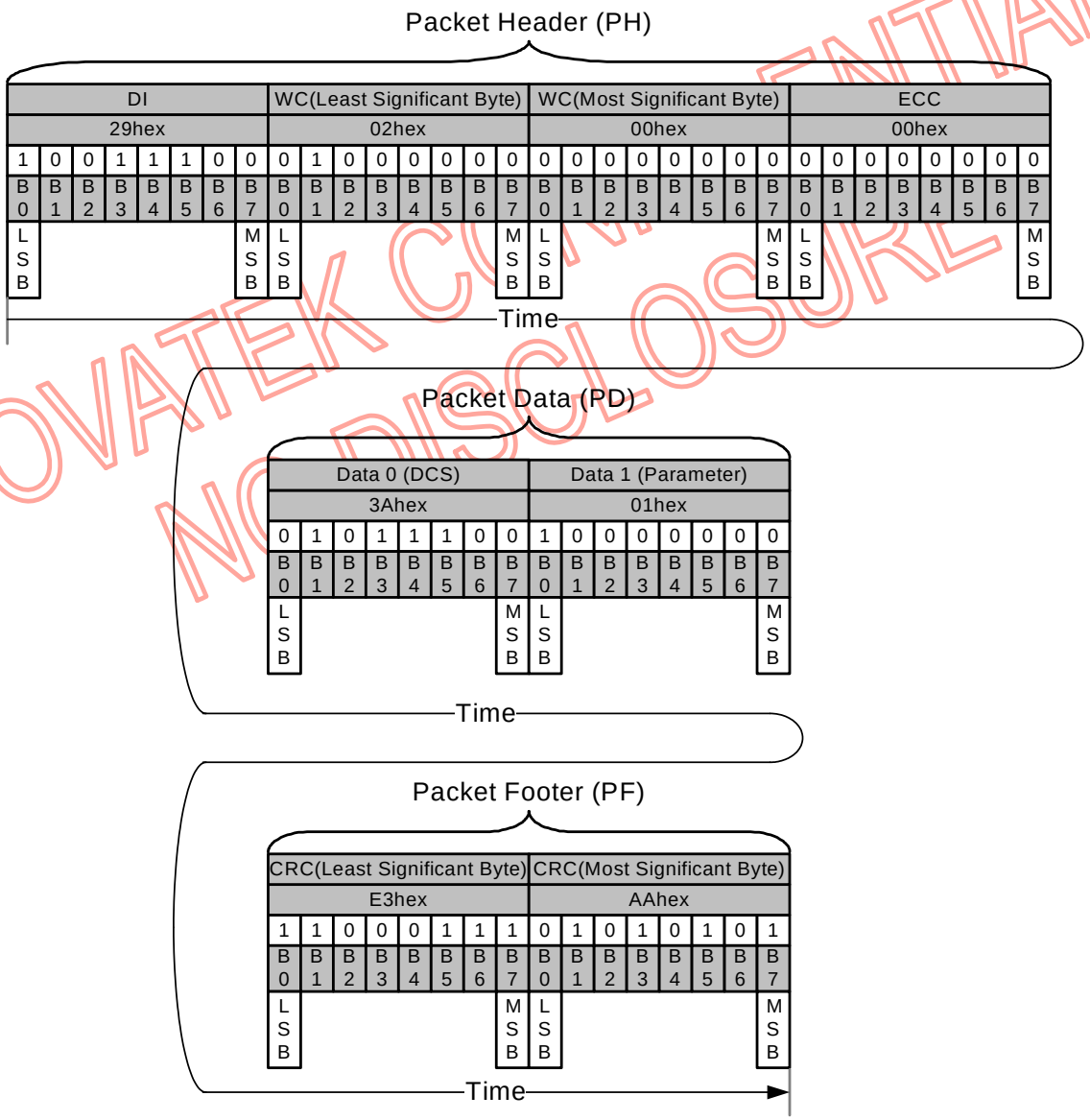


Generic Write Long (GENW-L) with DCS Only - Example

Long Packet (Lpa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Gamma Set (3Ah)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

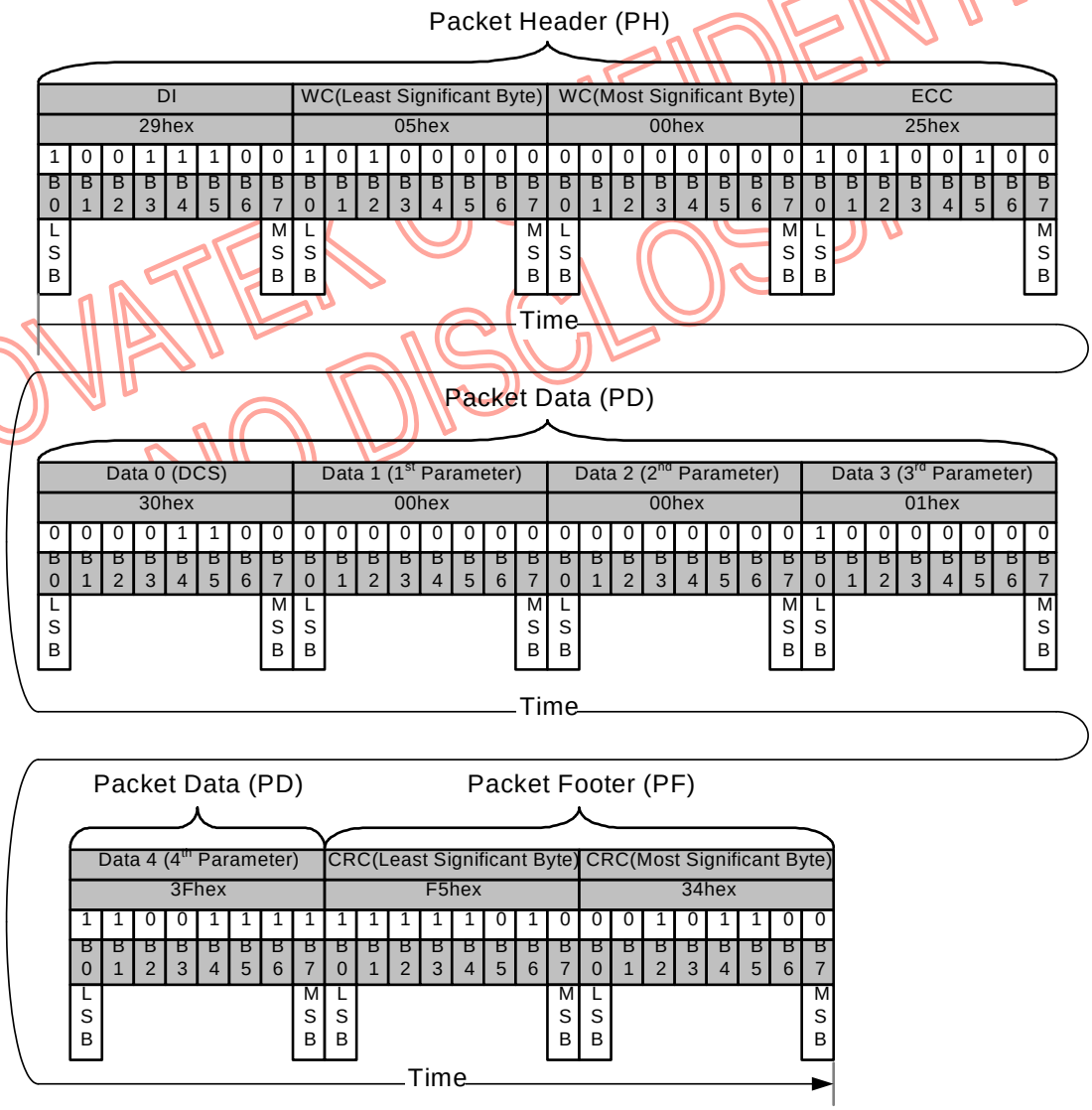


Generic Long Write with DCS and 1 Parameter - Example

Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “PARLINES (30h)”, Display Command Set (DCS)
  - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]
  - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]
  - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]
  - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.



Generic Write Long with DCS and 4 Parameters - Example

Generic Read, 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (Spa), what is defined on Data Type (DT, 01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "6 Instruction Description") below.

The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

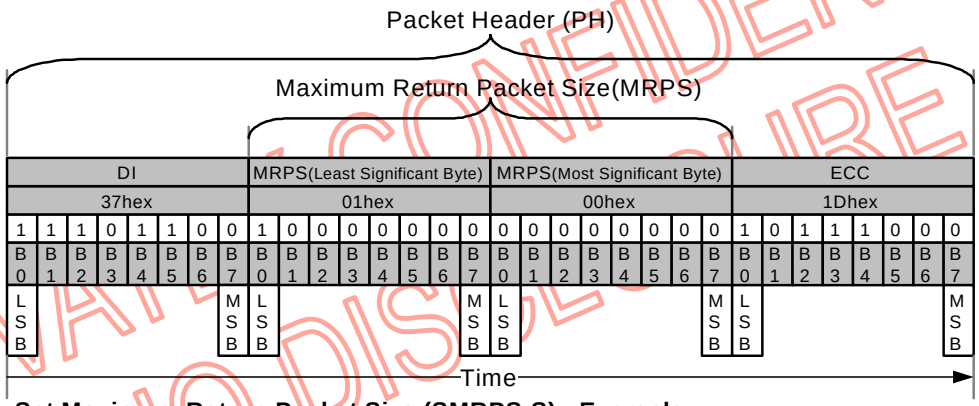
Command
RDNUMED (05h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
RAMRD (2Eh), Note
RAMRDC (3Eh), Note
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDFSVM (5Ah)
RDFSVL (5Bh)
RDMFFSVM (5Ch)
RDMFFSVL (5Dh)
RDCABCMB (5Fh)
RDLSCCM (66h)
RDLSCCL (67h)
RDBWLB (70h)
RDBkx (71h)
RDBky (72h)
RDWx (73h)
RDWy (74h)
RDRGLB (75h)
RDRx (76h)
RDRy (77h)
RDGx (78h)
RDGy (79h)
RDBALB (7Ah)
RDBx (7Bh)
RDBy (7Ch)
RDAx (7Dh)
RDAy (7Eh)
RDDDBST (A1h)
RDDDBC (A8h)
RDFCS (AAh)
RDCCS (AFh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

Note：One Subpixel has been read

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

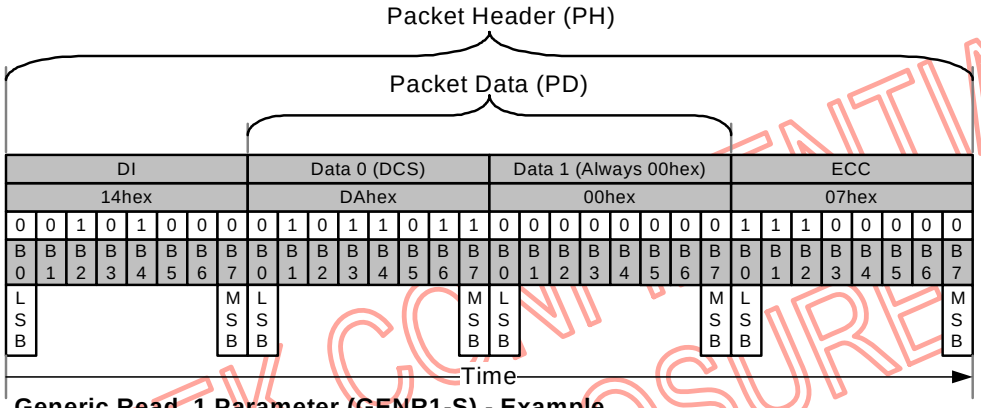
- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0100b
- Packet Data (PD)
  - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)



Generic Read, 1 Parameter (GENR1-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

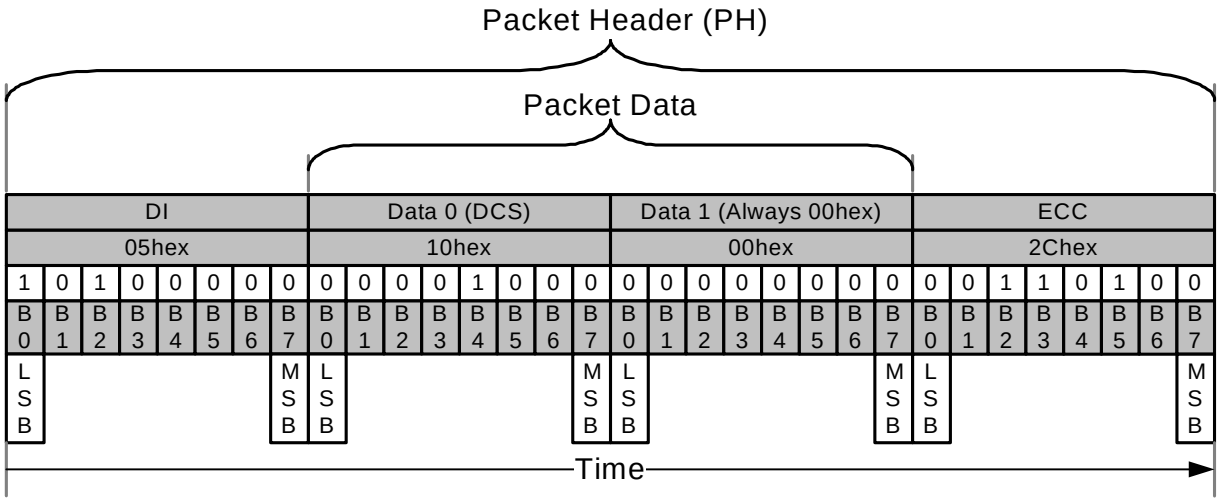
Command
NOP (00h)
SWRESET (01h)
SLPIN (10h)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
Memory Write (2Ch), Note
TEOFF (34h)
IDMOFF (38h)
IDMON (39h)

Note : Subpixel has not been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

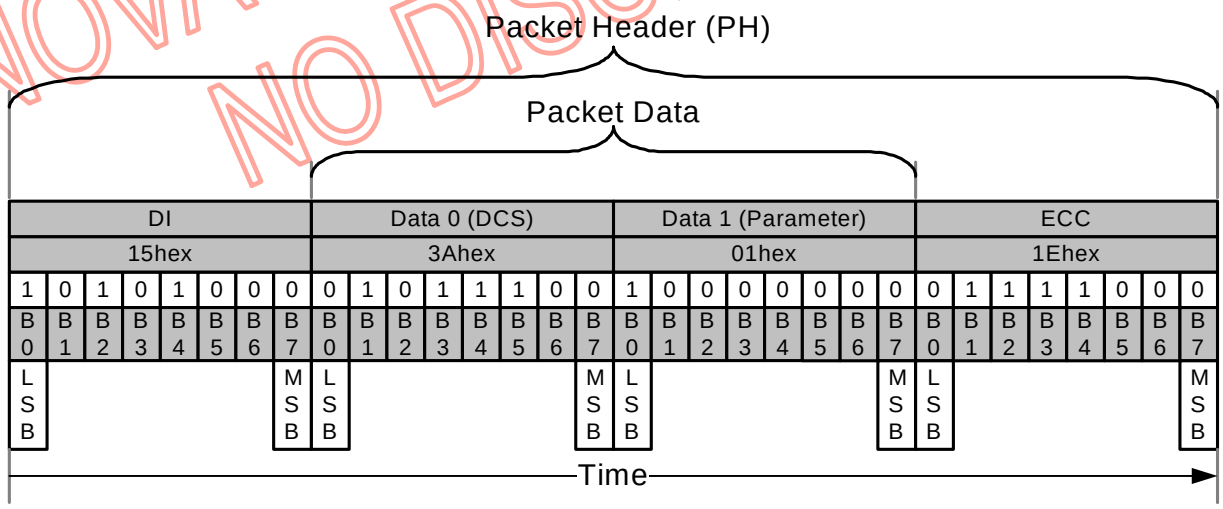
Command
GAMSET (26h)
Memory Write (2Ch), Note
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
RAMWRC (3Ch), Note
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Note：One Subpixel has been written.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
PTLON (12h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
CASET (2Ah)
RASET (2Bh)
RAMWR (2Ch) , Note2
RGBSET (2Dh)
PARLINES (30h)
SCRLAR (33h)
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTR (36h) , Note2
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
RAMWRC (3Ch), Note2
TEARLINE (44h)
WRPFD (50h)
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRHYSTE (57h) ,
WRGAMMSET (58h) ,
WRCABCMB (5Eh)
WRLSLC(65h)

Notes :

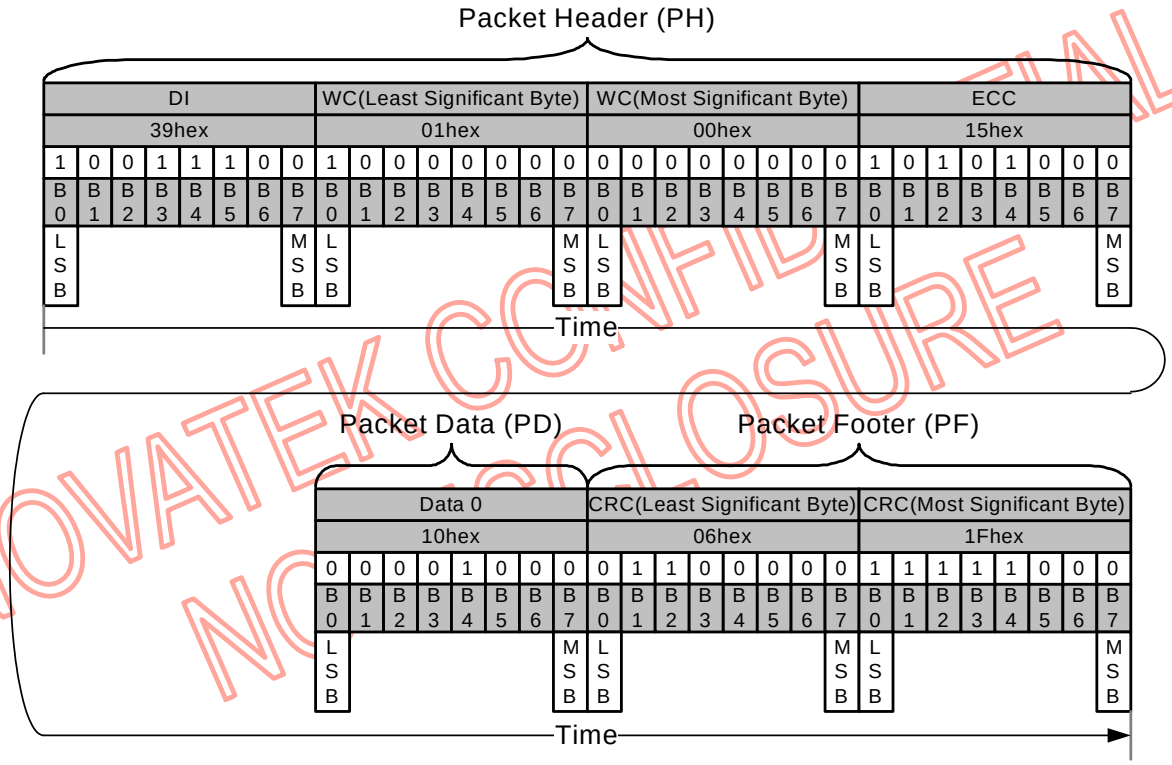
1. Also Short Packet (SPa) can be used; See_Display Command Set (DCS) Write, No Parameter.

2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

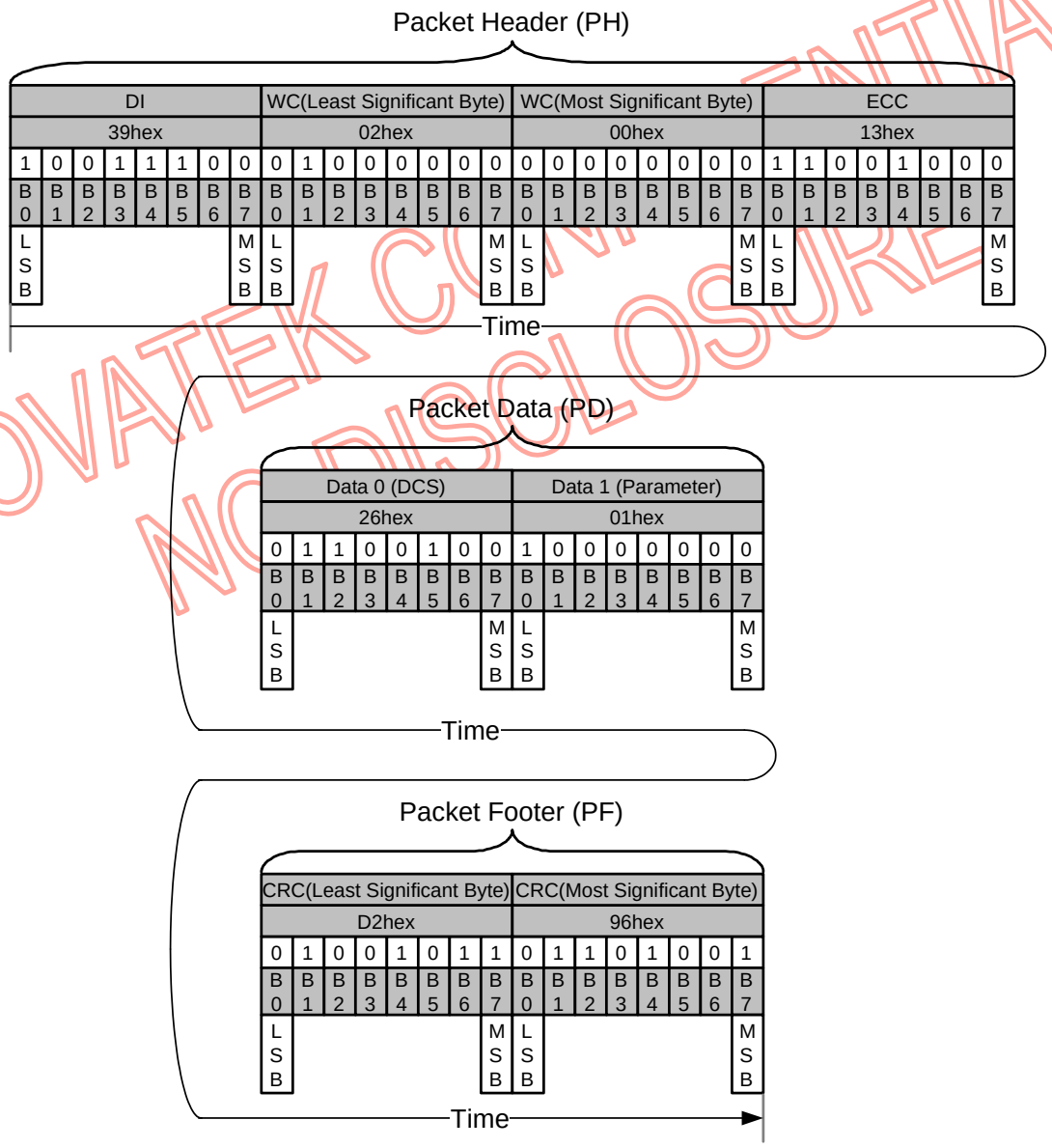


Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

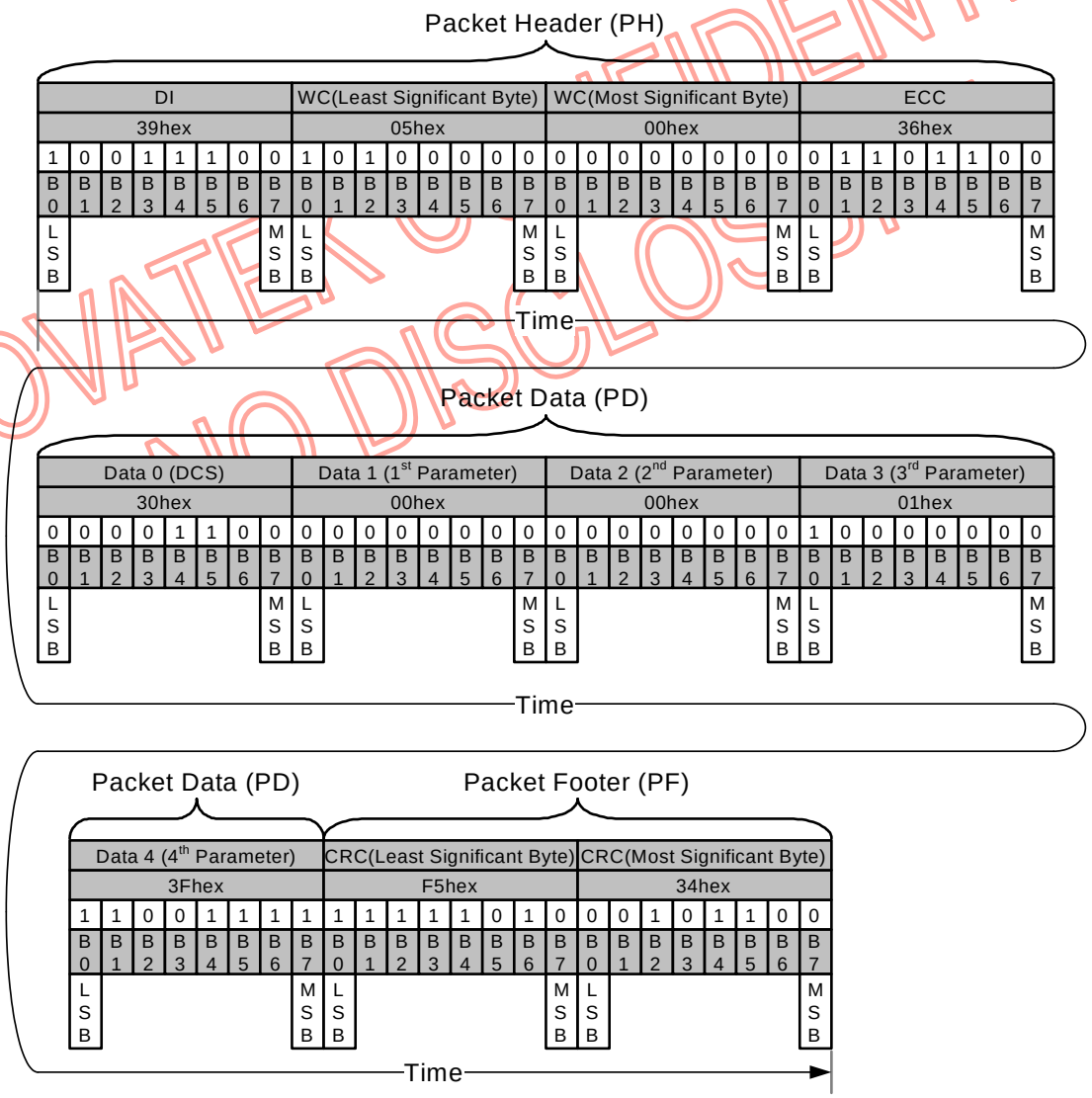


Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “PARLINES (30h)”, Display Command Set (DCS)
  - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]
  - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]
  - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]
  - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S) , Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

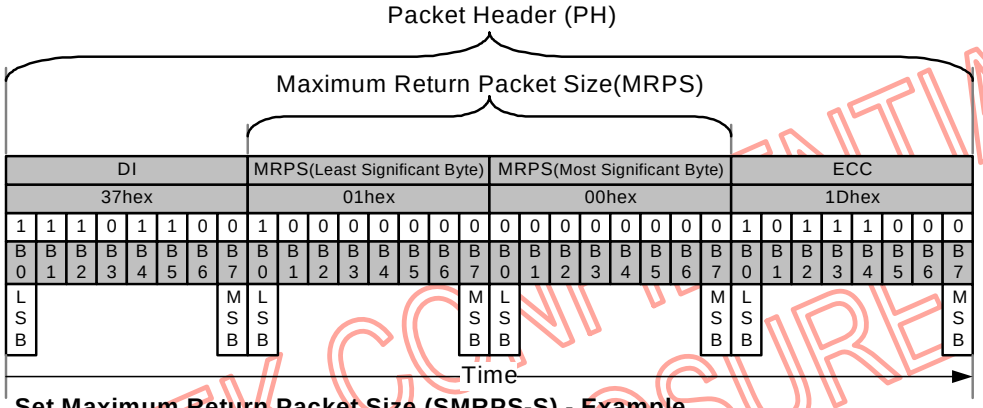
The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

Command
RDNUMED (05h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
RAMRD (2Eh), Note
RAMRDC (3Eh), Note
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDFSVM (5Ah)
RDFSVL (5Bh)
RDMFFSVM (5Ch)
RDMFFSVL (5Dh)
RDCABCMB (5Fh)
RDLSCCM (66h)
RDLSCCL (67h)
RDBWLB (70h)
RDBkx (71h)
RDBky (72h)
RDWx (73h)
RDWy (74h)
RDRGLB (75h)
RDRx (76h)
RDRy (77h)
RDGx (78h)
RDGy (79h)
RDBALB (7Ah)
RDBx (7Bh)
RDBy (7Ch)
RDAx (7Dh)
RDAy (7Eh)
RDDDBST (A1h)
RDDDBC (A8h)
RDFCS (AAh)
RDCCS (AFh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

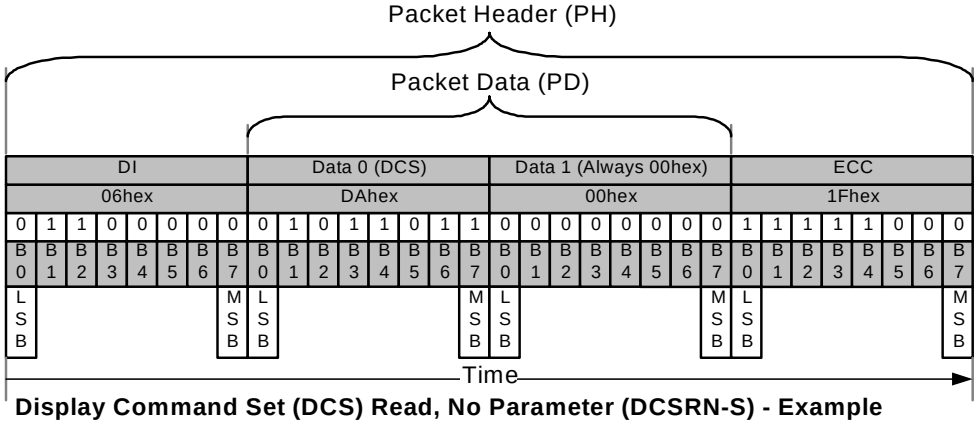
- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex
- Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0110b
- Packet Data (PD)
  - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
  - Data 1: Always 00hex
- Error Correction Code (ECC)



Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

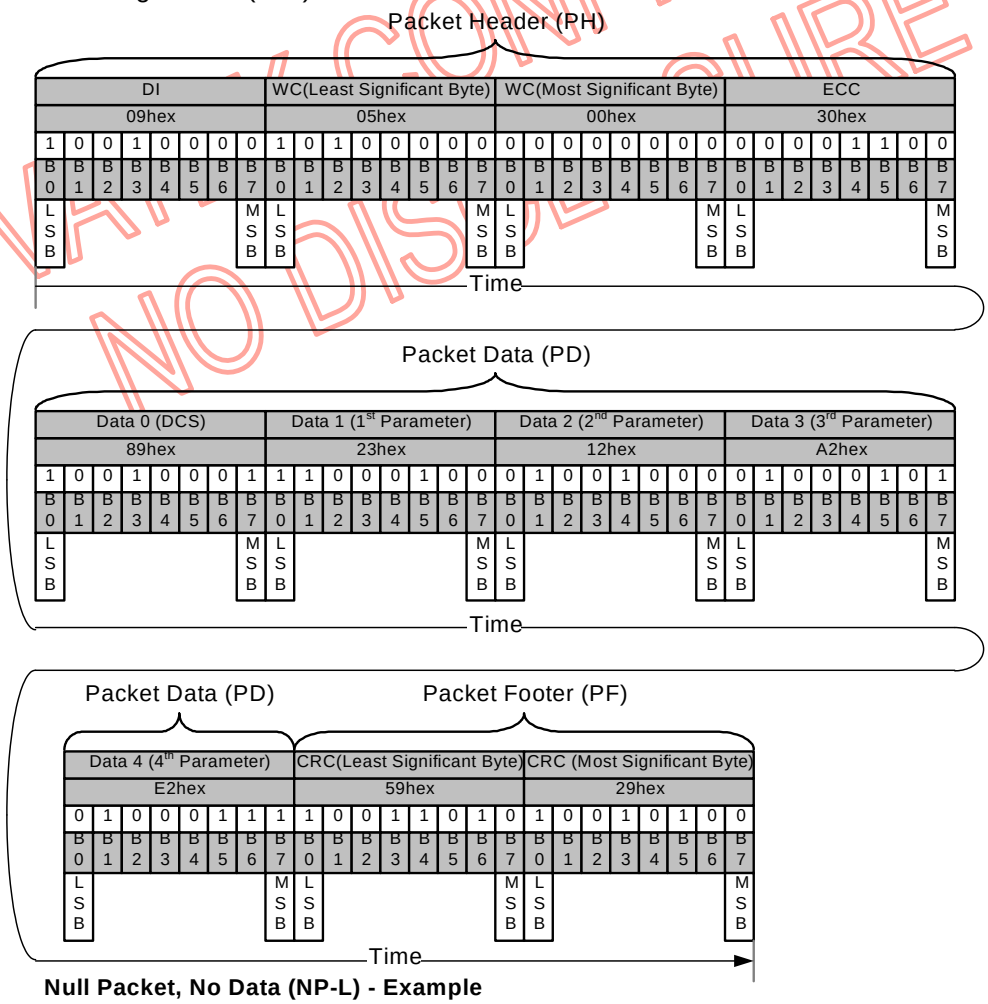
Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89h (Random data)
  - Data 1: 23h (Random data)
  - Data 2: 12h (Random data)
  - Data 3: A2h (Random data)
  - Data 4: E2h (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The NT35510 has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

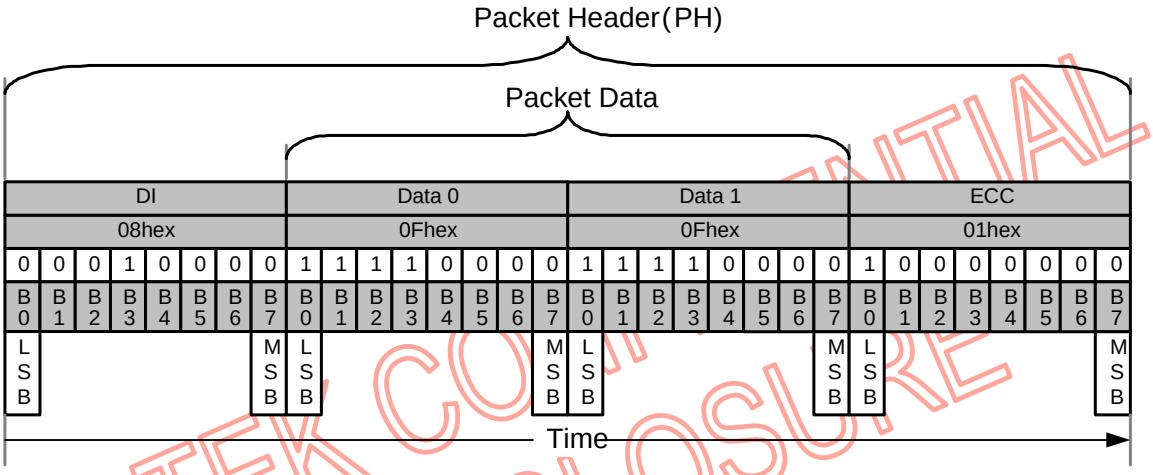
The summary of the receiving and transmitting EoTP is listed below.

Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver => MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

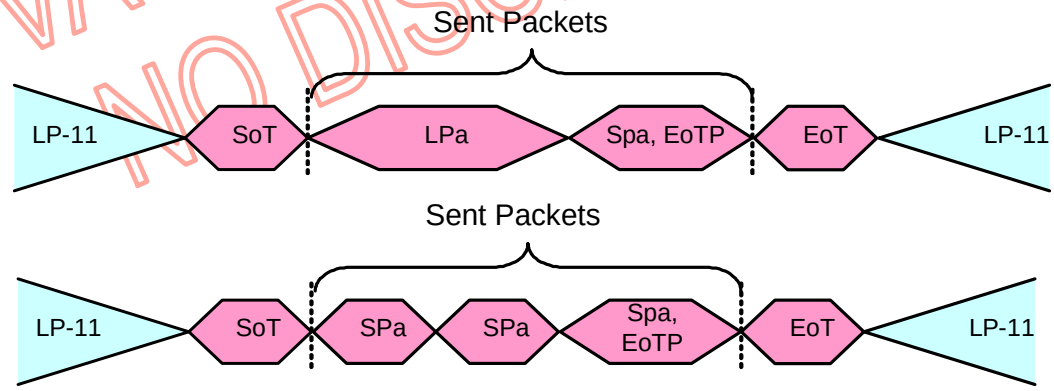
Short Packet (SPa) is using a fixed format as follow

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 1000b
- Packet Data (PD):
  - Data 0: 0Fh
  - Data 1: 0Fh
- Error Correction Code (ECC)
  - ECC: 01h



End of Transmission Packet (EoTP)

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.



End of Transmission Packet (EoTP) - Examples

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

• Data Type = 00 0001 (01h) V Sync Start
• Data Type = 01 0001 (11h) V Sync End
• Data Type = 10 0001 (21h) H Sync Start
• Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

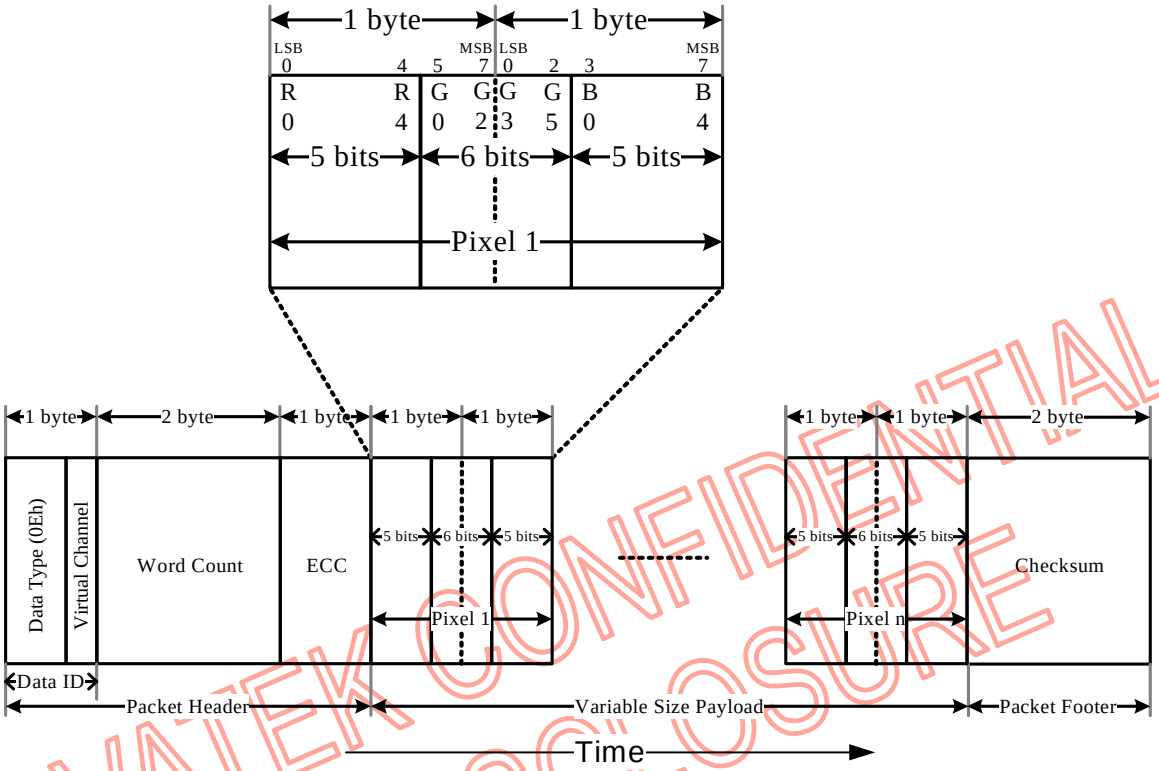
Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have *Sync Event* packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)



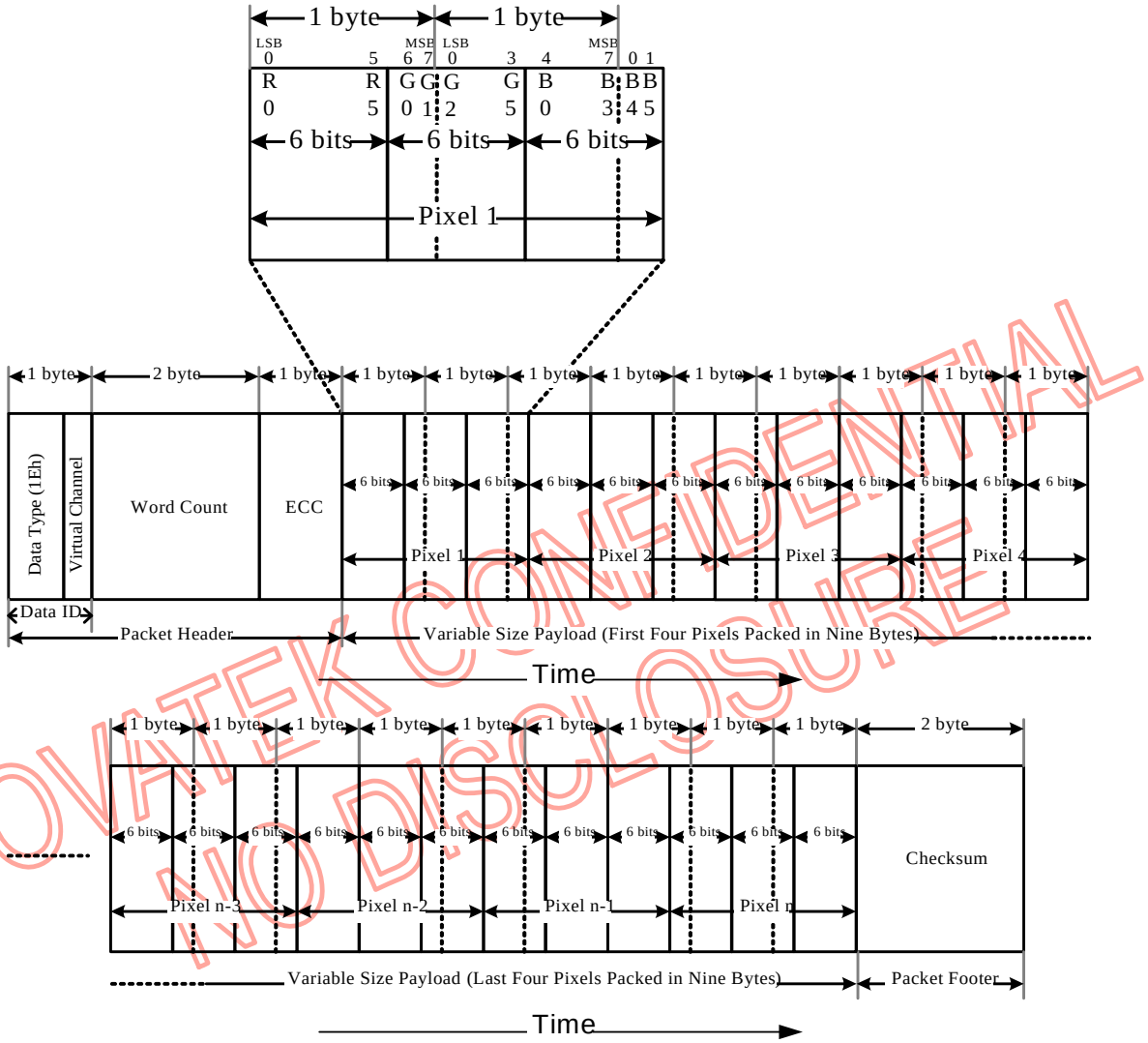
16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)



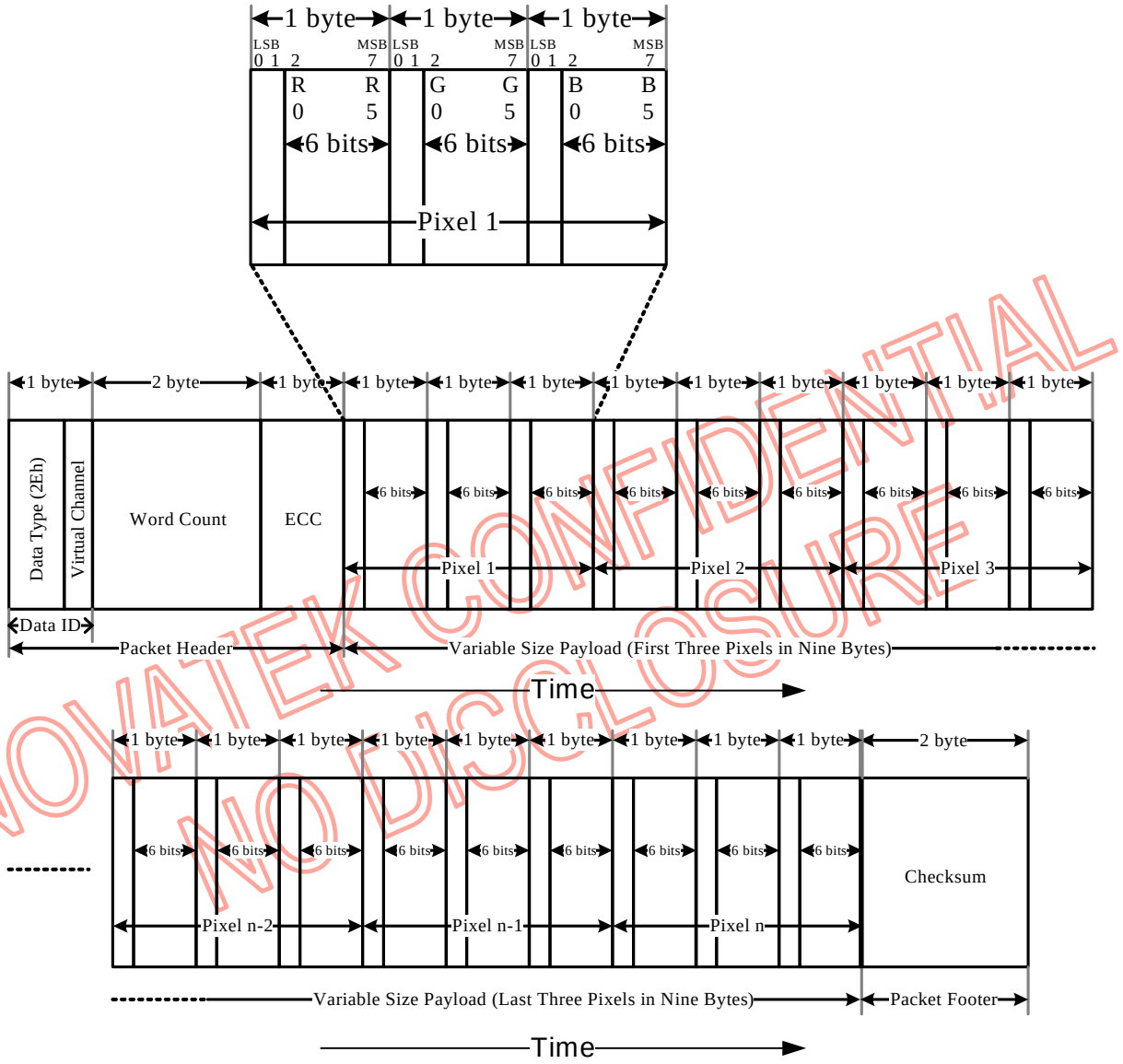
18-bit per Pixel (Packed)– RGB Color Format, Long packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



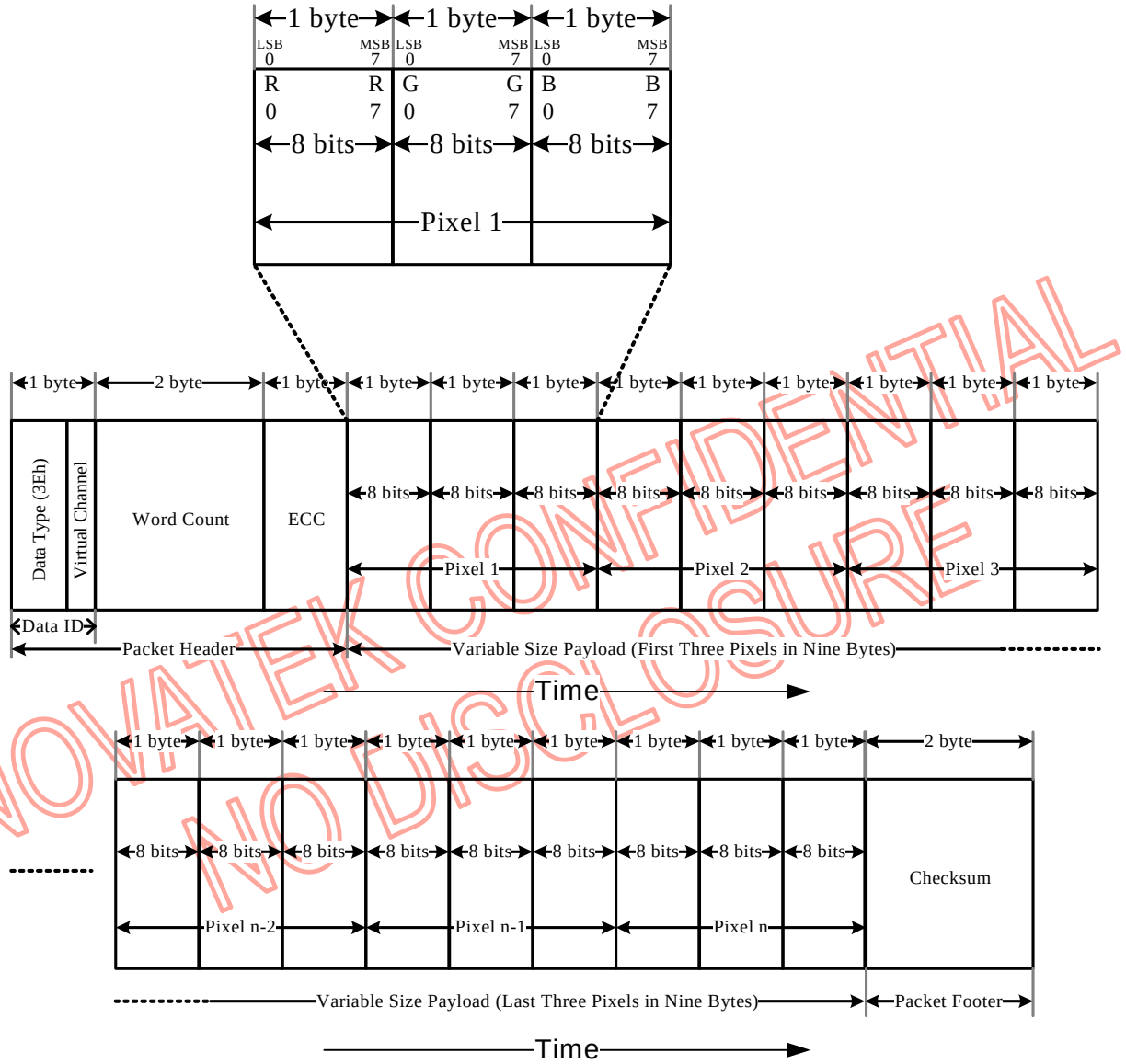
18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)



24-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.3.2.3.2.2 PACKET FROM THE DISPLAY MODULE TO THE MCU

Used Packet Types

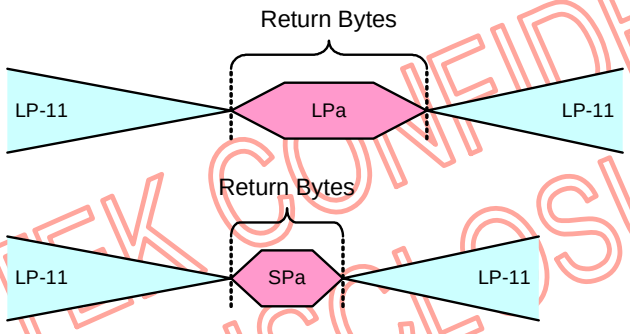
The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “5.3.2.3.2.1 Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “5.3.2.3.2.2 Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “5.3.2.3.1.3 Data Type (DT)”.

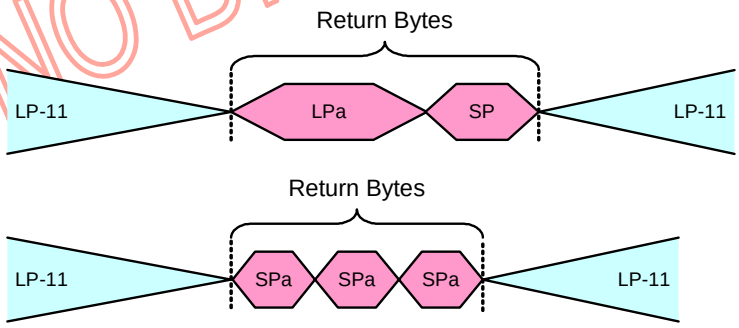
A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.



Return Bytes on Single Packet

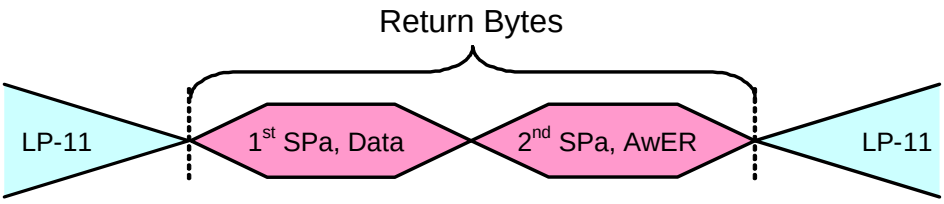


Return Bytes on Several Packets – Not Possible

Data Types for Display Module-sourced Packets

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	DCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	10 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Short Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Short Read Response, 2 Byte returned	Short

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table” Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). This return packets are illustrated for reference purpose below.



AwER = Acknowledge with Error Report

Exception when Return Bytes on Several Packet

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to "0" internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

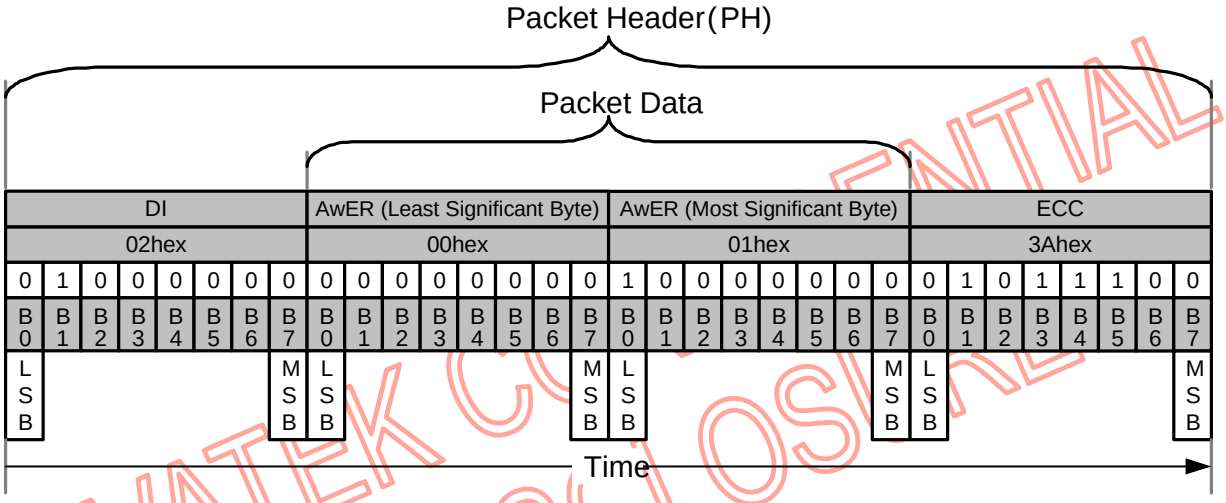
These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

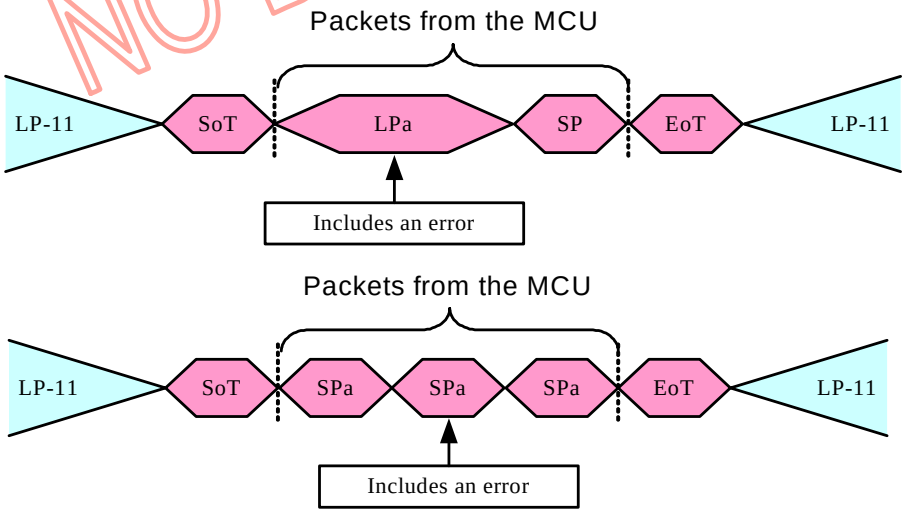
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD):
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER) Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.



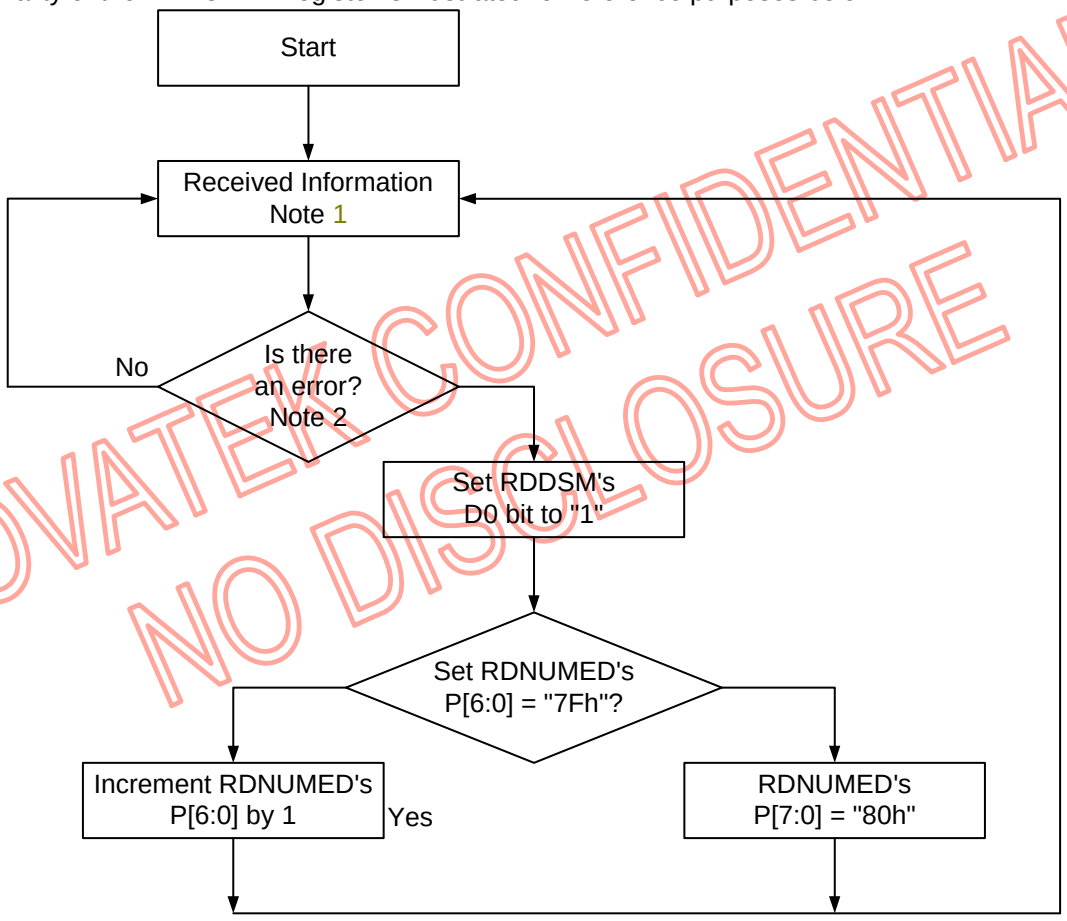
Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. *This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.*
2. *CRC or ECC error.*

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

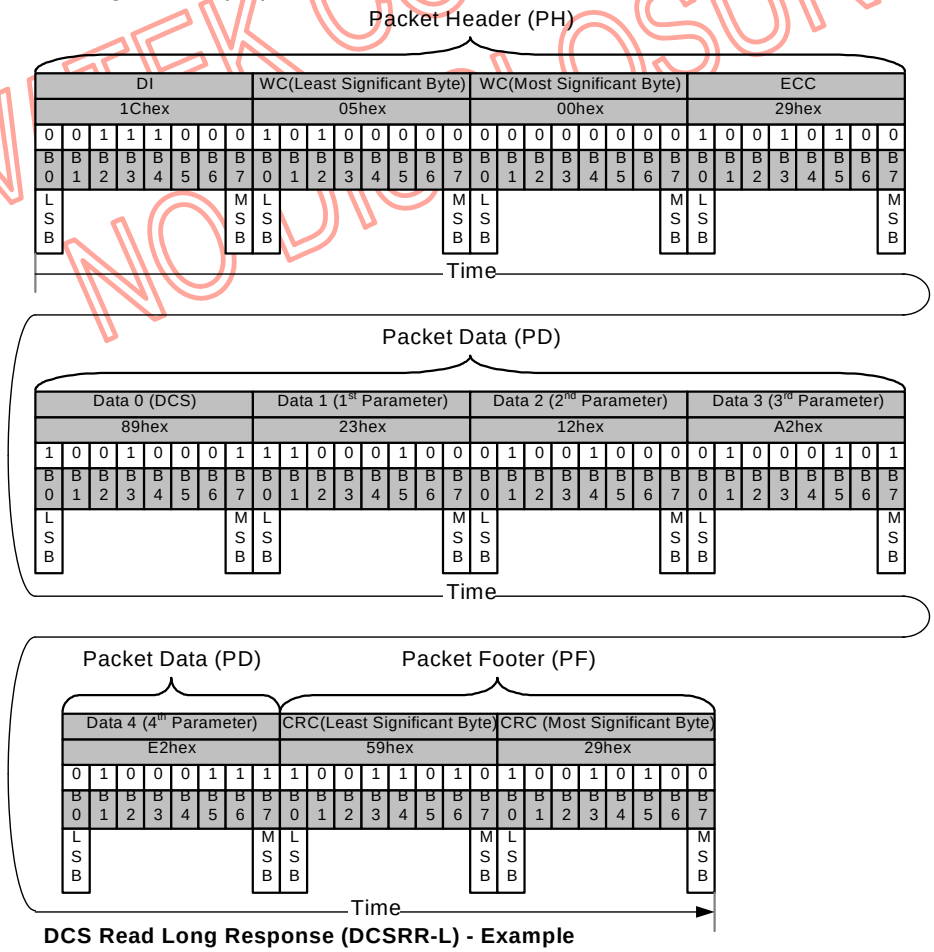
"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 1100b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89h
  - Data 1: 23h
  - Data 2: 12h
  - Data 3: A2h
  - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response (DCSRR-L) - Example

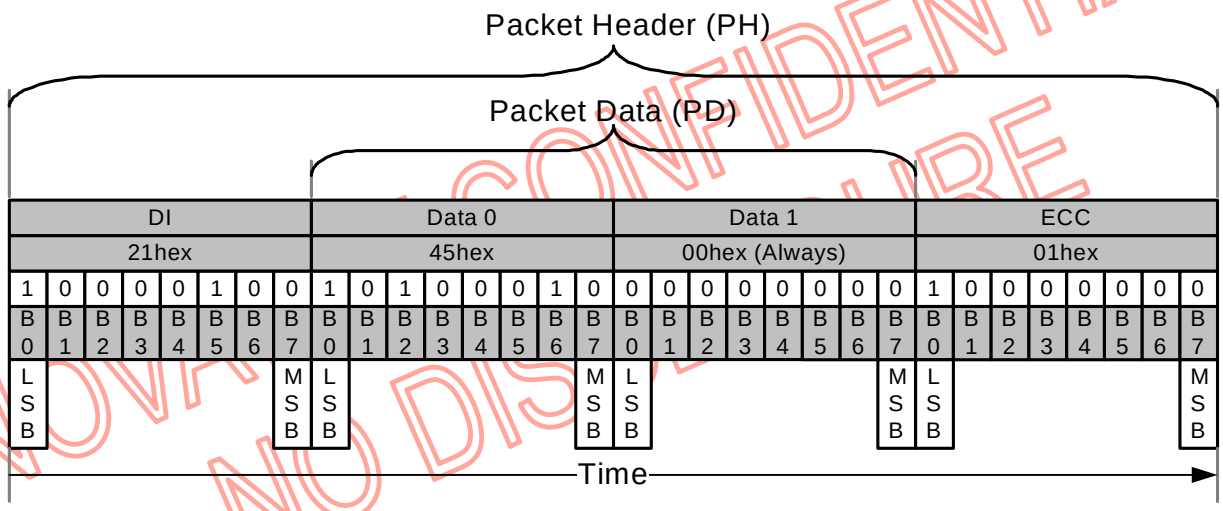
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0001b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

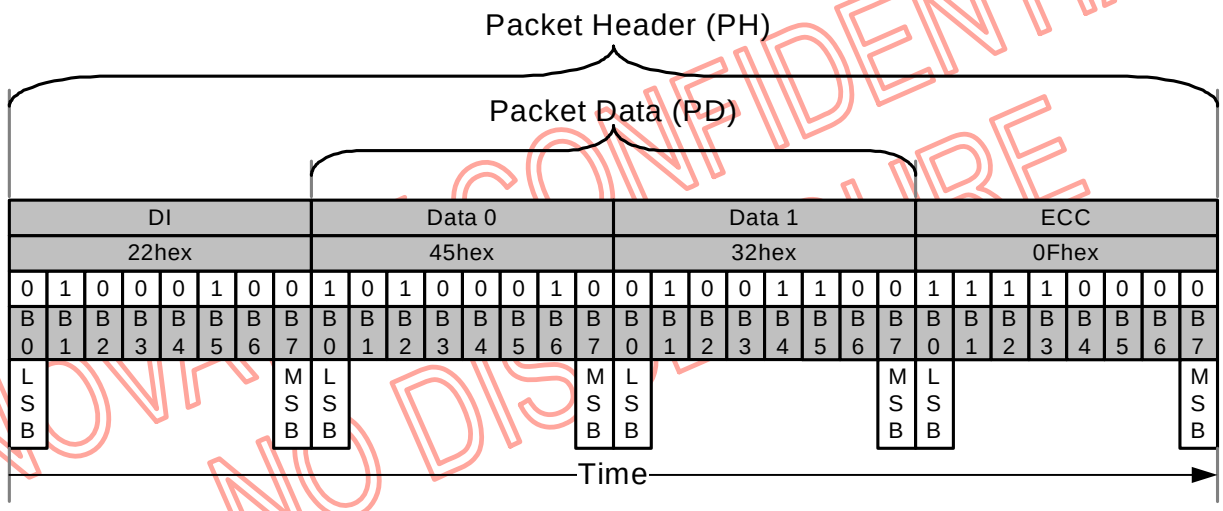
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0010b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

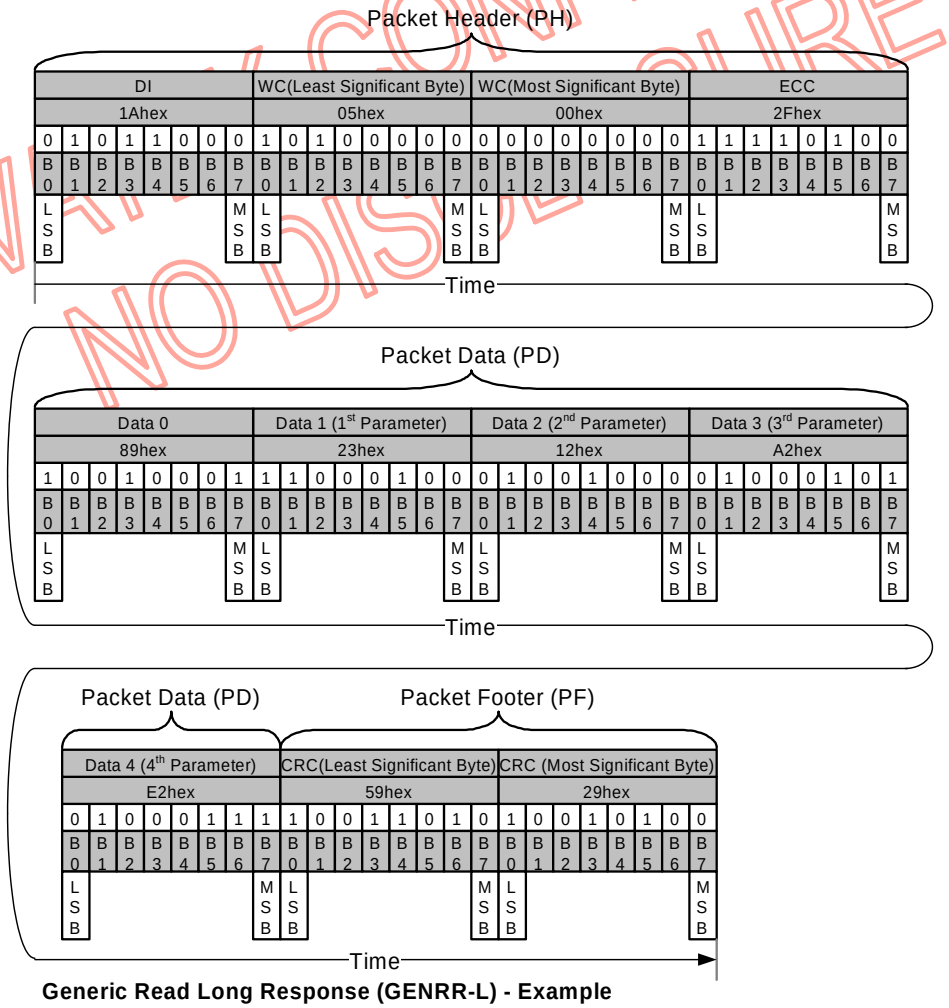
Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 1010b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89h
  - Data 1: 23h
  - Data 2: 12h
  - Data 3: A2h
  - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Generic Read Long Response (GENRR-L) - Example

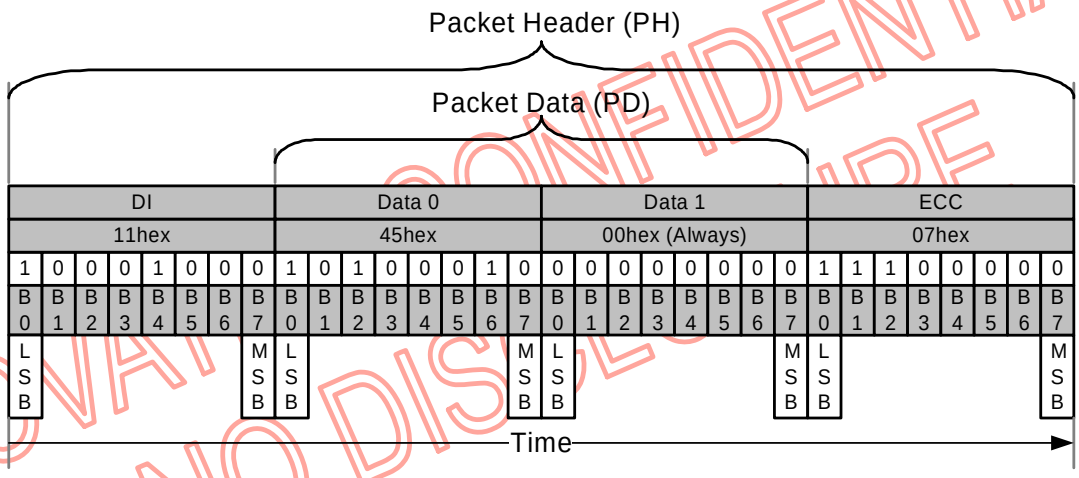
Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

"Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. "Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0001b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S) - Example

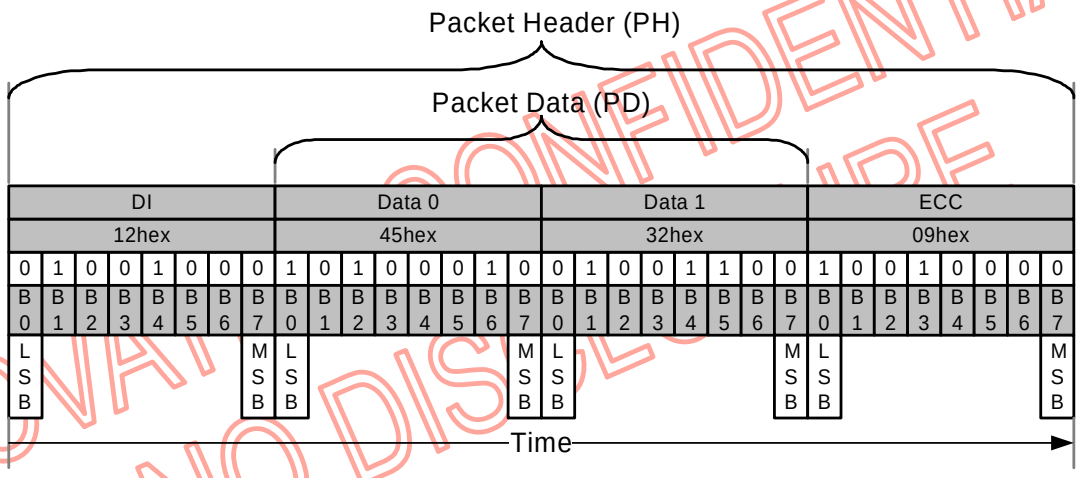
Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0010b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 2 Bytes Returned (GENRR2-S) - Example

5.3.2.3.3 COMMUNICATION SEQUENCES

5.3.2.3.3.1 GENERAL

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.3.2.3.3.2 SEQUENCES

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Memory Write (2Ch)
3	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
4	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
5	DCSW1-S	HSDT	=>	-	-	Memory Write Continue(3Ch) with 1 parameter
6	EoTP	HSDT	=>	-	-	End of Transmission Packet
7	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR-L	Responsed 200 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module t to he MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR-L	Responsed 200 bytes return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
2	EoTP	HSDT	=>	-	-	End of Transmission Packet
3	-	LP-11	=>	-	-	End

5.3.2.4 VIDEO MODE COMMUNICATION

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.3.2.4.1 TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

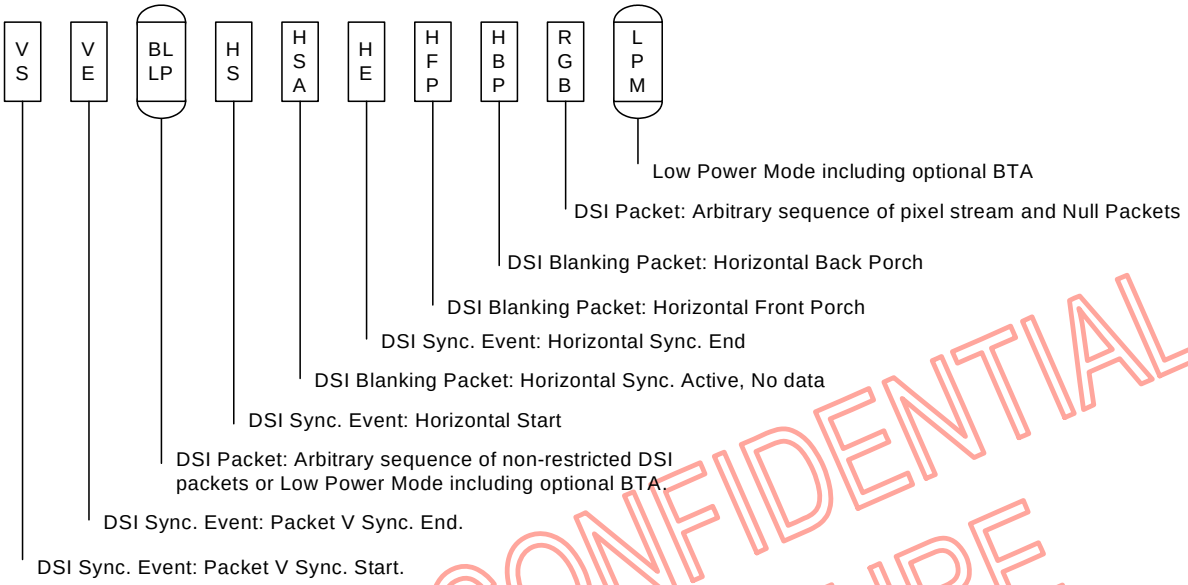
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

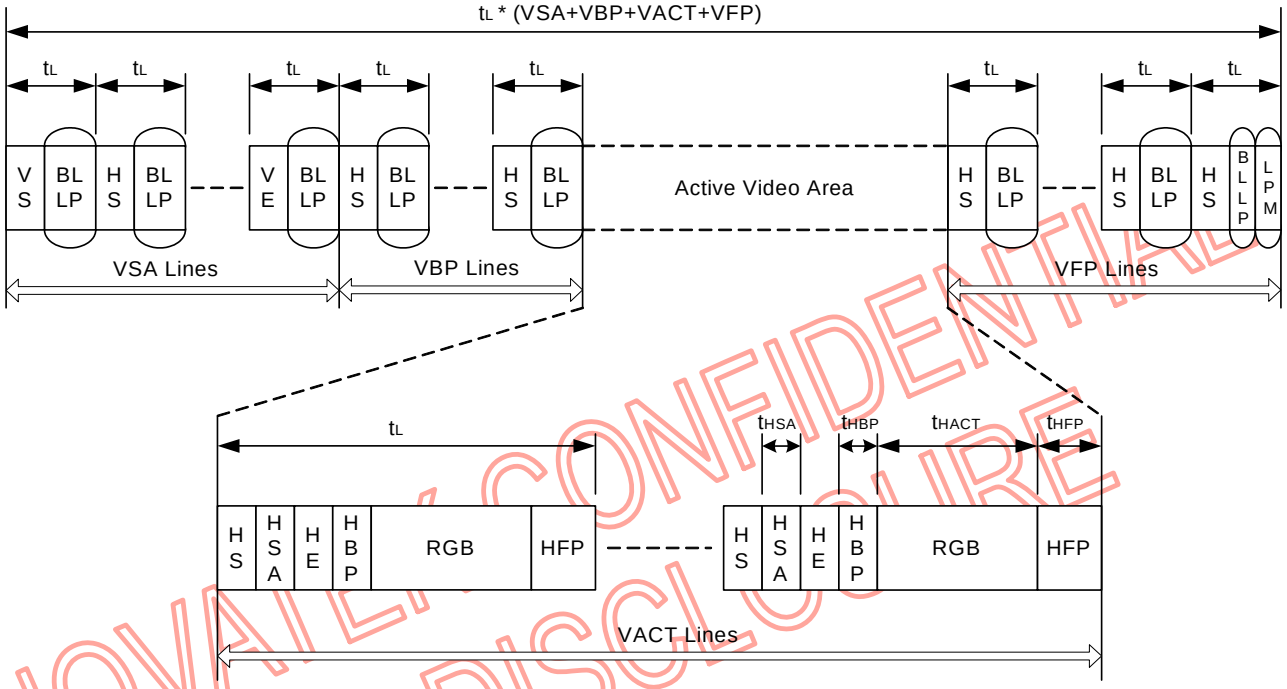


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.3.2.4.2 NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

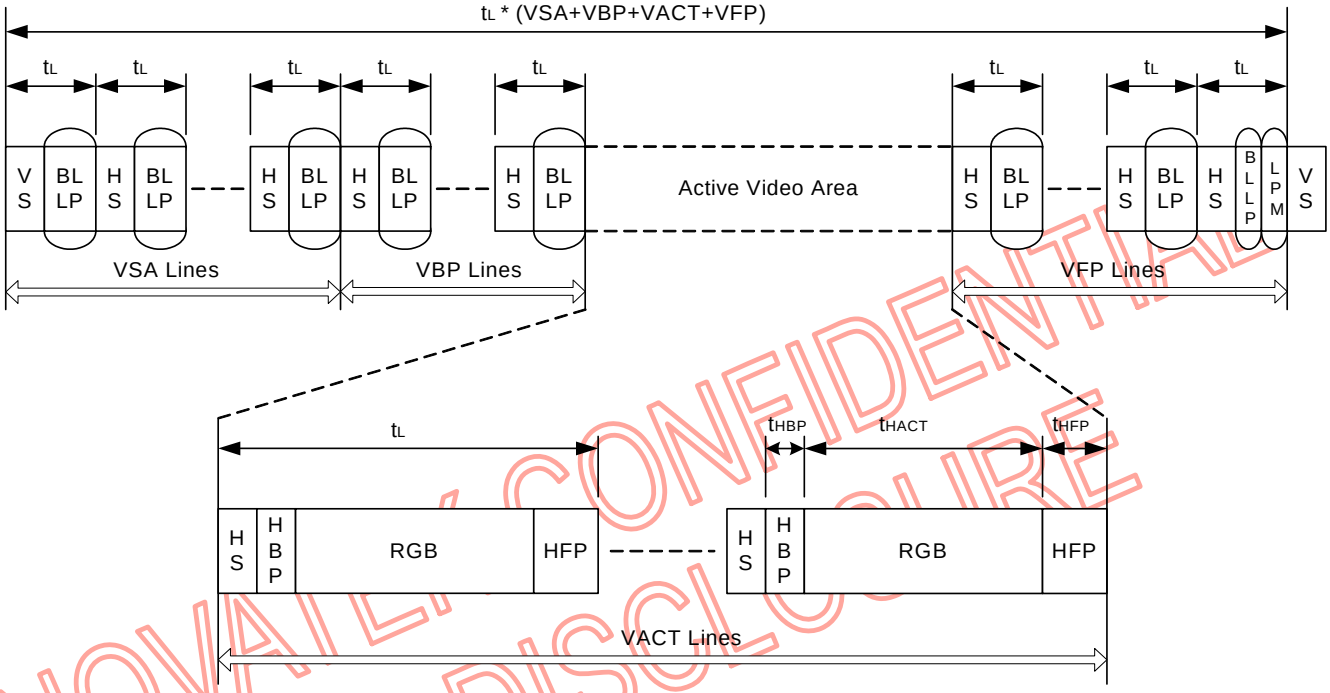


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.2.4.3 NON-BURST MODE

This mode is a simplification of the format described in section 5.3.2.4.2 “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

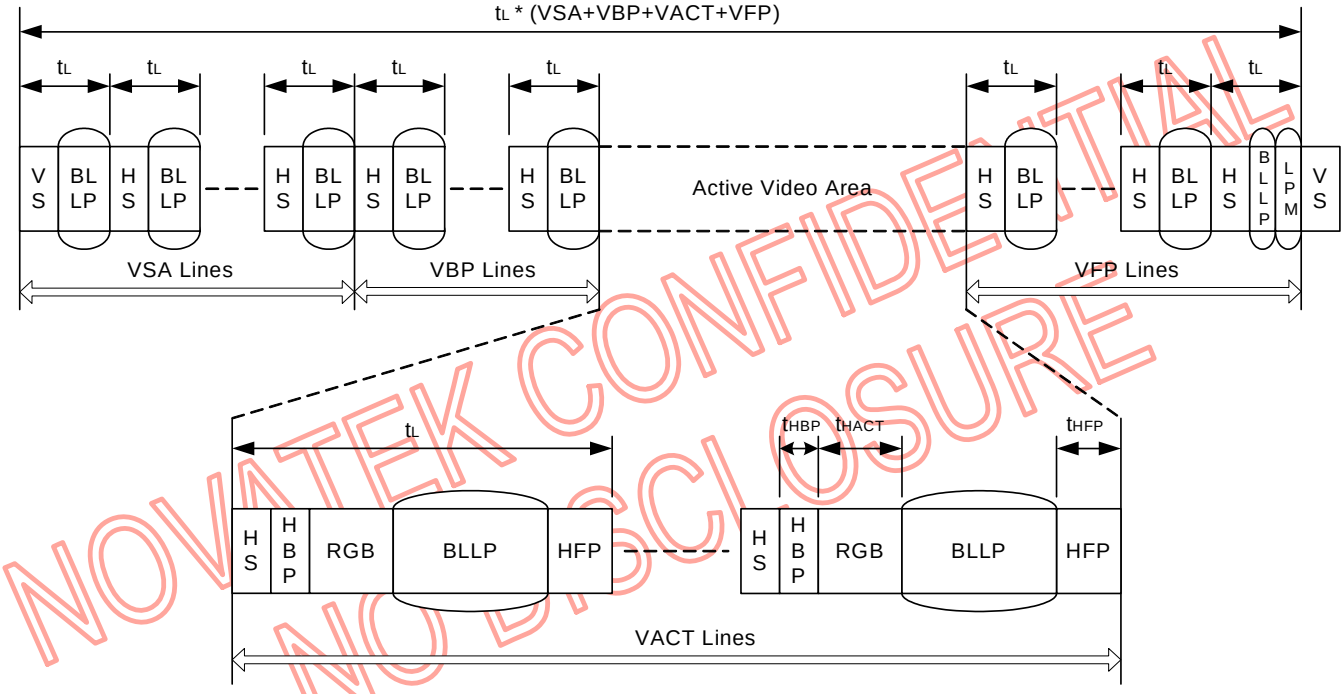


DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.2.4.4 BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.3.2.4.5 PARAMETERS

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

Required Peripheral Timing Parameters

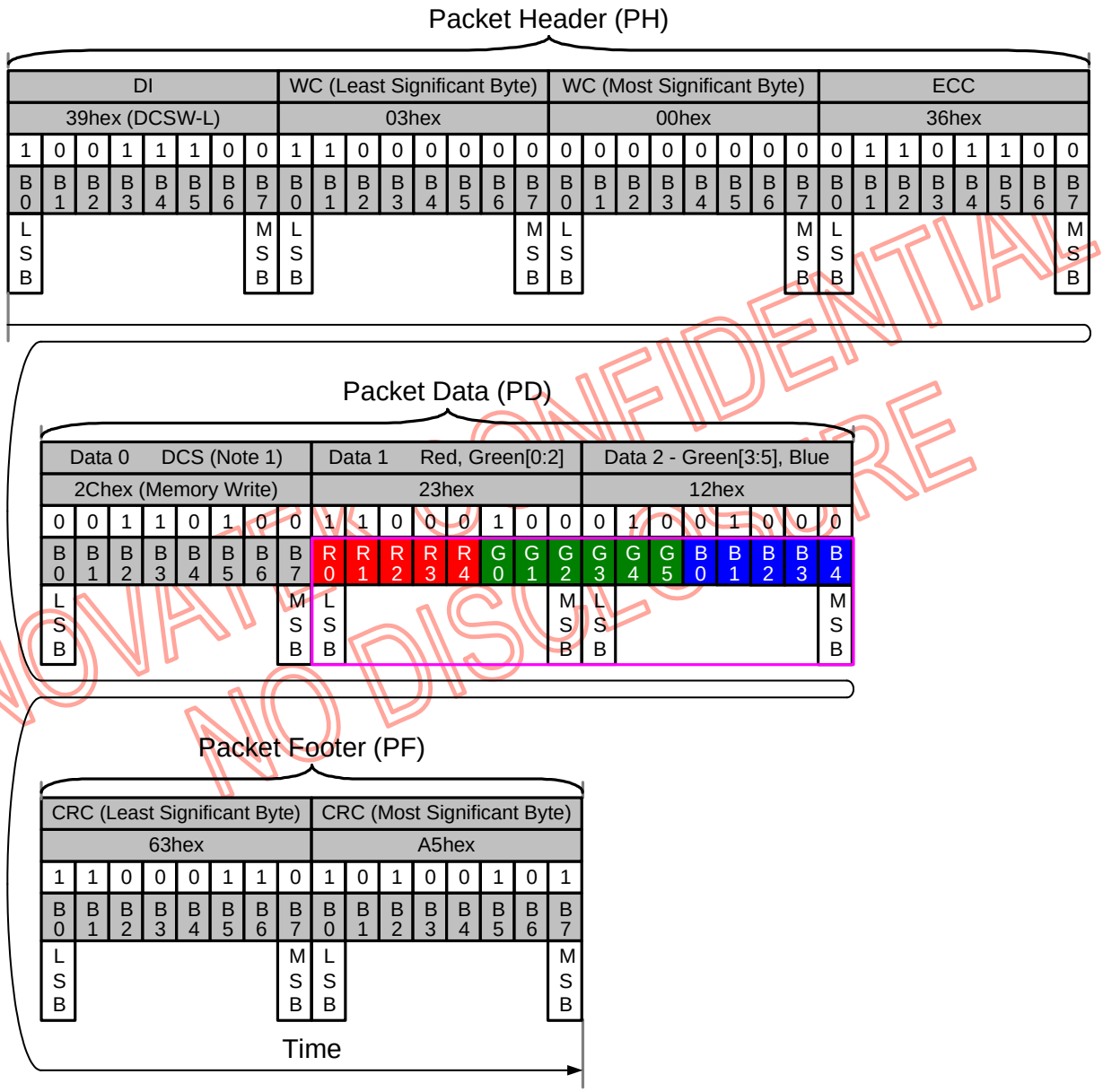
Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes	WVGA	80	-	500	Mbps
tL	Line time	WVGA	-	19	-	us
tHBP	Horizontal back porch	WVGA	0.5	-	-	us
tHACT	Time for image data	2 data lane	7.68	-	Note3	us
HACT	Active pixels per line	WVGA	-	480	-	pixels
tHFP	Horizontal front porch	-	0.5	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	4, Note2	-	-	H
VACT	Active lines per frame	WVGA	-	864	-	H
VFP	Vertical front porch	-	4	-	-	H

Note1: Frame rate (Typ)=60Hz
Note2: VBP (min) value can change by command set.
Note3: tHACT+tHFP+ tHBP ≥ tL

5.3.3 Memory Write/Read Format

- 16 bit/pixel Writing

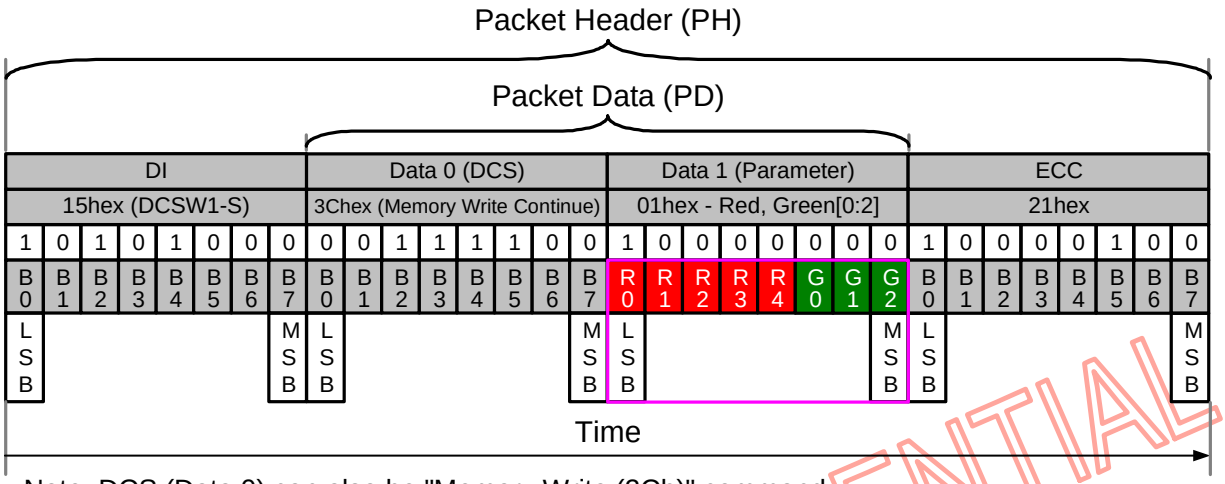
The MCU can send to the display module a following packet.



Notes:

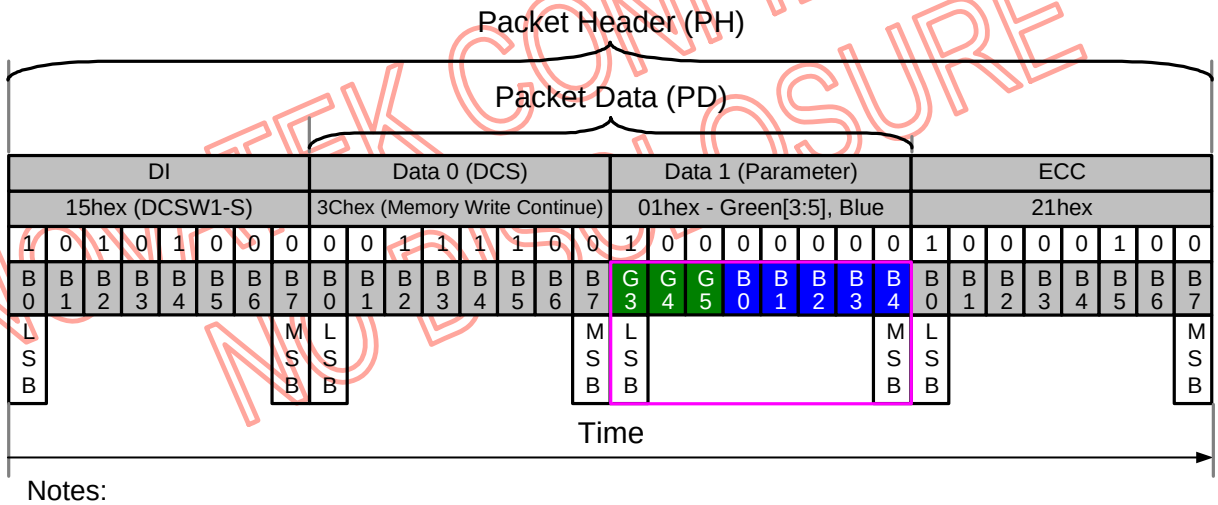
1. Memory Write (2Ch) or Memory Write Continue (3Ch)
2. It is possible that one pixel information is split in one different packets which are ending and starting as follows: RG GB (2 packets)
3. Packet can include several pixel (Not only one pixel as in this example)

One Pixel Write (DCSW-L) Example 1



Note: DCS (Data 0) can also be "Memory Write (2Ch)" command

Red/Green[0:2] Subpixel Write (DCSW1-S) Example 2

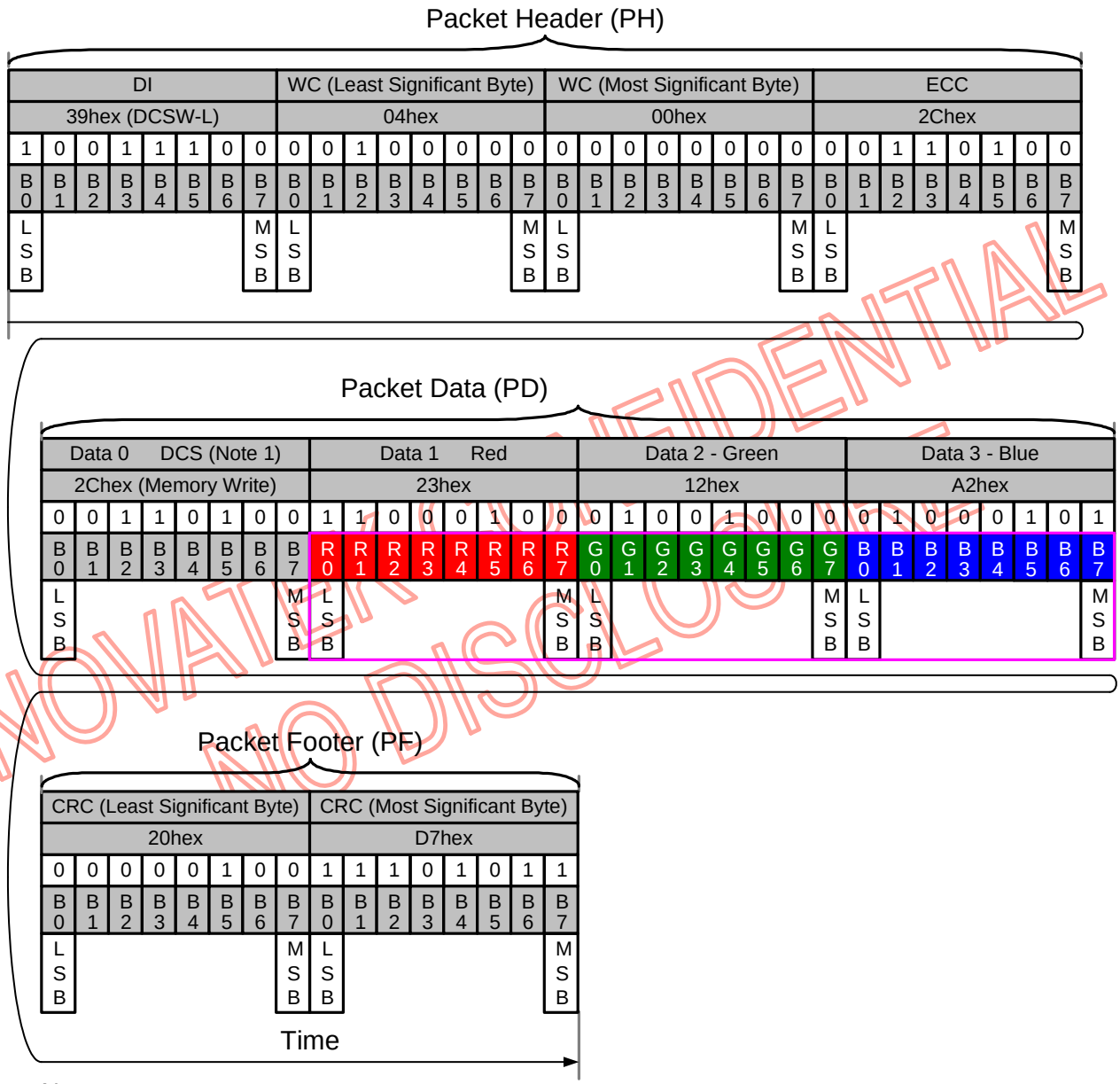


Notes:
1. DCS (Data 0) can not be "Memory Write (2Ch)" command.
   It must always be "Memory Write Continue (3Ch)".
2. Previous data byte was R[0:4]G[0:2]

Green[3:5]/Blue Subpixel Write (DCSW1-S) Example 3

- 24 bit/pixel Writing

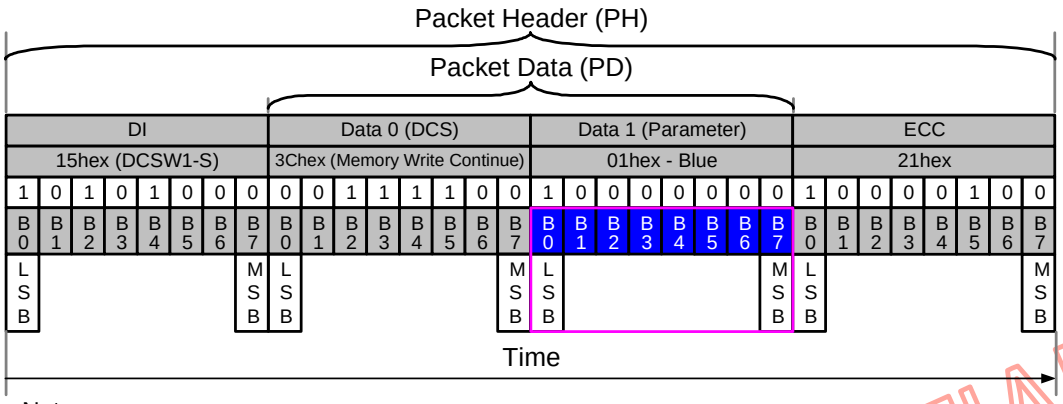
The MCU can send to the display module a following packet.



Notes:

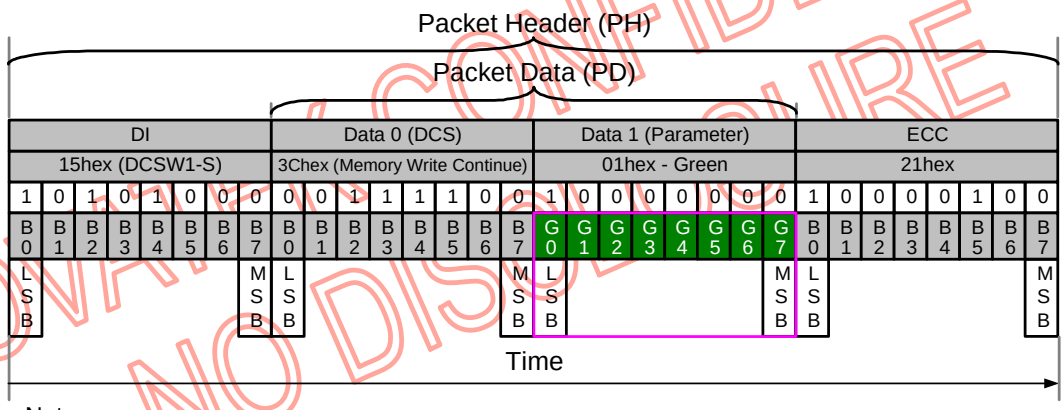
1. Memory Write (2Ch) or Memory Write Continue (3Ch)
2. It is possible that one pixel information is split in two or three different packets which are ending and starting as follows:
   - R - GB (2 packets)
   - RG - B (2 packets)
   - R - G - B (3 packets)
3. Packet can include several pixel (Not only one pixel as in this example)

One Pixel Write (DCSW-L) - Example 1



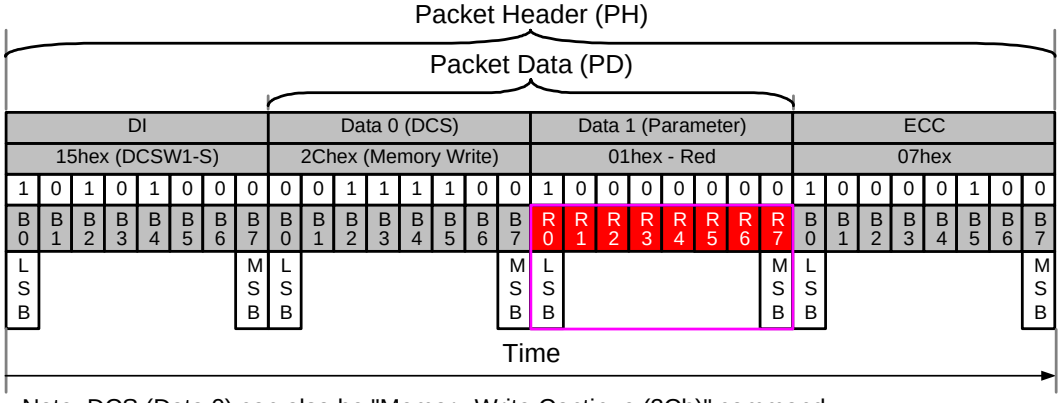
Notes:
1. DCS (Data 0) can not be "Memory Write (2Ch)" command.
   It must be always be "Memory Write Continuec(3Ch)" .
2. Previous data byte was G[0:7]

Blue Subpixel Write (DCSW1-S) - Example 2



Notes:
1. DCS (Data 0) can not be "Memory Write (2Ch)" command.
   It must always be "Memory Write Continue (3Ch)".
2. Previous data byte was R[0:7]

Green Subpixel Write (DCSW1-S) - Example 3

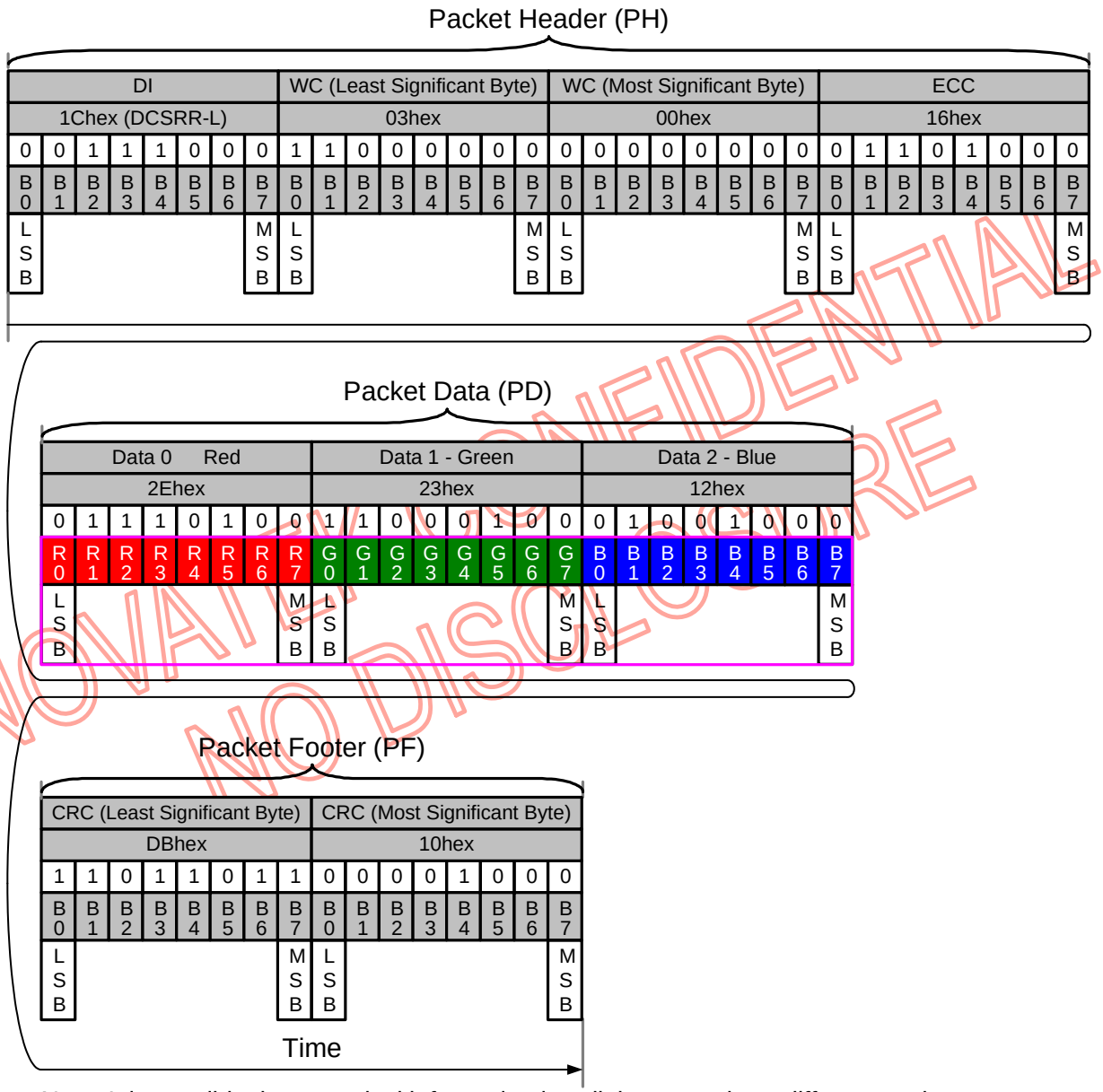


Note: DCS (Data 0) can also be "Memory Write Continue (3Ch)" command.

Red subpixel Write (DCSW1-S) - Example 4

- 24 bit/pixel Reading

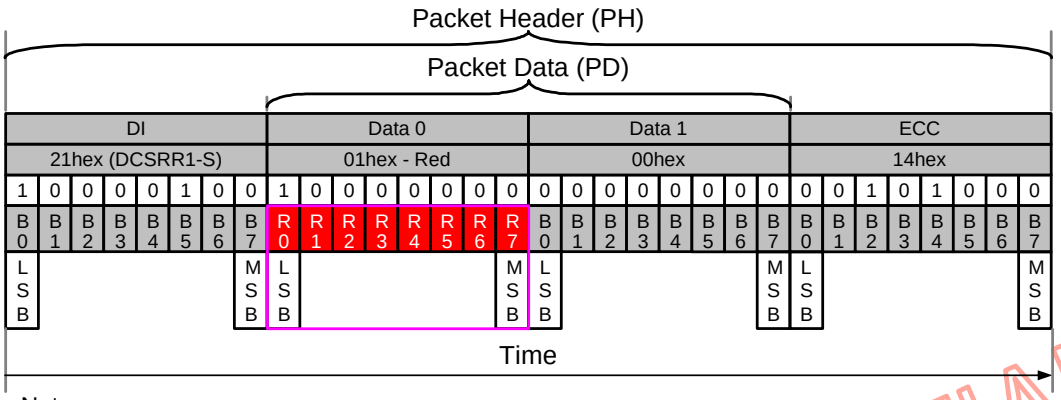
The display module can send to the MCU following packets after the MCU has a read command “Memory Read (2Eh)” or “memory Read Continue (3Eh)”.



Note: It is possible that one pixel information is split in two or three different packets:

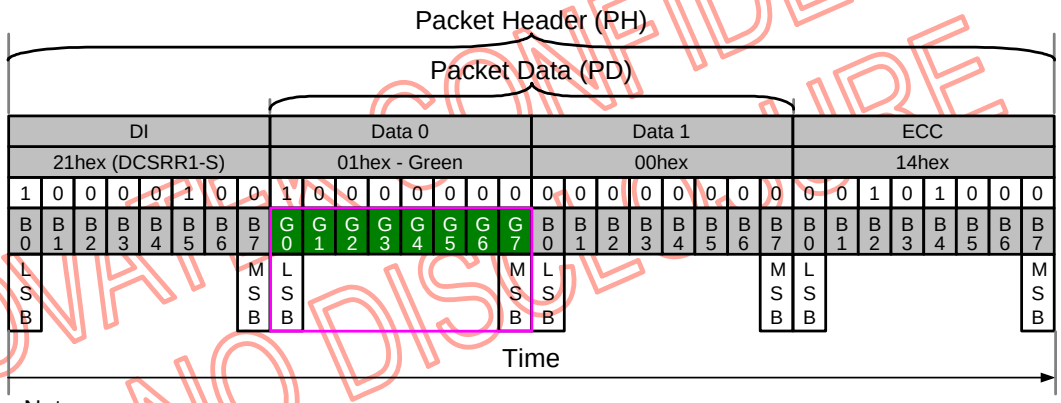
- R - GB (2 packets)
- RG - B (2 packets)
- R - G - B (3 packets)

One Pixel Read Response (DCSRR-L) - Example 1



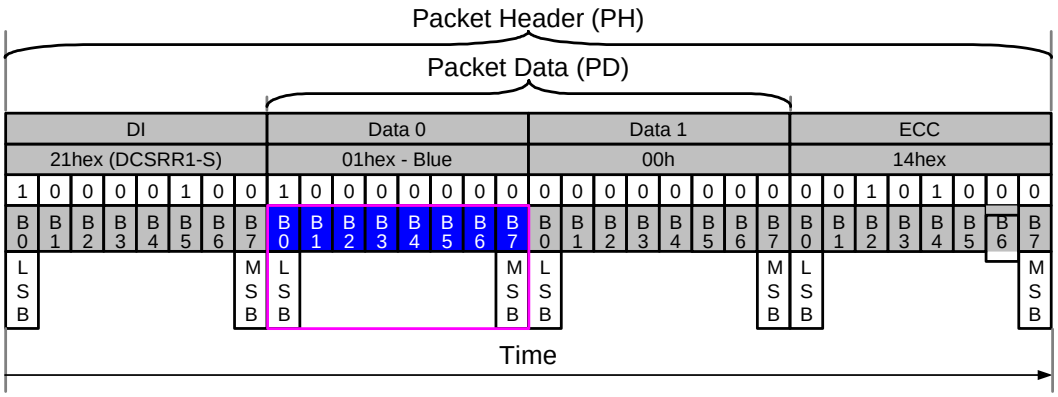
Notes:
1. Data 1 is always "00h".
2. Previous data byte was B[0:7]

Red Subpixel Response (DCSRR1-S) - Example 2



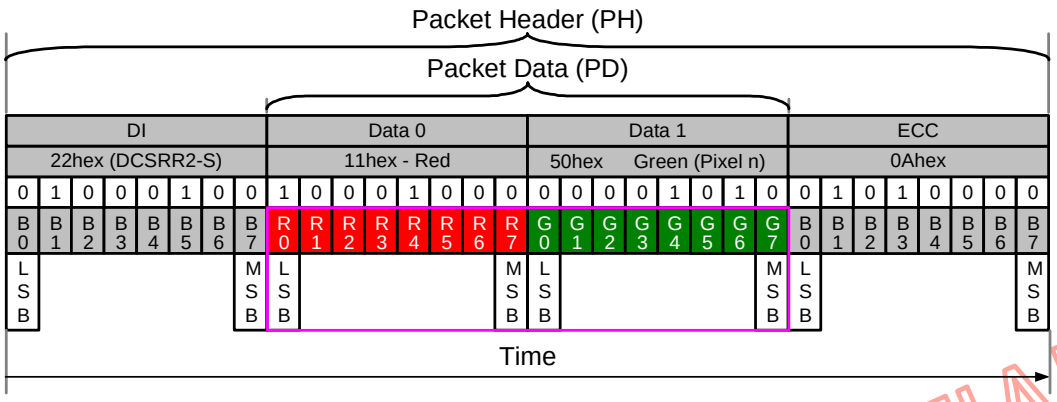
Notes:
1. Data 1 is always "00h".
2. Previous data byte was R[0:7]

Green Subpixel Response (DCSRR1-S) - Example 3

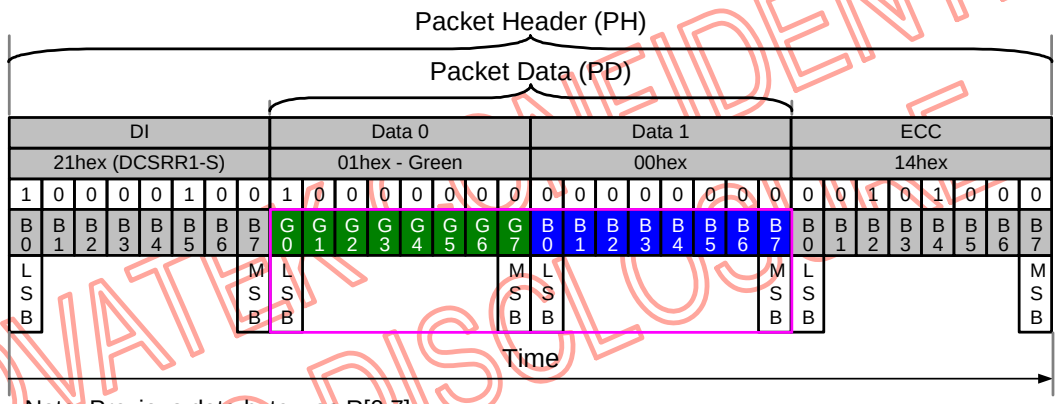


Note: Data 1 is always "00h".

Blue subpixel Response (DCSRR1-S) - Example 4

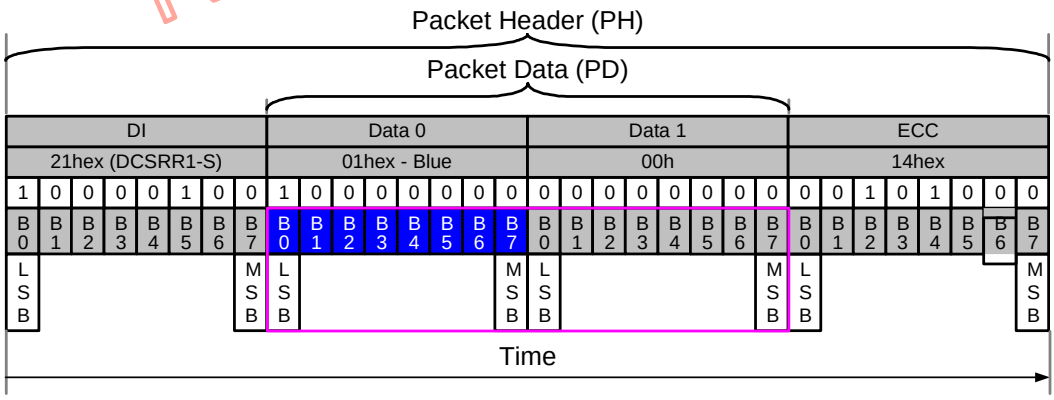


Red and Green Subpixels Response (DCSRR2-S) - Example 5



Note: Previous data byte was R[0:7]

Green and Blue Subpixels Response (DCSRR2-S) - Example 6



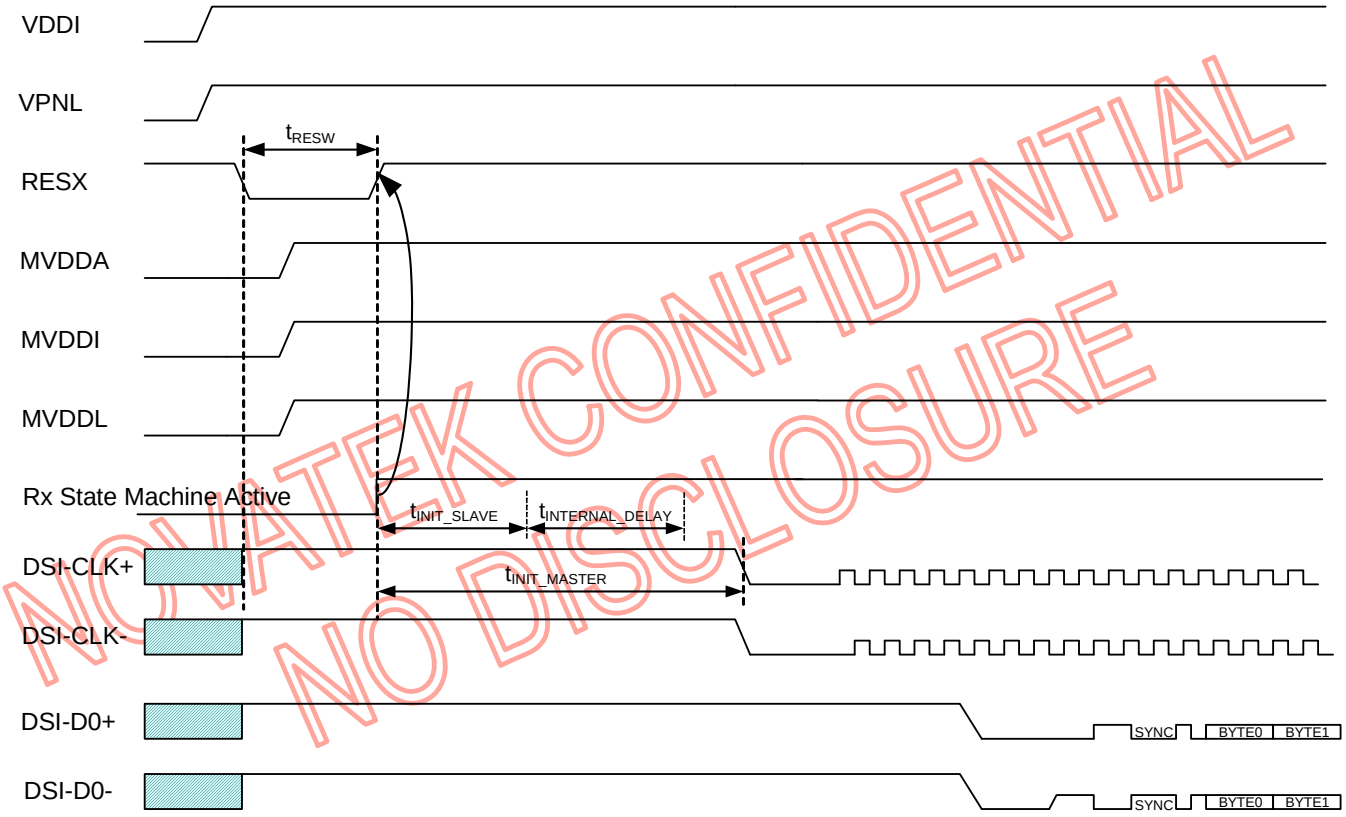
Note: Previous data byte G[0:7]

Blue and Red Subpixels Response (DCSRR2-S) - Example 7

5.3.4 System Power-Up and Initialization

After power-on, the host processor shall observe an initialization period, t_{INIT}, during which it shall drive a sustained Tx-Stop state (LP-11) on all Lanes of the Link.

Figure below illustrates an example power-up sequence for a DSI display module. In the figure, a hardware reset (RESX) mechanism is assumed for initialization. Internally within the display module, de-assertion of RESX could happen after both IO and core voltages were ramped up. In this example, the host's t_{INIT_MASTER} parameter is programmed for driving LP-11 for a period longer than the sum of t_{RESW}, t_{INIT_SLAVE} and $t_{INTERNAL\_DELAY}$. The display module may ignore all Lane activities during this time.



$(t_{INIT\_MASTER}) >= (t_{RESW} + t_{INIT\_SLAVE} + t_{INTERNAL\_DELAY})$

Symbol	Parameter	Min	Typ	Max	Units
t_{INIT_MASTER}	MIPI Tx initialize time	5	-	-	mS
t_{RESW}	Reset "L" pulse width	Note	-	-	µS
t_{INIT_SLAVE}	MIPI Rx initialize time	4	-	-	mS
$t_{INTERNAL\_DELAY}$	Internal delay time.	500	-	-	µS

Note: See section "7.6.7 Reset Input Timing"

5.4 MDDI Interface

The NT35510 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following lines: DATA0_P/M, DATA1_P/M and STB_P/M.

The specifications of MDDI supported by the NT35510 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA).

The NT35510 offers the Bi-direction Link to use for the register and display data read / write.

For power saving, the NT35510 offers both Hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption.

The NT35510 supports the MDDI Type-I and Type-II of the MDDI specifications Version 1.2 and the application diagram is illustrated as Fig. 5.4.1.

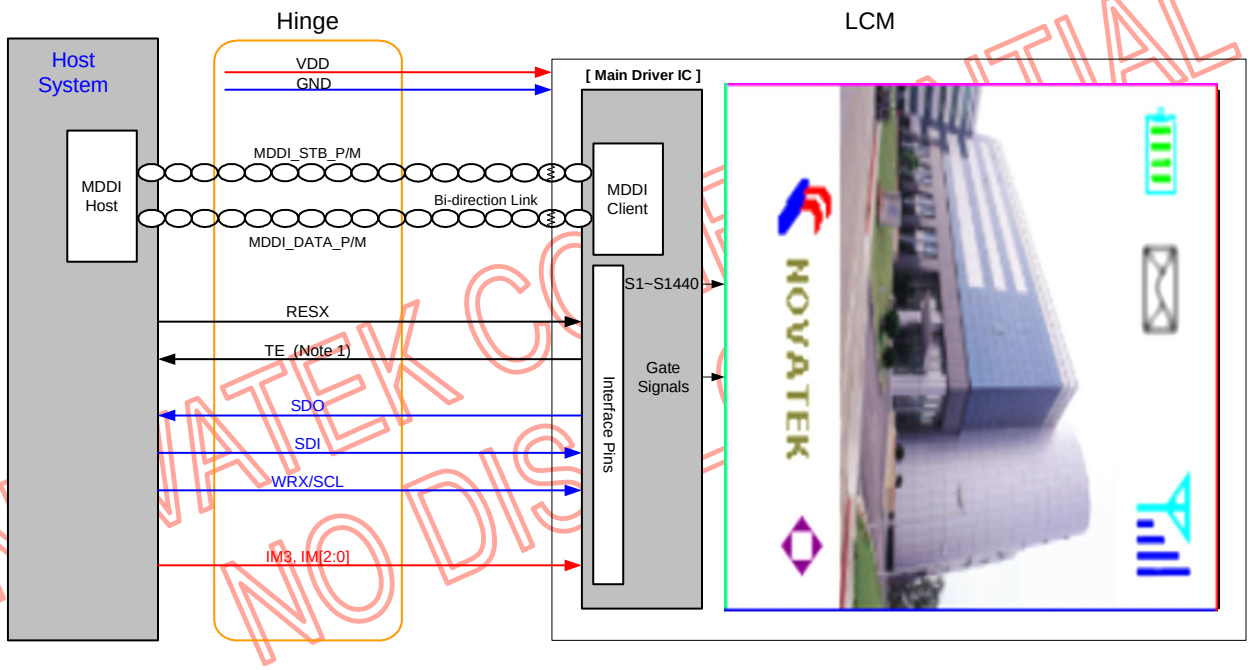


Fig. 5.4.1 MDDI application diagram

Notes:

1. Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effect.
2. When enter to the MDDI interface from other interface, the Host needs to wait 100ms and can start to send any packet. For example wake up packet.
3. After shutting down the MDDI interface the Host needs to wait 500ns and can start to send wake up packet to wake up the MDDI link.
4. The terminal resistors are embedded between MDDI_DATA0_P/M, MDDI_DATA1_P/M and MDDI_STB_P/M.

5.4.1 MDDI Link Protocol by The NT35510

The NT35510's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol.

DO NOT send any packets that are not supported by the NT35510 into a system containing the NT35510. Supported MDDI packets are as follows:

Table 5.4.1 Summary of MDDI packets supported by NT35510

NT35510 MDDI packets	Packet Name	Packet Type	Direction	Supported Type
Link Control Packet	Sub-frame header packet	15359 (0x3BFF)	Forward	Type I/Type II
	Filler packet	0	Forward/Reverse	Type I/Type II
	Link Shutdown packet	69 (0x45)	Forward	Type I/Type II
	Reverse link encapsulation packet	65 (0x41)	Forward	Type I Only
	Round-trip delay measurement packet	82 (0x52)	Forward	Type I/Type II
	Forward link skew calibration packet	83 (0x53)	Forward	Type I/Type II
Client Status and Control Packet	Client capability packet	66 (0x42)	Reverse	Type I Only
	Client request and status packet	70 (0x46)	Reverse	Type I Only
	Register access packet	146 (0x92)	Forward/Reverse	Type I/ Type II (Forward) Type I Only (Reverse)
Basic Media Stream Packet	Video stream packet	16 (0x10)	Forward	Type I/Type II
	Flexible video stream packet	20 (0x14)	Forward	Type I/Type II
	Windowless video stream packet	22 (0x16)	Forward	Type I/Type II

5.4.2 MDDI Link Packet Descriptions by the NT35510

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub-frame Header Packet

Packet Length	Packet Type =0x3bff	Unique word = 0x005a	Reversed 1	Sub-frame Length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0x3bff

Unique Word: unique word is 0x005a

Reserved 1: not used (set to zero)

Sub-frame Length: specify the number of bytes per sub-frame

Protocol version: set to zero

- Bit [15:2] – Reserved for future expansion. These should be set to all zero.
- Bits[1:0] – Sub-frame operational mode

  "00" – Sub-frame lengths strictly followed.

  "01" – Sub-frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame length has been transmitted.

  "10" – Sub-frame lengths are unlimited. No more sub-frame packets are required tobe transmitted after the first Sub-Frame packet at startup.

Sub-frame Count: specify the number of sub-frame header packet

Media-frame Count: specify the number of media-frames

CRC: error check

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

Filler Packet

Packet Length	Packet Type=0	Filler Bytes (all zero recommended)	CRC
2 bytes	2 bytes	(Packet_Length 4) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0

Filler Bytes: set to zero

CRC: error check

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.

Link Shutdown Packer

Packet Length	Packet Type=69	CRC	All Zero
2 bytes	2 bytes	2 bytes	(Packet_Length 4) bytes

Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 69
CRC: error check
All Zero: set to zero (Type I: size is 16 bytes, Type II: size is 32 bytes)

Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.

Reverse Link Encapsulation Packet

Packet Length	Packet Type=65	hClient ID	Reverse Link Flags	Reverse Rate Divisor	Turn-Around 1 Length	Turn-Around 2 Length
2 bytes	2 bytes	2 bytes	1 bytes	1 bytes	1 bytes	1 bytes

Parameter CRC	All Zero 1	Turn-Around 1	Reverse Data Packets	Turn-Around 2	All Zero 2
2 bytes	8 bytes	x bytes	(Packet_Length -x – y – 26) bytes	y bytes	8 bytes

Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 65
hClient ID: set to zero
Reverse Link Flags:

- Bit 0 – 0: No packet request
  1: Host needs the Client Capability Packet
- Bit 1 – 0: No packet request
  1: Host needs the Client Request and Status Packet
- Bit [7:2] – set to zero

Reverse Rate Divisor: reverse data rate = reverse link data clock
Turn-Around 1 Length: the length of Turn-Around 1 is the forward link data rate
Turn-Around 2 Length: the length of Turn-Around 2 is determined by Round-trip delay of the link
Parameter CRC: error check
All zero: set to zero
Turn-Around 1: First turn-around period
Reverse Data Packets: A series of data packets transferred from the client to host
Turn-Around 2: The second turn-around period

Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

Round Trip Measurement Packet

Packet Length	Packet Type=82	hClient ID	Parameter CRC
2 bytes	2 bytes	2 bytes	2 bytes

Guard Time 1	Measurement Period	All Zero	Guard Time 2
64 bytes	64 bytes	2 bytes	64 bytes

Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 82
hCilent ID: set to zero
Parameter CRC: error check
Guard Time 1: allow overlap of the host and client
Measurement Period: a 64 bytes window to allow the client to respond
All Zero: set to zero
Guard Time 2: allow overlap of the measurement period by the client

Fig. 5.4.2 illustrates the timing of events during the Round-Trip Delay Measurement Packet.

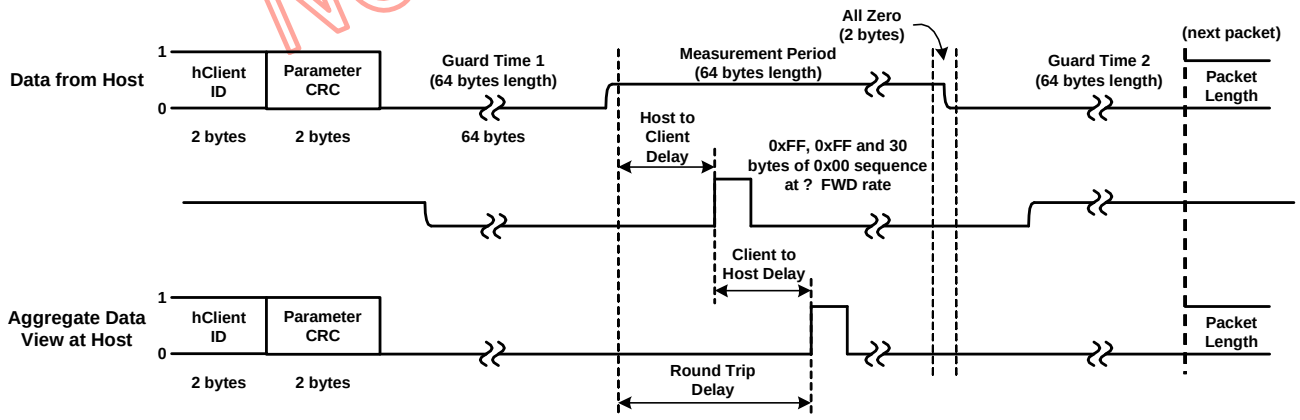


Fig. 5.4.2 Round-Trip Delay Measurement Timing

Forward Link Skew Calibration Packet

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_DATA signals with respect to the MDDI_STB signal. Without delay skew compensation the maximum data rate must be limited to account for the worst-case variation in these delays. It is recommended that this packet only be sent when the forward link data rate is configured to 50 Mbps or lower. After sending this packet to calibrate the client the data rate may be stepped up above 50 Mbps. With the data rate set too high during the skew calibration process the client might synchronize to an alias of the bit period which would cause the delay skew compensation setting to be off by more than one bit time, resulting in erroneous data clocking. The greatest possible Interface Type must be selected prior to sending the Forward Link Skew Calibration Packet so that all existing data bits are calibrated. The client must indicate its ability to support the Forward Link Skew Calibration Packet via bit 19 of Client Feature Capability Indicators field of the Client Capability Packet.

Prior to performing skew calibration the host must not send data faster than the rate specified by the Pre-calibration Data Rate Capability field of the Client Capability Packet. However, after calibration is performed, the host may send data up to the rate defined by the Post-calibration Data Rate Capability field. It is recommended that the host send the Forward Link Skew Calibration Packet at regular intervals to correct changes in the relative delay between the different signal pairs due to changes in temperature.

Forward Link Skew Calibration Packet

Packet Length	Packet Type=83	hClient ID	Parameter CRC	All Zero 1	Calibration Data Sequence	All Zero 2
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	Packet Length - 22 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 83

hCilent ID: set to zero

Parameter CRC: error check from packet length to the hClient ID.

All Zero 1:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field ensures that there will be a transition on MDDI_STB at the beginning of the Calibration Data Sequence field. It also provides sufficient time for the client core logic to change the mode of the clock recovery circuit from using the XOR of MDDI_Data0 and MDDI_STB to simply using MDDI_STB as the recovered clock.

Calibration Data Sequence:

a data sequence that causes the MDDI_Data signals to toggle at every data period. The length of the Calibration Data Sequence field is determined by the interface type being used on the forward link. During the Calibration Data Sequence the MDDI host controller sets all MDDI_Data signals equal to the strobe signal. The client clock recovery circuit must use only MDDI_STB rather than MDDI_STB XOR MDDI_Data0 to recover the data clock while the Calibration Data Sequence field is being received by the client. Depending on the exact phase of MDDI_STB at the beginning of the Calibration Data Sequence field the Calibration Data Sequence will be one of the following based on the interface Type being used when this packet is sent:

- Type 1 – (64 byte data sequence) AAh, AAh … or 55h, 55h…
- Type 2 – (128 byte data sequence) CCh, CCh … or 33h, 33h…

All Zero 2:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field provides sufficient time for the client core logic to change the mode of the clock recovery circuit back to the original state, from using MDDI_STB as the recovered clock to using the XOR of MDDI_Data0 and MDDI_STB.

Client Capability Packet

It is recommended that the client send a Client Capability Packet to the host after forward link synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

Client Capability Packet

Packet Length	Packet Type=66	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	1 bytes

Number of Alt Display	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size
1 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	4 bytes

Color Map RGB Width	RGB Capability	Monochrome Capability	Reversed 1	Y Cb Cr Capability	Bayer Capability	Revered 2
2 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes	2 bytes

Client Feature Capability	Max Video Frame Rate	Min Video Frame Rate	Min Sub-frame Rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample Rate Capability
4 bytes	1 bytes	1 bytes	2 bytes	2 bytes	2 bytes	2 bytes

Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name
1 bytes	1 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes

Product Code	Revered 3	Serial Number	Week of Mfr	Year of Mfr	CRC
2 bytes	2 bytes	4 bytes	1 bytes	1 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 66
cClient ID: set to zero
Protocol Version: set to 0002h
Min Protocol Version: specify the minimum protocol version (0001h)
Pre-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)
Interface Type Capability: Client can function in Type 2 (2-bit) mode on the forward link (01h)
Number of Alt Displays: set to zero
Post-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)
Bitmap Width: specify the width of the bitmap
Bitmap Height: specify the height of the bitmap
Display Window Width: specify the width of the display window
Display Window Height: specify the height of the display window
Color Map Size: set to zero
Color Map RGB Width: set to zero
RGB Capability: specify the resolution of RGB format (8888h)
Monochrome Capability: set to zero
Reserved 1: set to zero
Y Cb Cr Capability: set to zero
Bayer Capability: set to zero
Reserved 2: set to zero
Client Feature Capability Indicators: 00CC8000h
Maximum Video Frame Rate Capability: specify the maximum video frame (3Ch)
Minimum Video Frame Rate Capability: specify the minimum video frame (00h)
Minimum Sub-frame Rate: specify the minimum sub-frame rate (01h)
Audio Buffer Depth: set to zero
Audio Channel Capability: set to zero
Audio Sample Rate Capability: Set to zero
Audio Sample Resolution: set to zero
Mic Audio Sample Resolution: set to zero
Mic Sample Rate Capability: set to zero
Keyboard Data Format: set to zero
Pointing Device Data Format: set to zero
Content Protection Type: set to zero
Mfr Name: set to B9F6h
Product Code: set to 5510h
Reserved 3: set to zero
Serial Number: set to zero
Week of Manufacture: set to zero
Year of Manufacture: 0Ah
CRC: error check

Client Request and Status Packet

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Client Request and Status Packet

Packet Length	Packet Type=70	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 bytes	2 bytes	2 bytes	2 bytes	1 bytes	1 bytes	2 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 70
cClient ID: set to zero
Reverse Link Request: specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.
CRC Error Count: count the number of CRC errors occurred
Client Status:

- Bit 0 – 1: capability has changed
  0: capability has not changed
- Bit 1 – indicates the client has detected an error
- Bit [7:2] – set to zero

Client Busy Flags:

- Bit 0 – bitmap block transfer function is busy
- Bit 1 – bitmap area fill function is busy
- Bit 2 – bitmap pattern fill function is busy
- Bit 3 – the graphics subsystem is busy
- Bit [15:4] – set to zero

CRC: error check

Register Access Packet

Register Access Packet is utilized when setting instruction to the NT35510. This packet cannot be used for RAM access.

Register Access Packet

Packet Length	Packet Type =146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	(Packet Length 14) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 146

bClient ID: set to zero

Read/Write Info:

Bits [15:14]	Read/Write Flags
00	Write
01	Reserved
10	Read
11	Response to read

Bit [13:0] – specifies the number of 32-bit register data list items to be transferred in the Register Data List Filed.

Register Address: upper bits shall set to zero

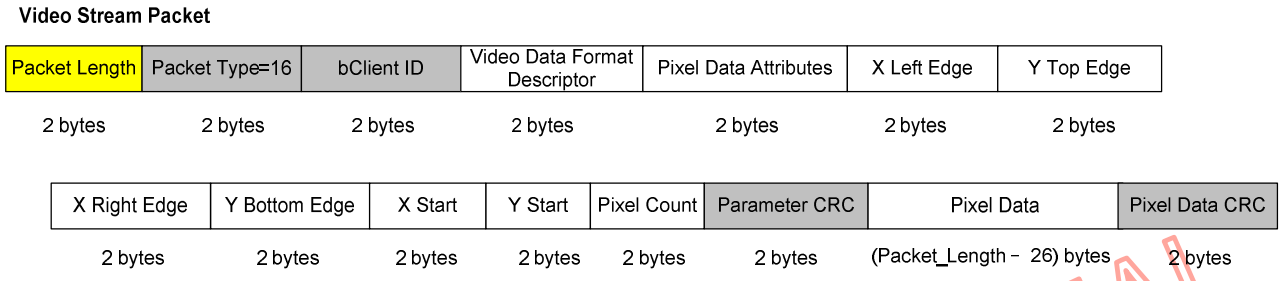
Parameter CRC: error check from packet length to the register address

Register Data List: written (or read) registers to (from) client

Register Data CRC: error check of the register data list

Video Stream Packet

The NT35510 supports the Video Stream Packet to transfer display data including RGB data to RAM.



Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 16
bClient ID: set to zero
Video Data Format Descriptor

[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of NT36551 (00C3h)
X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.
Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field
X Right Edge: Specify the X coordinate of the right edge of the window being updated.
Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.
X Start: Specify X start address for the first pixel in the Pixel Data field below.
Y Start: Specify Y start address for the first pixel in the Pixel Data field below.
Pixel Count: specify the number of pixels
Parameter CRC: error check from packet length to the pixel count
Pixel Data: the raw video data
Pixel Data CRC: error check of the pixel data

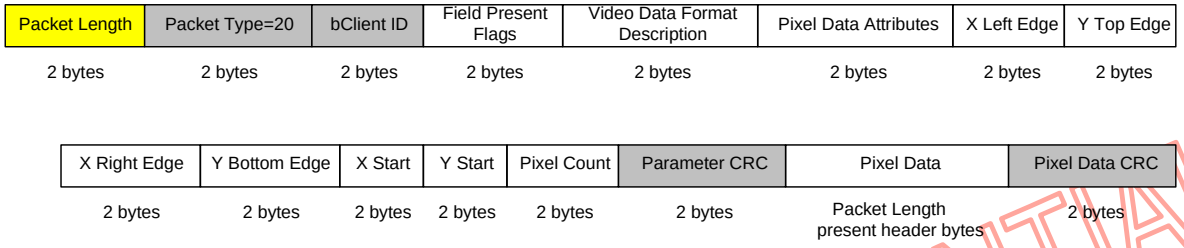
Table 5.4.1 Pixel Data Format

MDDI date byte		D7	D6	D5	D4	D3	D2	D1	D0	Color
RGB 5:6:5	Byte n	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color (1 pixel/ 16 bits RGB format)
	Byte n+1	R4	R3	R2	R1	R0	G5	G4	G3	
RGB 6:6:6	Byte n	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1 pixel/ 18 bits RGB format)
	Byte n+1	R3	R2	R1	R0	G5	G4	G3	G2	
	Byte n+2	B5	B4	B3	B2	B1	B0	R5	R4	
RGB 8:8:8	Byte n	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color (1 pixel/ 24 bits RGB format)
	Byte n+1	G7	G6	G5	G4	G3	G2	G1	G0	
	Byte n+2	R7	R6	R5	R4	R3	R2	R1	R0	

Flexible Video Stream Packet

The NT35510 supports the Flexible Video Stream Packet to transfer display data including RGB data to RAM. This allows for a reduction in the number of fields sent in an environment where one or more fields are not changing values.

Flexible Video Stream Packet



Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 20
bClient ID: set to zero
Field Present Flags: indicates the field in the packet is present (value “1”) or not present (value “0”).
- Bit 0: indicates the presence of the Video Data Format Description Field.
- Bit 1: indicates the presence of the Pixel Data Attributes Field.
- Bit 2: indicates the presence of the X Left Edge Field.
- Bit 3: indicates the presence of the Y Top Edge Field.
- Bit 4: indicates the presence of the X Right Edge Field.
- Bit 5: indicates the presence of the Y Bottom Edge Field.
- Bit 6: indicates the presence of the X Start Field.
- Bit 7: indicates the presence of the Y Start Field.
- Bit 8: indicates the presence of the Pixel Count Field.
- Bits [15:9] are all “0”.

Video Data Format Descriptor

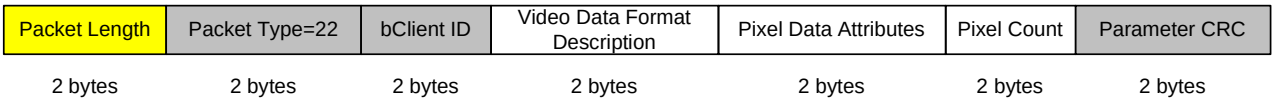
[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

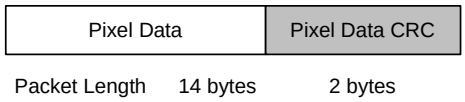
X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.
Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field
X Right Edge: Specify the X coordinate of the right edge of the window being updated.
Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.
X Start: Specify X start address for the first pixel in the Pixel Data field below.
Y Start: Specify Y start address for the first pixel in the Pixel Data field below.
Pixel Data Attributes: The pixel data is written to RAM buffer of NT35510 (00C3h)
Pixel Count: specify the number of pixels
Parameter CRC: error check from packet length to the pixel count
Pixel Data: the raw video data
Pixel Data CRC: error check of the pixel data

Windowless Video Stream Packet

The NT35510 supports the Windowless Video Stream Packet to transfer display data including RGB data to RAM. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information.

Windowless Video Stream Packet





Packet Contents:

Packet Length: packet length not including the packet length field
Packet Type: packet type is 22
bClient ID: set to zero
Video Data Format Descriptor

[15:12]	[11:8]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of NT36551 (00C3h)
Pixel Count: specify the number of pixels
Parameter CRC: error check from packet length to the pixel count
Pixel Data: the raw video data
Pixel Data CRC: error check of the pixel data

5.4.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.

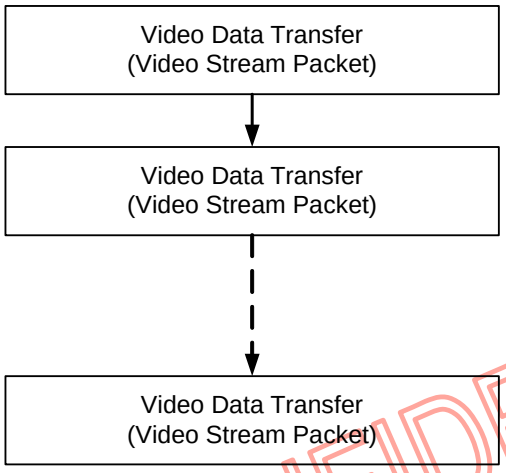


Fig. 5.4.3 Writing Video Data to Memory Sequence

5.4.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.

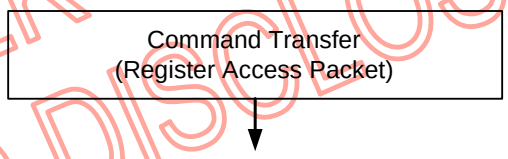


Fig. 5.4.4 Writing Register Sequence

5.4.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2E00h) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

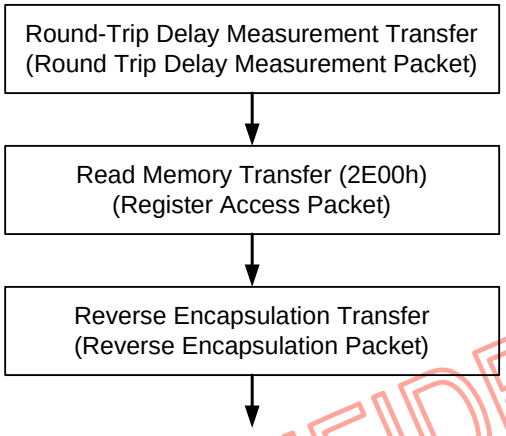


Fig. 5.4.5 Reading Video Data from Memory Sequence

Notes:

1. X addresses for memory data read is set by 2A00h and 2A01h (XS[15:0]).
   The parameters of 2A00h and 2A01h are stored on relative registers while command 2A00h~2A03h are executed completely. See also section “6.1 User Command Set” and Note 2.
2. Y addresses for memory data read is set by 2B00h and 2B01h (YS[15:0]).
   The parameters of 2B00h and 2B01h are stored on relative registers while command 2B00h~2B03h are executed completely. See also section “6.1 User Command Set” and Note 2.

5.4.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

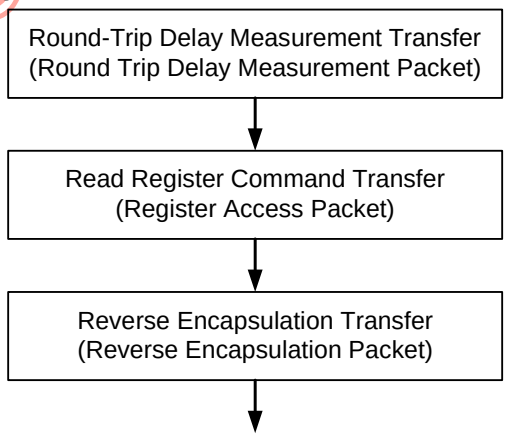


Fig. 5.4.6 Reading Register Sequence

5.4.7 Hibernation Setting

The Client MDDI of the NT35510 provides a hibernation setting. The methods for waking up the hibernation mode can be determined based on actual usage.

Wake-up	Condition
Host-Initiated Wake-up	Wake up the MDDI link by MDDI Host

Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained.

Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

Hibernation setting sequence

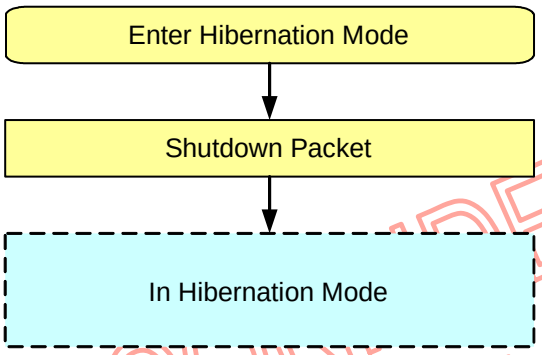


Fig. 5.4.7 Enter Hibernation Mode Sequence

Hibernation Wake-up sequence

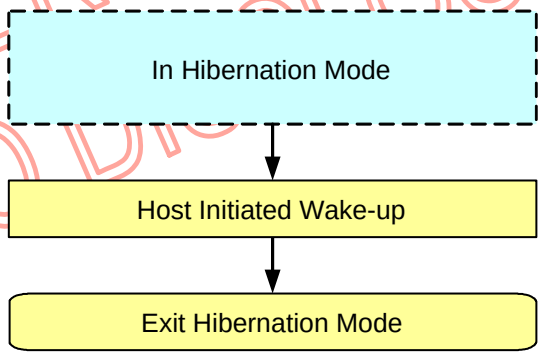


Fig. 5.4.8 Hibernation Wake-up Sequence

5.4.8 MDDI Deep Standby Mode Setting

The Client MDDI of the NT35510 includes a MDDI deep standby mode setting so it can enter a off state and reduce power consumption during Hibernation mode.

The MDDI enters Hibernation mode when a Shutdown Packet is sent. The standby power needs of the Client MDDI can be reduced, even while the MDDI Link is maintained in Hibernation mode.

When entering MDDI deep standby mode, the NT35510 stops operation rather than maintaining Hibernation mode. Input low pulse 3 msec from RESX pin to cancel deep standby mode, after which a Host-Initiated Wake-up should cancel the Hibernation mode.

When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

Follow the sequence indicated in the VESA MDDI specifications when initiating or canceling the Hibernation mode.

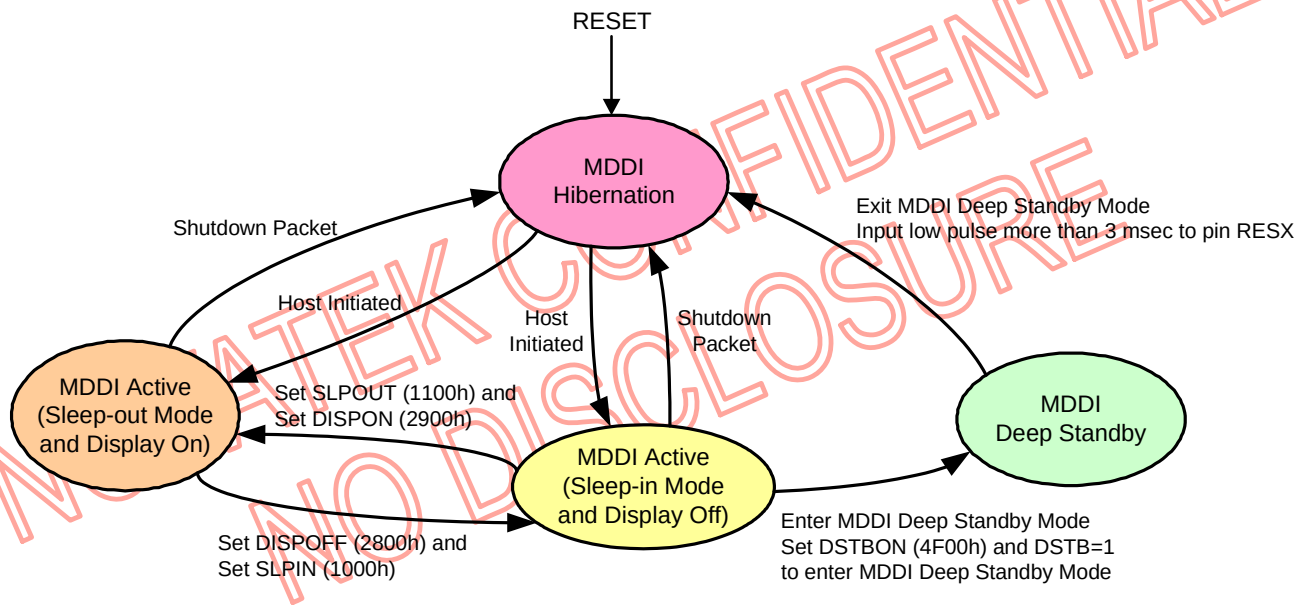


Fig. 5.4.9 State Transitions in MDDI Deep Standby Mode

Note: When the NT35510 is in the MDDI Hibernation mode or MDDI deep standby mode, both links are in the link hibernation states.

MDDI Deep Standby Mode Sequence

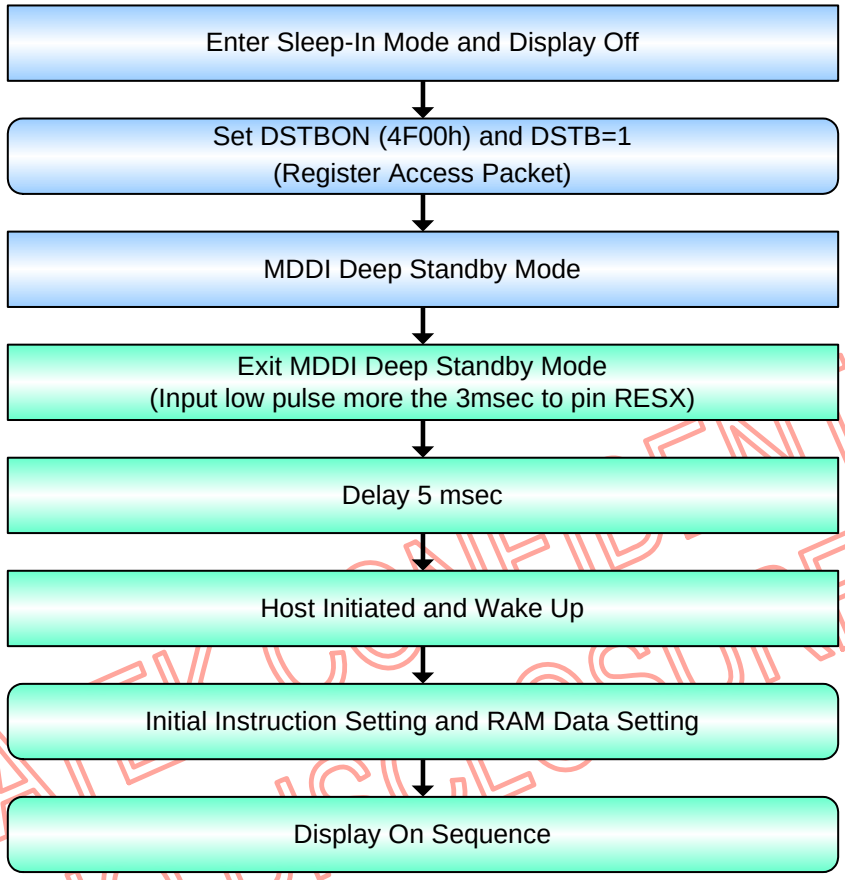


Fig. 5.4.10 Enter and Exit MDDI Deep Standby Mode Sequence

Note: When in MDDI Deep Standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

5.5 Interface Pause

By using parallel interface, it is possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the CSX (Chip Select Line) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35510 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the CSX (Chip Select Line) is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the CSX (Chip Select Line) is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Parallel Interface Pause

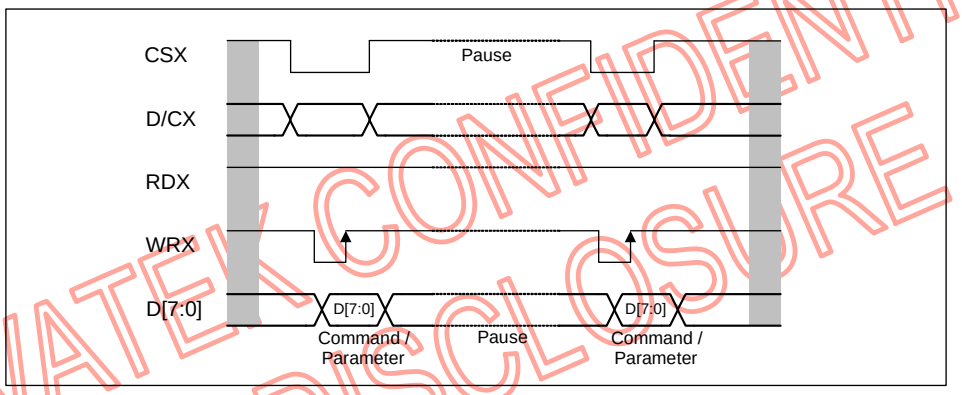


Fig. 5.5.1 Parallel bus protocol, write mode – paused by CSX

Serial Interface Pause

16-bit SPI interface does not support "Pause Mode"

MIPI Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.
1) Same receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => …
2) Different receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => …

The means that "=>" symbol means a pause on DSI.

5.6 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See ***Fig. 5.6.1***)

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See ***Fig. 5.6.2***)

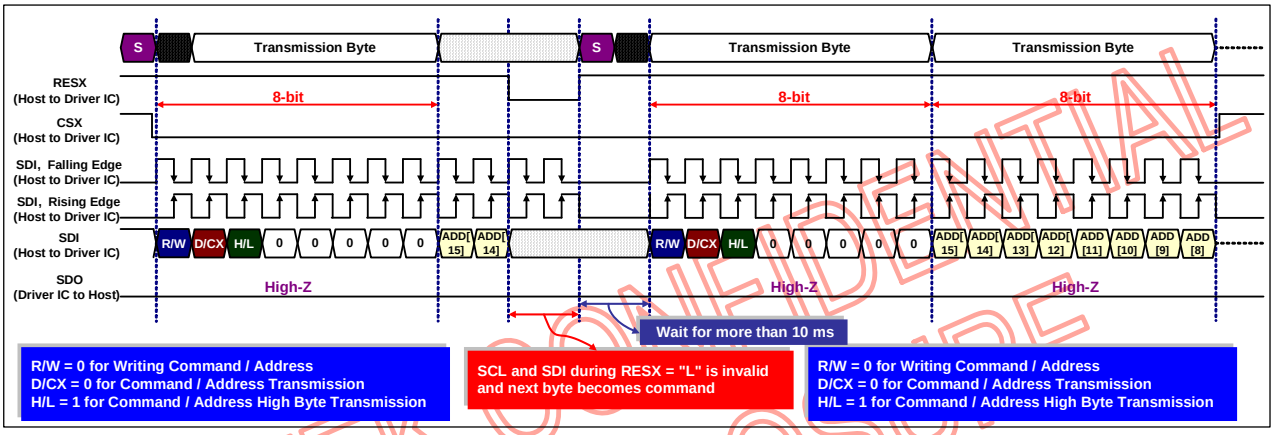


Fig. 5.6.1 Serial bus protocol, write mode – interrupted by REX

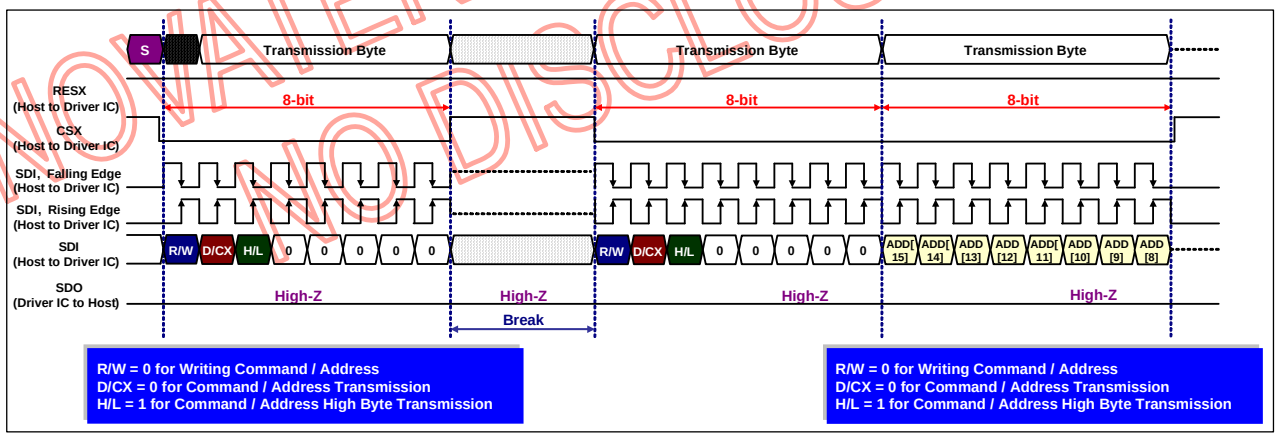
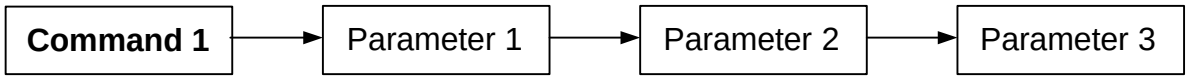


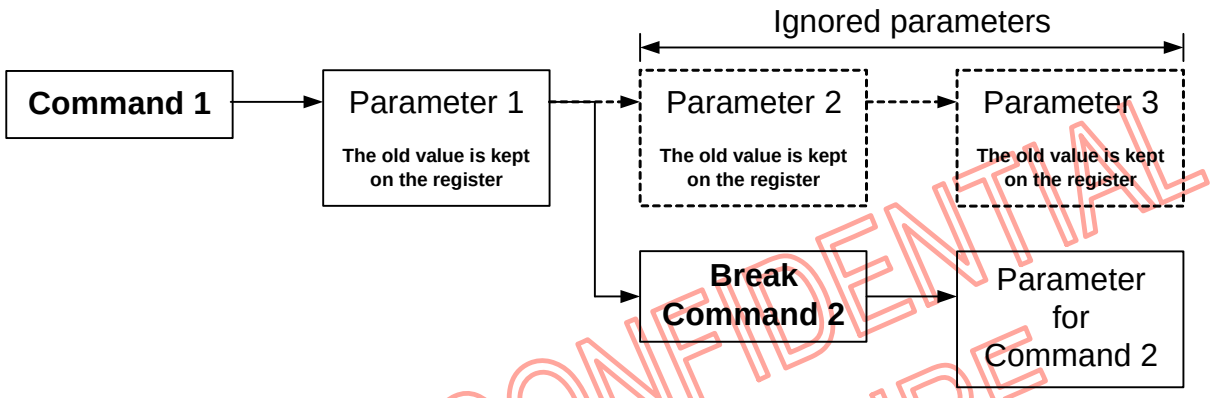
Fig. 5.6.2 Serial bus protocol, write mode – interrupted by CSX

Display data transfer break is illustrated for reference purposes below.

Without break



With break (See and check also exceptions*)



Break can be e.g. another command or noise pulse.

Fig. 5.6.3 Break during Parameter

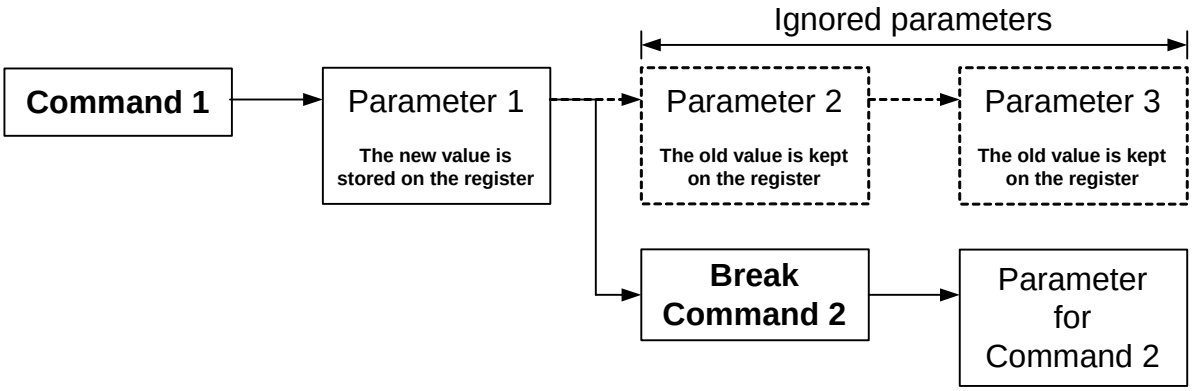
*) See also an exception on section “6.1 User Command Set” and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

The NT35510 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

Except MIPI interface, the data transfer break mechanism illustrated for reference purposes below.



5.7 Display Module Data Transfer Modes

The NT35510 has 3 kinds of color mode for transferring data to the frame Memory. There are 16-bit color per pixel, 18-bit color per pixel and 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

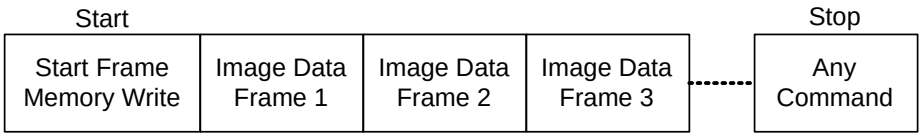


Fig. 5.7.1 Data Transfer Method 1

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

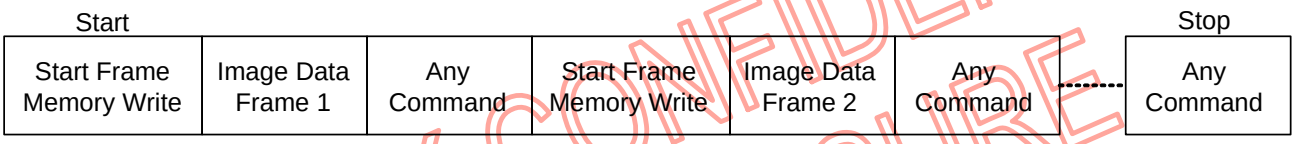


Fig. 5.7.2 Data Transfer Method 2 with "Start Frame Memory Write" Break

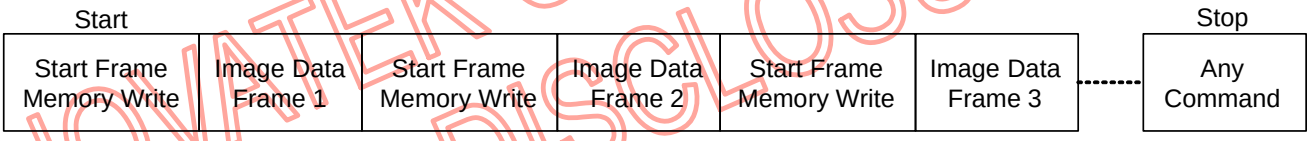


Fig. 5.7.3 Data Transfer Method 2 with "Any Command" Break

NOTES:

1) The Frame Memory can contain odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

2) "Memory Write Continue (3Ch)" or "Memory Read Continue (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any Command" has stopped the memory writing or reading.

3) "Any Command" can be as same as "Start Frame Memory Write".

5.8 RGB Interface

5.8.1 General Description

For direct interface with both graphic controller and MPU, NT35510 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[23:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

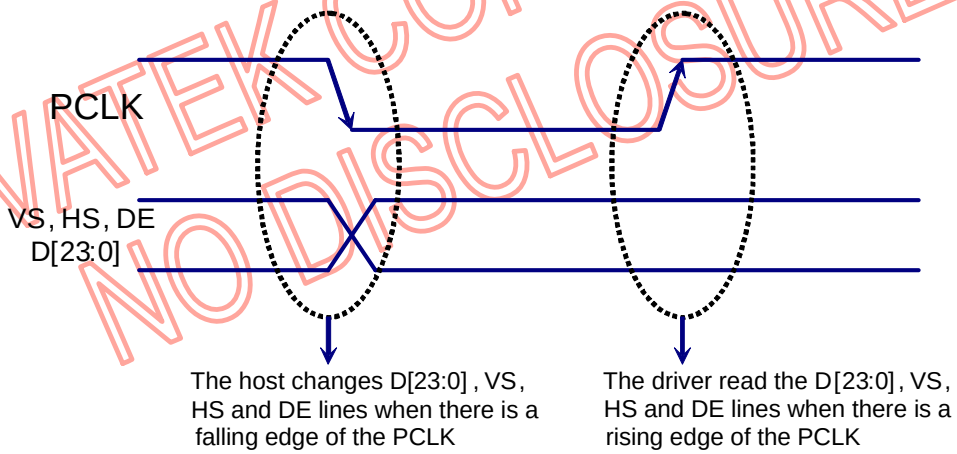
Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative (“0”, low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative (“0”, low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive (“1”, high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bit: R7-R0, G7-G0 and B7-B0;18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= “1” and there is a rising edge of PCLK). D[23:0] can be “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the follow figure.



Note: PCLK is an unsynchronized signal (It can be stopped)

5.8.2 RGB Interface Timing Chart

The image information must be correct on the display, when the timings are in range on the interface.
However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

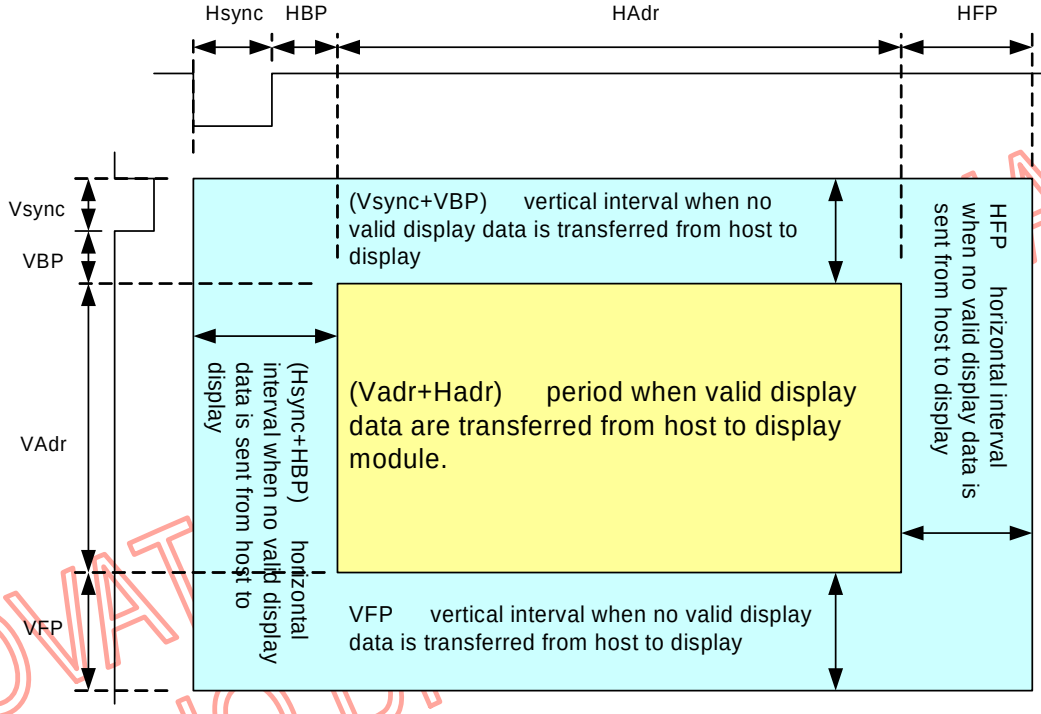


Fig. 5.8.1 RGB interface general timing diagram

5.8.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VFP[7:0], VBP[7:0] HFP[7:0], HBP[7:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC only)	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35510 DDI.

In RGB Mode 2, back porch of Vsync VBP is defined by VBP[7:0] of RGBCTR command. And back porch of Hsync HBP is defined by HBP[7:0] of RGRCTR command. Front porch of Vsync VFP is defined by VFP[7:0] of RGBCTR command. And front porch of Hsync HFP is defined by HFP[7:0] of RGBCTR command.

Note: VBP[7:0]=Vsync+VBP and HBP[7:0]=Hsync+HBP.

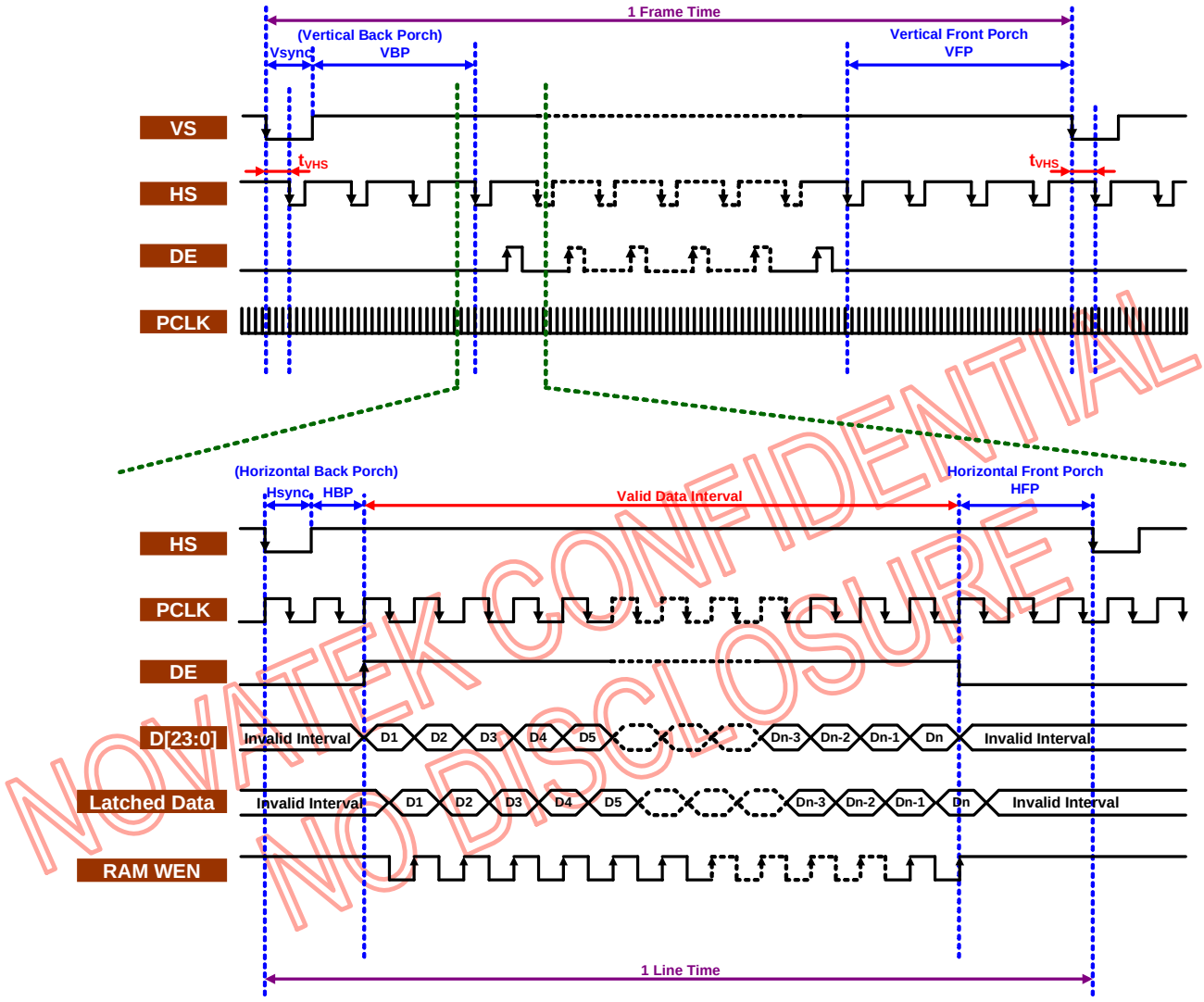


Fig. 5.8.2 Video signal data writing method in RGB Mode 1 Interface

Notes:

1. Constraint:

V-Back Porch (Vsync+VBP)≧ 5 HS lines, V-Front-Borch (VFP) ≧ 2 HS lines

Vsync+VBP+VFP (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch)

H-Back Porch (Hsync+HBP)≧ 5 PCLK clocks, H-Front-Porch (HFP) ≧ 2 PCLK clocks

2. t_{VHS}≧400ns

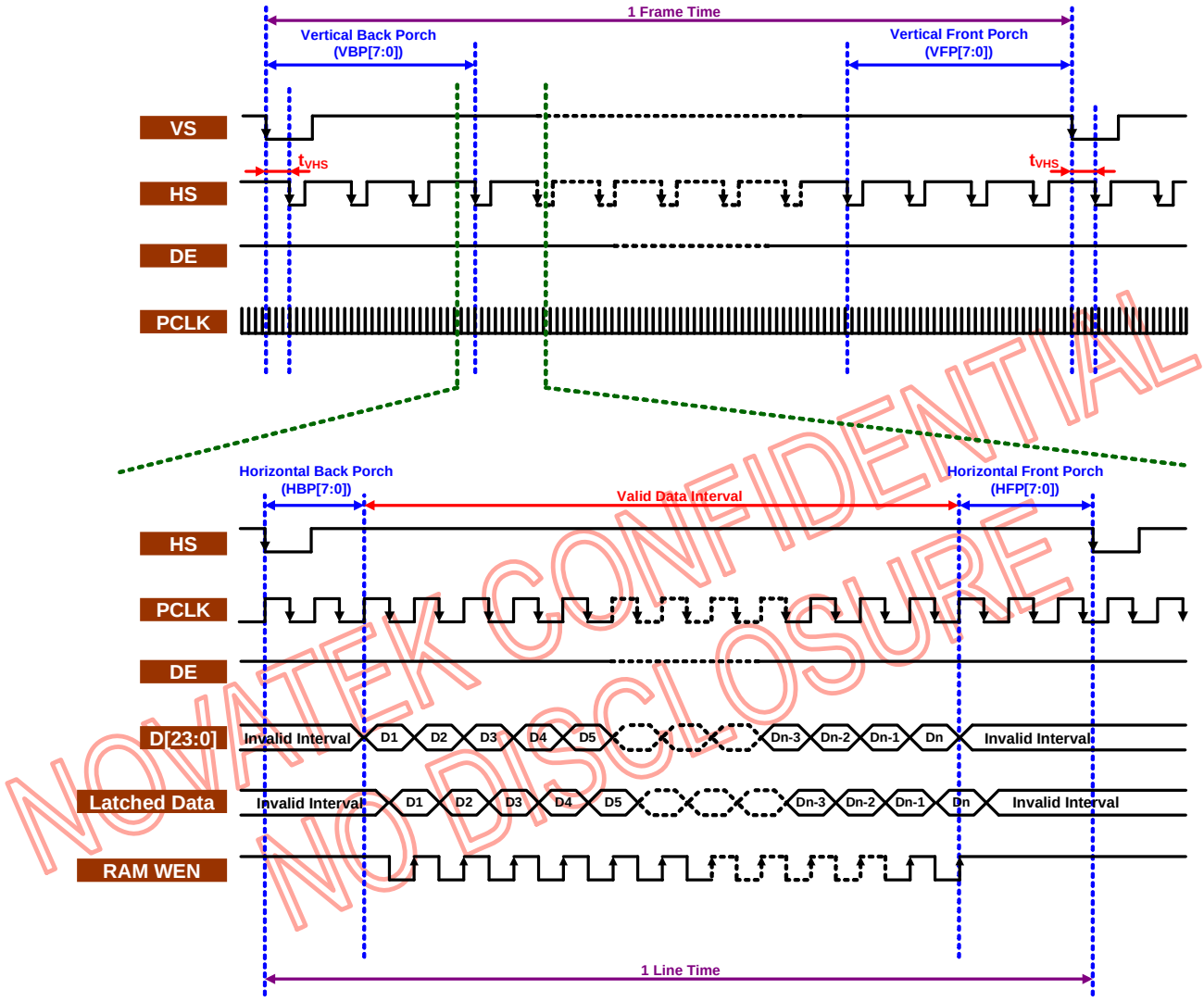


Fig. 5.8.3 Video signal data writing method in RGB Mode 2 Interface

Notes:

1. Constraint:

V-Back Porch (VBP[7:0]) ≧ 5 HS lines, V-Front Porch (VFP[7:0]) ≧ 2 HS lines

VBP[7:0]+VFP[7:0] (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch)

H-Back Porch (HBP[7:0]) ≧ 5 PCLK clocks, H-Back Porch (HFP[7:0]) ≧ 2 PCLK clocks

2. t_{VHS}≧400ns

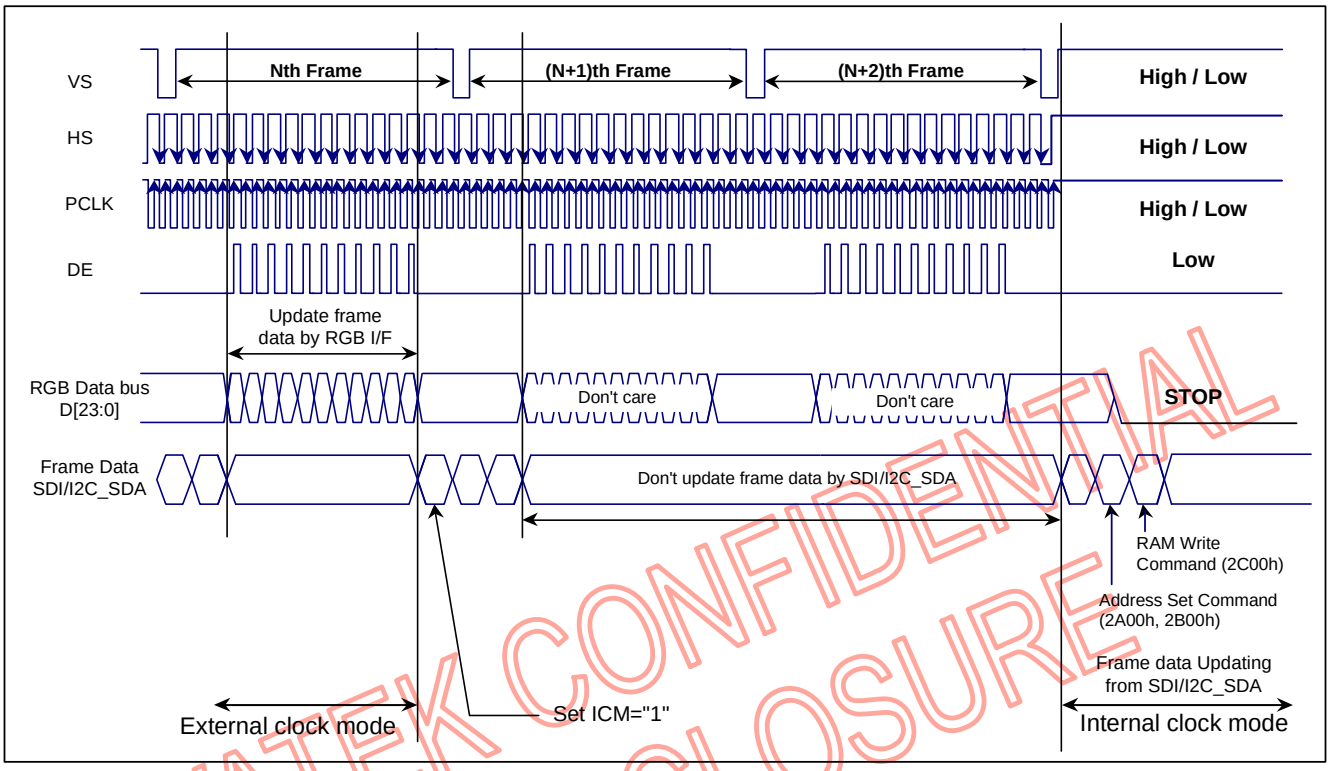


Fig. 5.8.4 RGB with SPI Timing Sequence (Enter Internal Clock Mode, ICM="1")

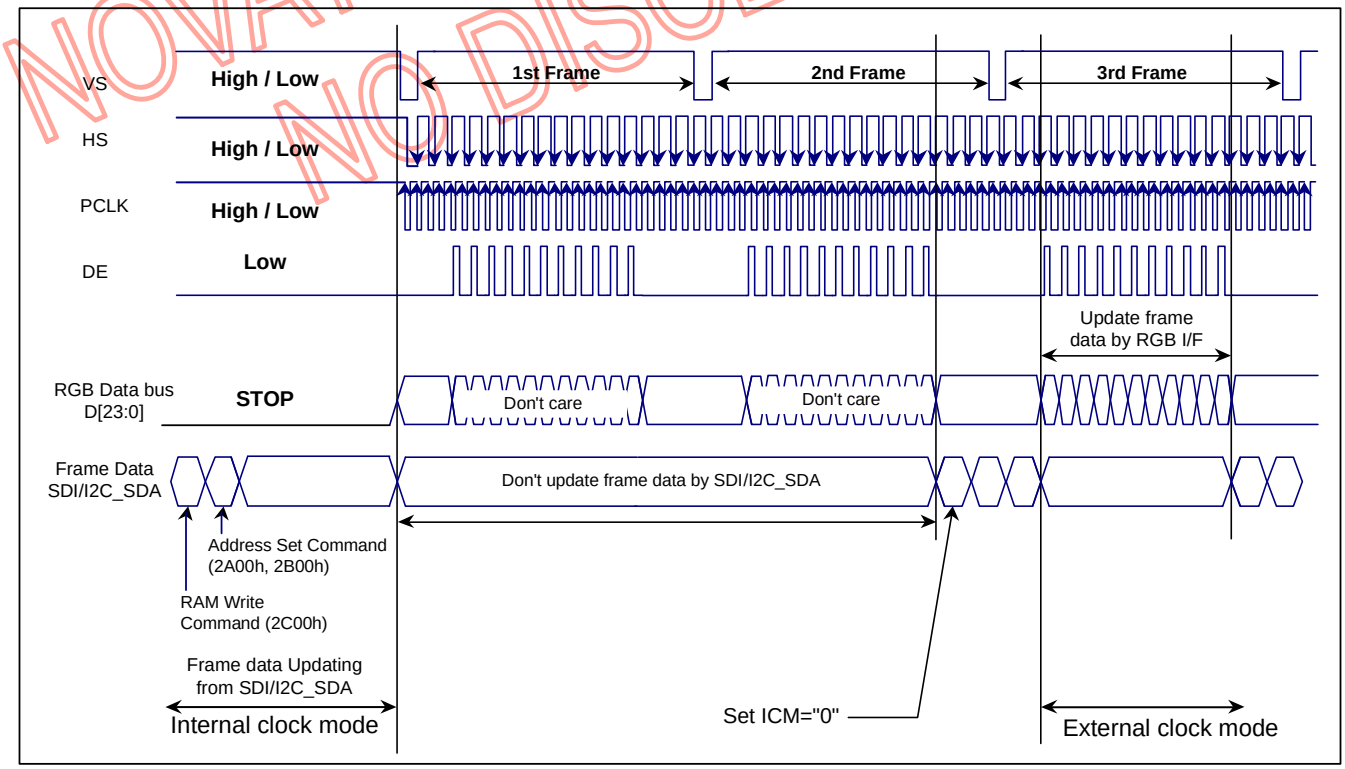


Fig. 5.8.5 RGB with SPI Timing Sequence (Exit Internal Clock Mode, ICM="0")

5.8.4 RGB Interface Bus Width Set

All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command (3A00h): VIPF[3:0]).

3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
50h	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	16-bit data
60h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	18-bit data
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit data

NOTES:

1. "x": Unused RGB data bus connected with VSSI.

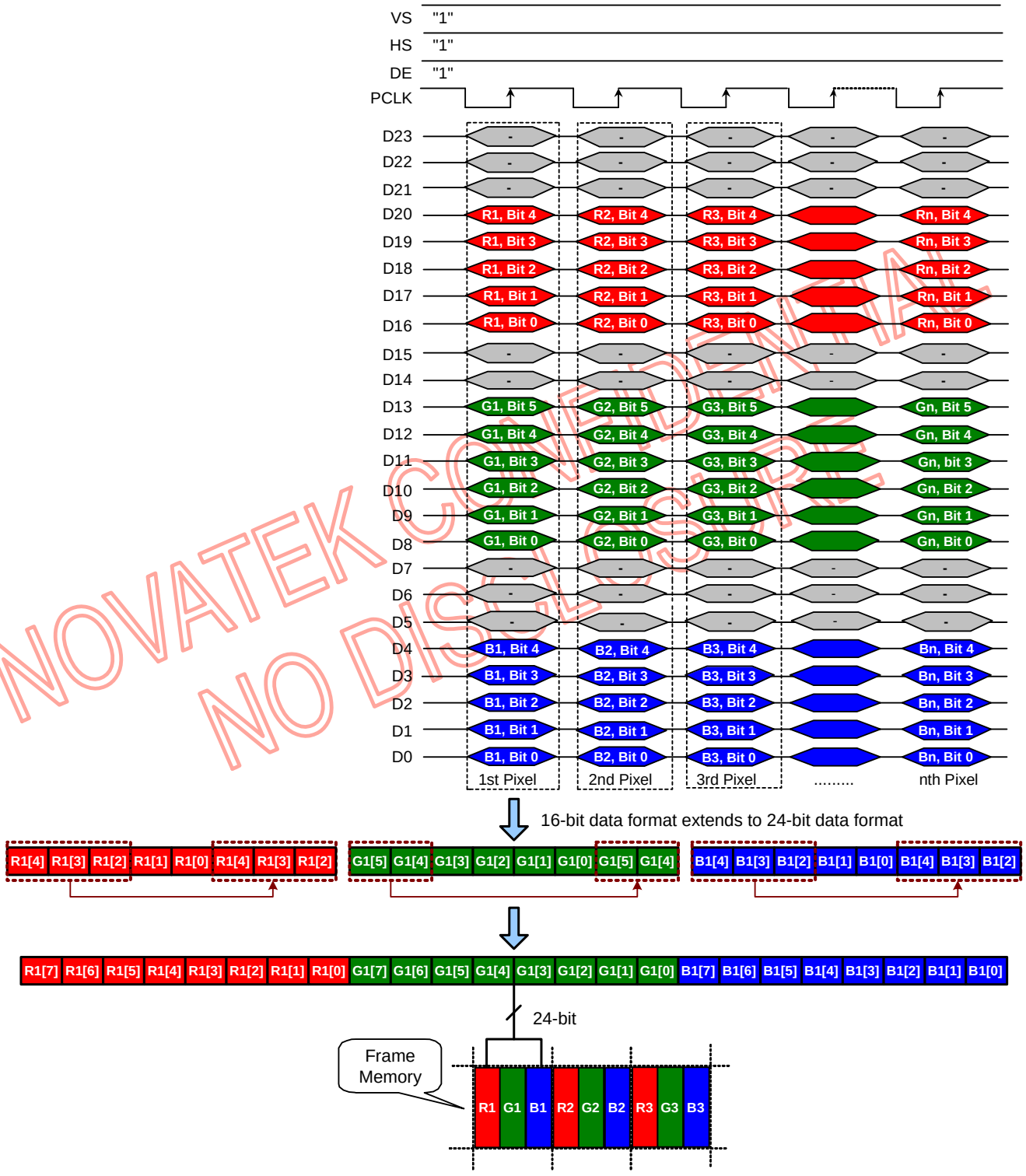
2. R0 is the LSB for the red component; G0 is the LSB for the green component, etc.

3. For 16-bit pixels, R primary color MSB is R4, G primary color MSB is G5 and B primary color MSB is B4.

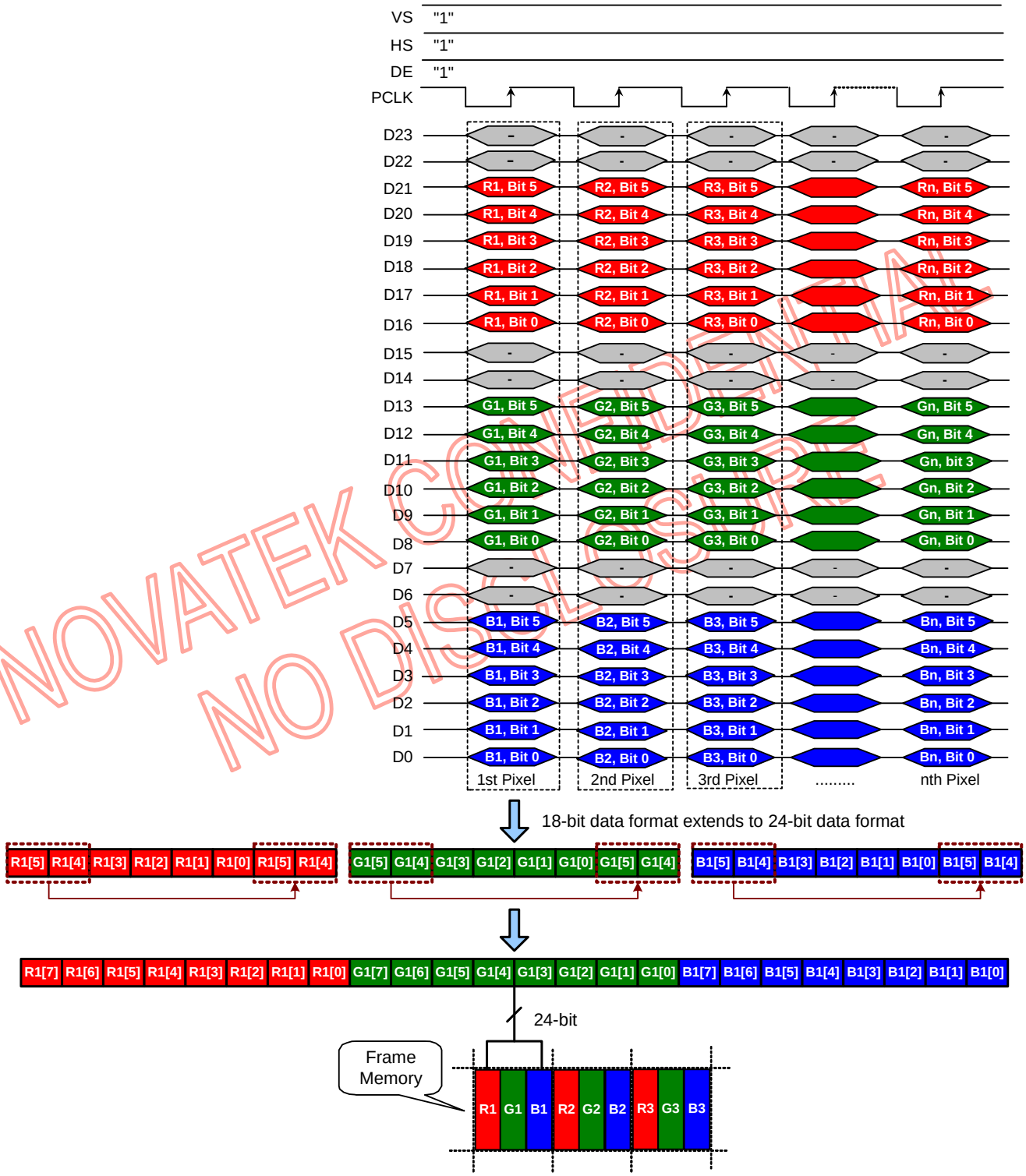
4. For 18-bit pixels, R primary color MSB is R5, G primary color MSB is G5 and B primary color MSB is B5.

5. For 24-bit pixels, R primary color MSB is R7, G primary color MSB is G7 and B primary color MSB is B7

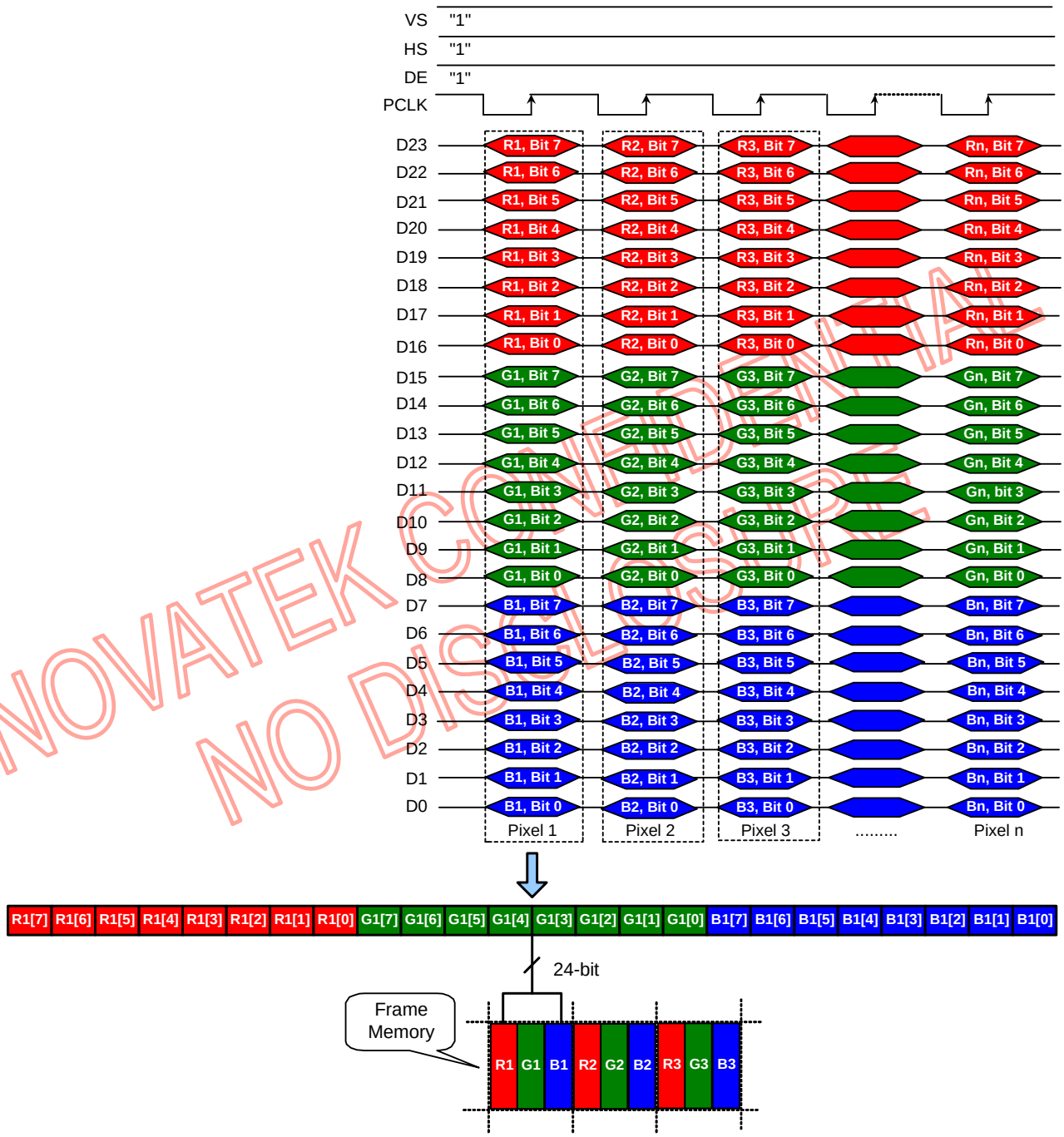
Write data for 16-bit RGB interface bus width set is shown below.



Write data for 18-bit RGB interface bus width set is shown below.



Write data for 24-bit RGB interface bus width set is shown below.

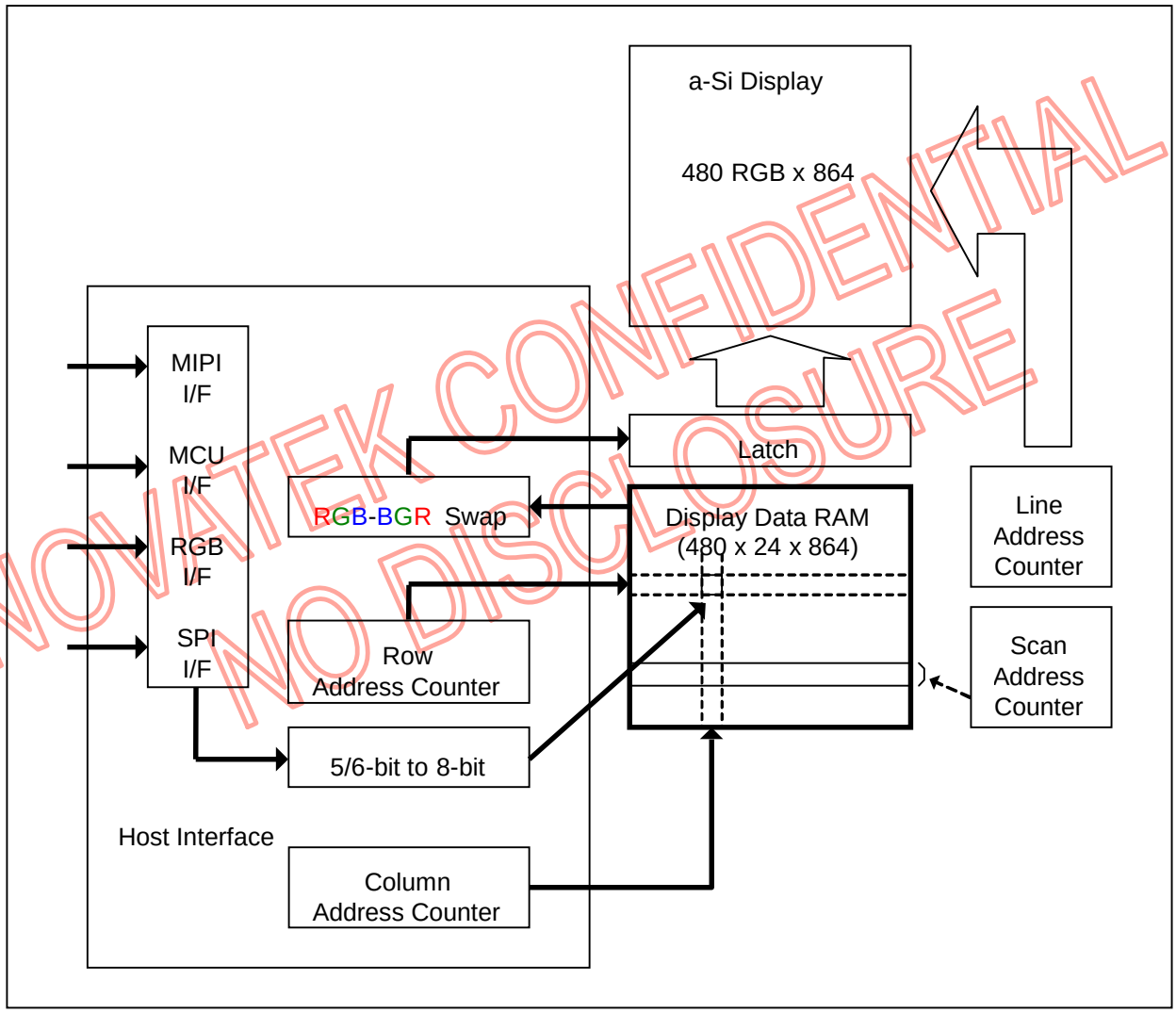


5.9 Frame Memory

5.9.1 Configuration

The NT35510 has an integrated 480 x 864 x 24-bit graphic type static RAM. This 9,953,280-bit memory allows to store on-chip a 480 x RGB x 864, 480 x RGB x 854, 480 x RGB x 800, 480 x RGB x 720 and 480 x RGB x 640 image with an 24-bit resolution (16.7M-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



5.9.2 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 1-1-1-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The address pointers address the locations of RAM.

When CGM[7:0]=”70h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=863 (35Fh).
When CGM[7:0]=”6Bh”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=853 (355h).
When CGM[7:0]=”50h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=799 (31Fh).
When CGM[7:0]=”28h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=719 (2CFh).
When CGM[7:0]=”00h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=639 (27Fh).

Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written when CGM[7:0]=”50h”, if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479 (1DFh), YE=799 (31Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.2 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

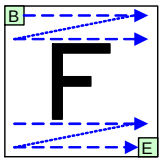
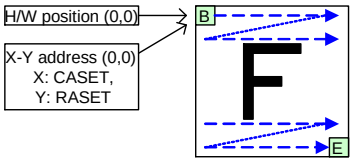
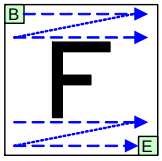
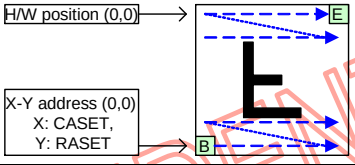
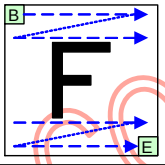
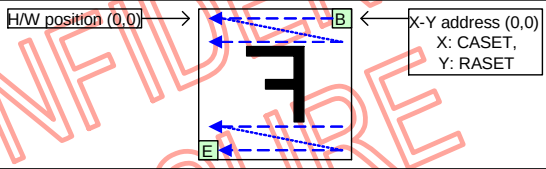
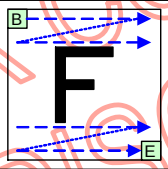
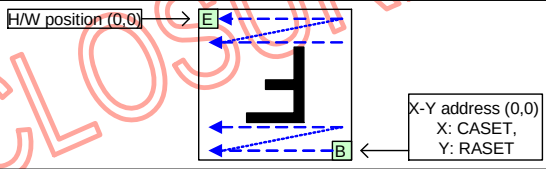
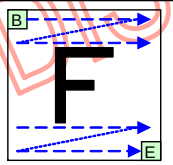
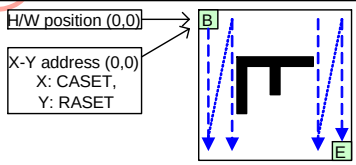
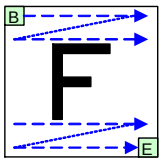
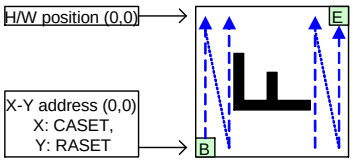
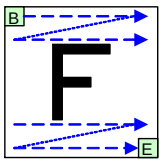
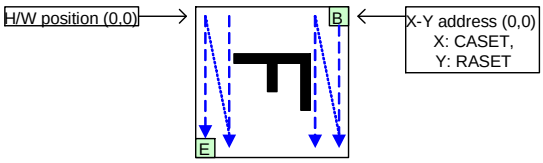
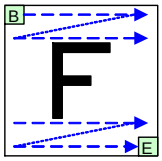
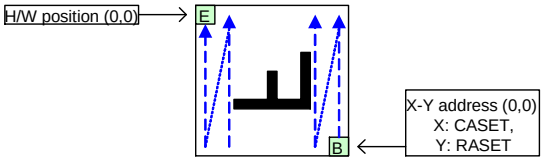
For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Pair Read / Write action	Twice Increment by 1 (First Pixel n then Pixel n+1)	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

NOTE:
Data is always written to the Frame Memory in the order, regardless of the Memory Write Direction set by command MADCTL (36h) bit MY, MX and MV. The write order for each pixel unit is (R, G, B) transferred from (D2, D1, D0) = (R, G, B). One pixel unit represents 1 column and 1 page counter value on the Frame Memory

5.9.3 Interface to Memory Write Direction

The resultant image for each orientation setting is illustrated below.

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.9.4 Frame Memory to Display Address Mapping

The frame memory to display address mapping for 480RGB x 864 resolution (RSMX=RSMY="0") is shown below figure. The maximum address of RA/SA/CA and used source outputs are decided by bit CGM[2:0] (see command 2Ah CASET, 2Bh PASET and section 8.2).

	Pixel 1			Pixel 2					---------			Pixel N-1			Pixel N			
Source Output	S1	S2	S3	S4	S5	S6	S7	S8	- - - -	S1433	S1434	S1435	S1436	S1437	S1438	S1439	S1440	**S1~S1440**
	R0	G0	B0	R1	G1	B1	R2	G2	- - - -	G477	B477	R478	G478	B478	R479	G479	B479	
RA (CA*)	RGB=0 : ⟶ RGB=1 : ⟶																	**SA**
MY=0	*MY=1*																	*ML=0*	*ML=1*
0	863								- - - -									0	863
1	862								- - - -									1	862
2	861								- - - -									2	861
3	860								- - - -									3	860
4	859								- - - -									4	859
5	858								- - - -									5	858
6	857								- - - -									6	857
7	856								- - - -									7	856
8	855								- - - -									8	855
9	854								- - - -									9	854
10	853								- - - -									10	853
11	852								- - - -									11	852
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	- - - -	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
856	7								- - - -									856	7
857	6								- - - -									857	6
858	5								- - - -									858	5
859	4								- - - -									859	4
860	3								- - - -									860	3
861	2								- - - -									861	2
862	1								- - - -									862	1
863	0								- - - -									863	0
CA (RA*)	*MX=0*	0		1			- - - -					478			479				
	MX=1	479		478			- - - -					1			0				

RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
PTD = Source output voltage selection for 1-bit data "0" and "1", parameter of PWCTR5 command
** RA and CA is exchange when MV = "1"*

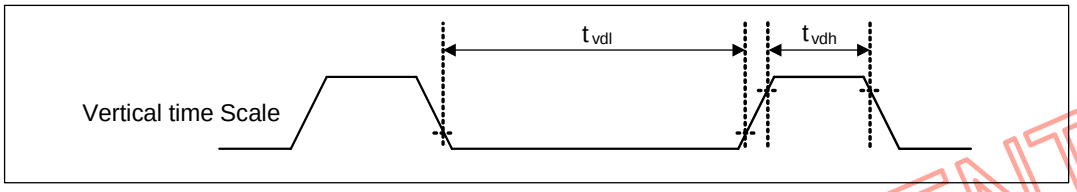
5.10 Tearing Effect Information

5.10.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

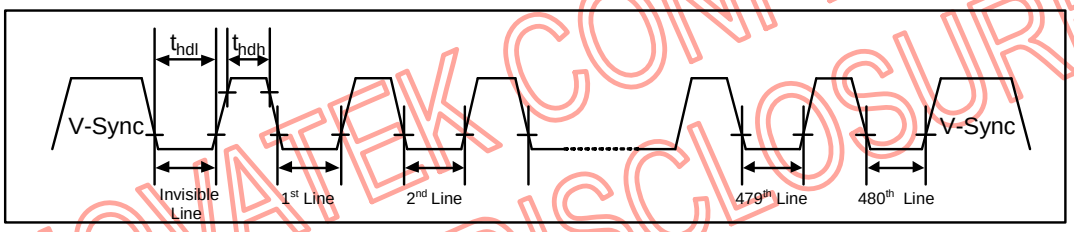
5.10.1.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



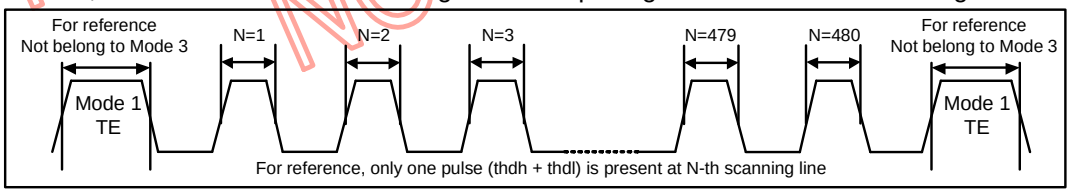
tvdh = The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



thdh = The LCD display is not updated from the Frame Memory
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

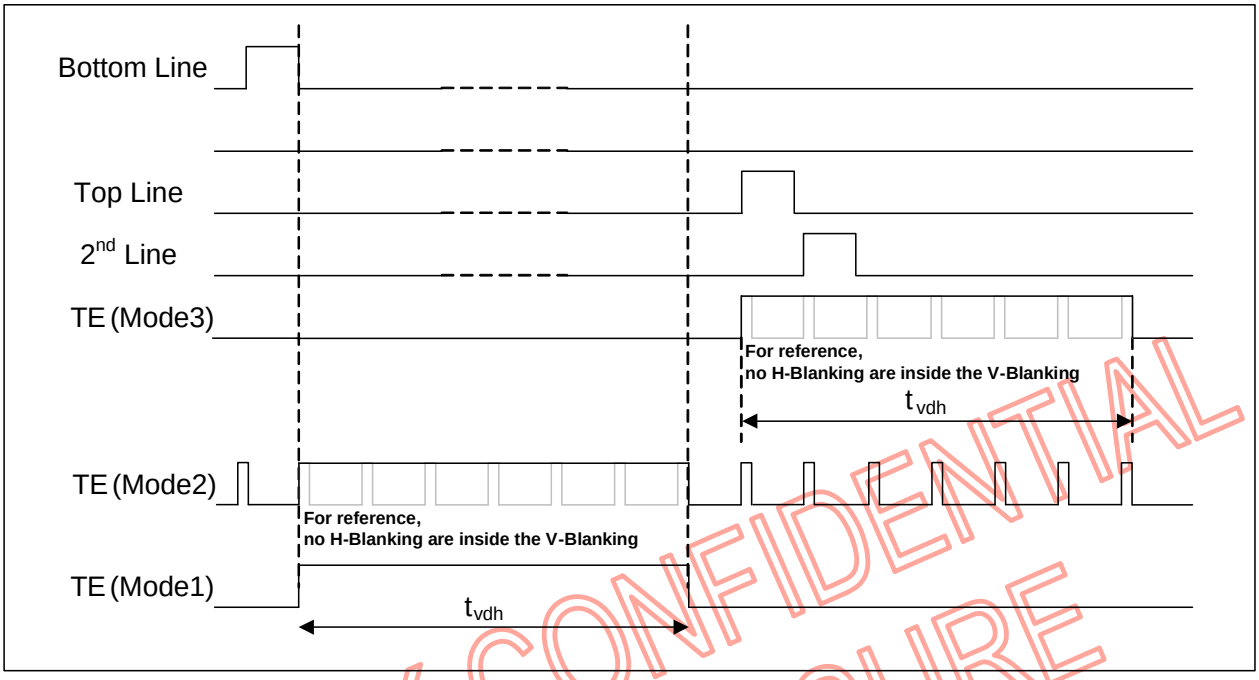
Mode 3, this mode turn on the Tearing Effect Output signal when vertical scanning reaches line N.



N = The N-th scanning line which set by register N[15:0] of command STESL (44h)

The TE mode selection is described as below table

DOPCTR (B100h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	M	N[15:0]	
0	X	X	TE off (output low)
1	34h	X	TE off (output low)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line (Mode 3)
1	35h with M=1	X	TE high in all V-porch and H-porch region (Mode 2)



NOTE: During Sleep In Mode, the Tearing Output Pin is active Low

5.10.1.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:

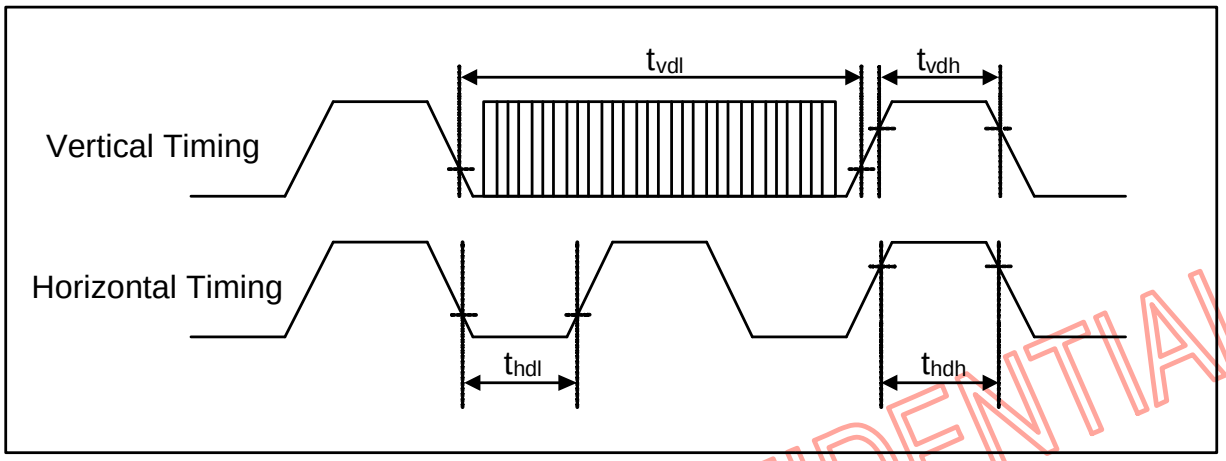


Table 5.10.1 AC characteristics of Tearing Effect Signal

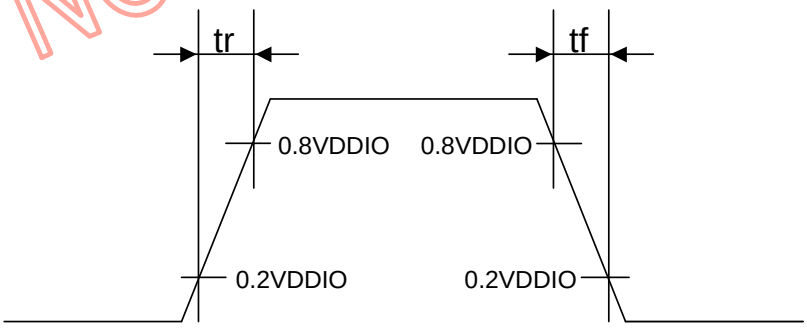
Symbol	Parameter	min	max	unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	TBD	-	µs	
thdh	Horizontal Timing High Duration	TBD	500	µs	

Notes:

1. The timings in above table apply when MADCTL ML=0 and ML=1.

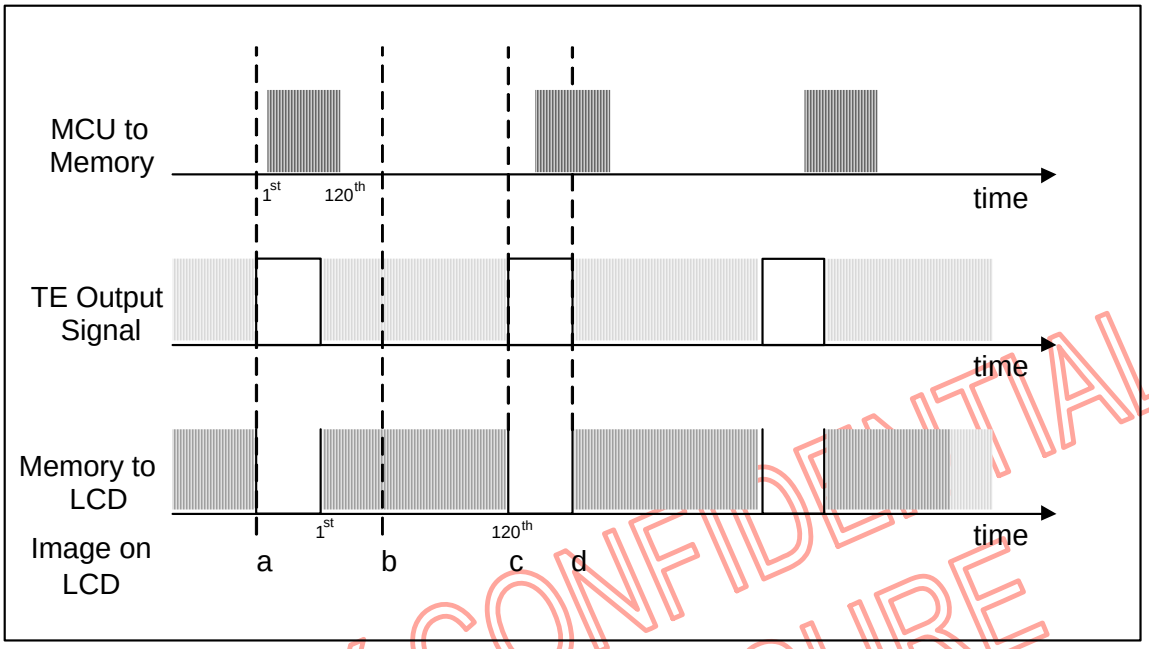
2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω.

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

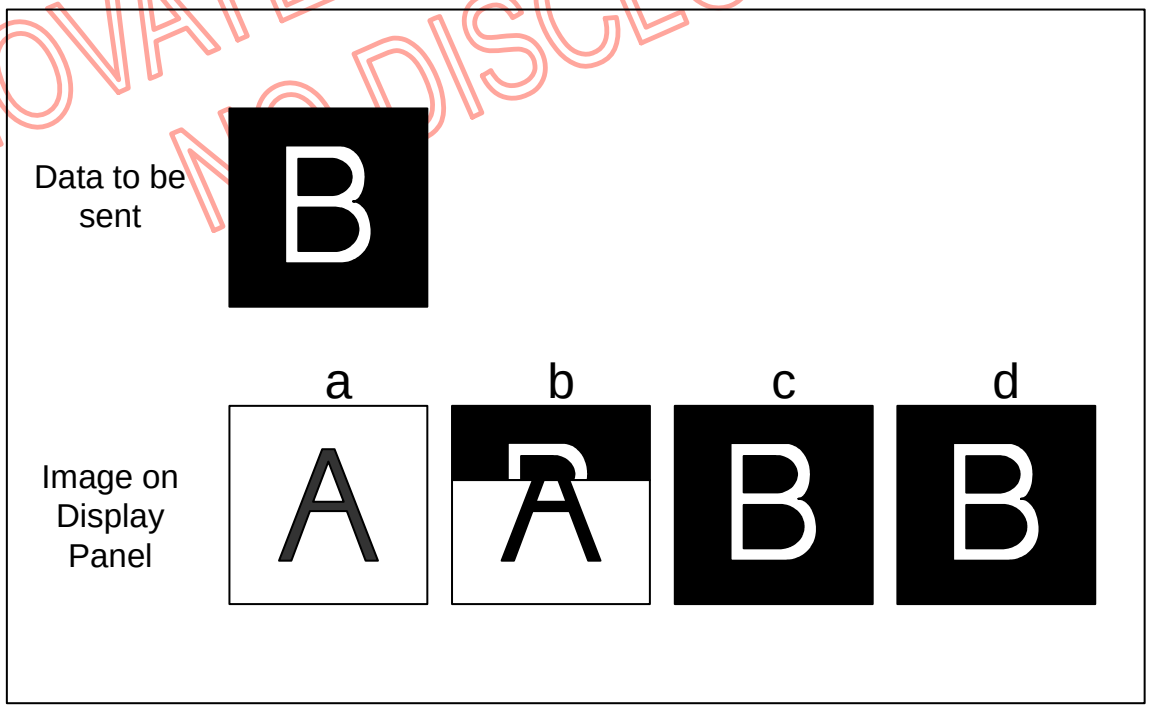


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

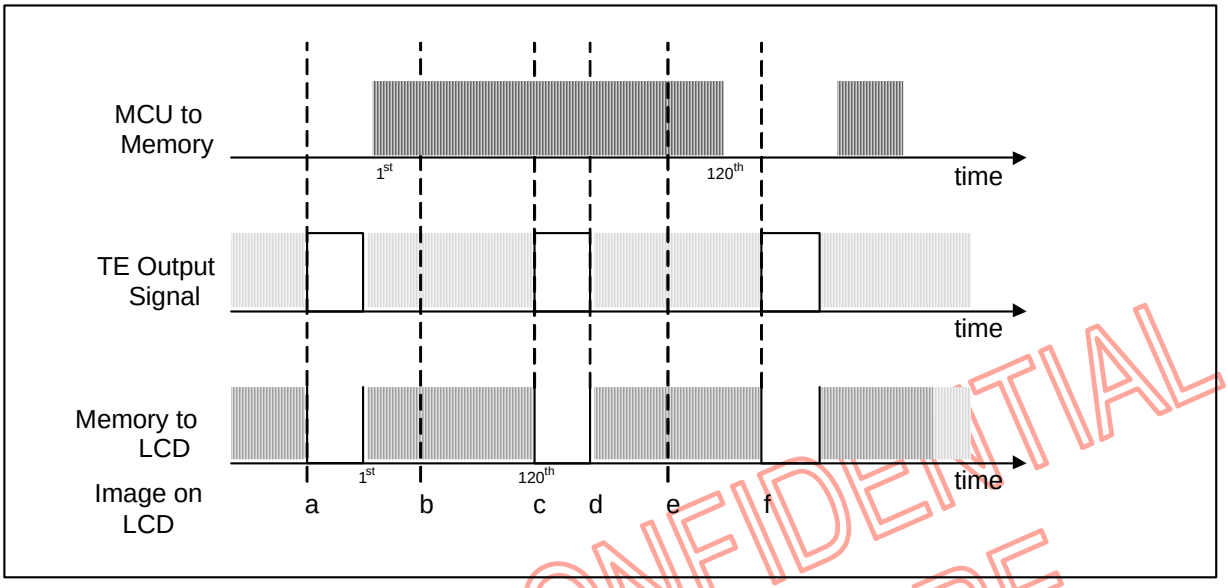
5.10.1.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.



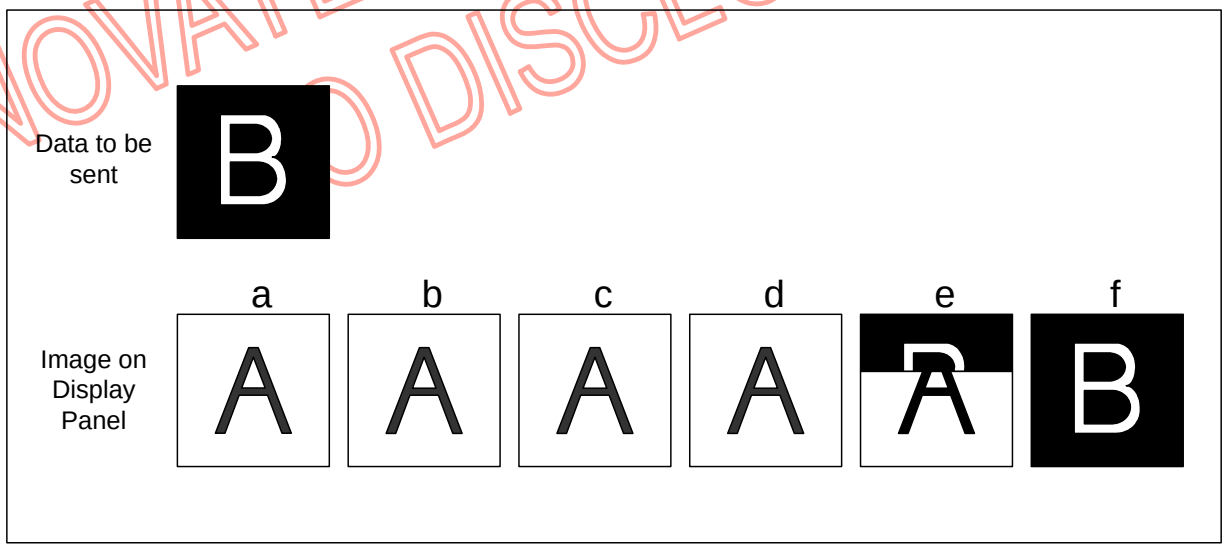
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.10.1.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.

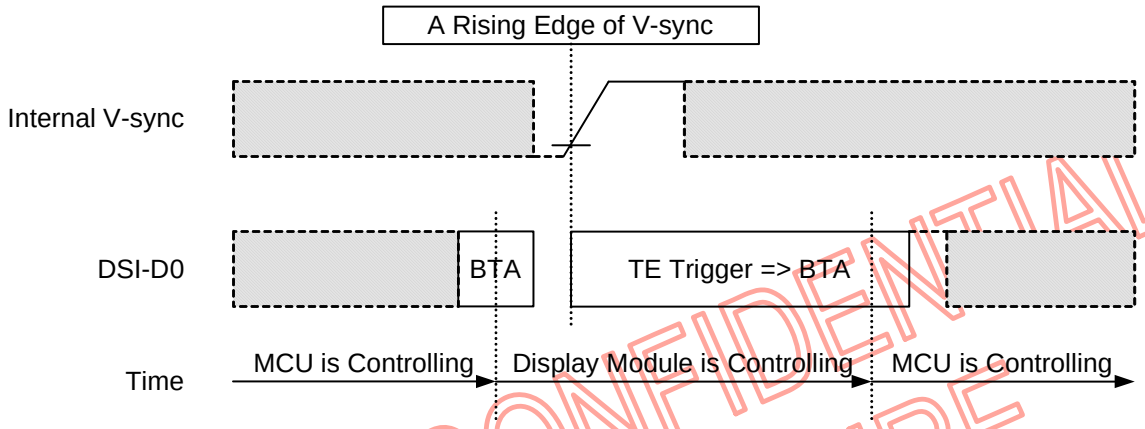


The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



5.10.2 Tearing Effect Bus Trigger

A Tearing Effect Bus Trigger information supplies to the MCU a Panel synchronization trigger and this Tearing Effect Bus Trigger information can be enabled or disabled by “Tearing Effect Line On (35h)” and “Tearing Effect Line Off (34h)” commands when the only mode of the Tearing Effect Signal is V-Sync information.
The driver IC is sending this trigger information in Escape Mode after the Bus Turnaround (BTA). and at a rising edge of the internal V-sync (A start of the new image frame). See section “Tearing Effect (TEE)”

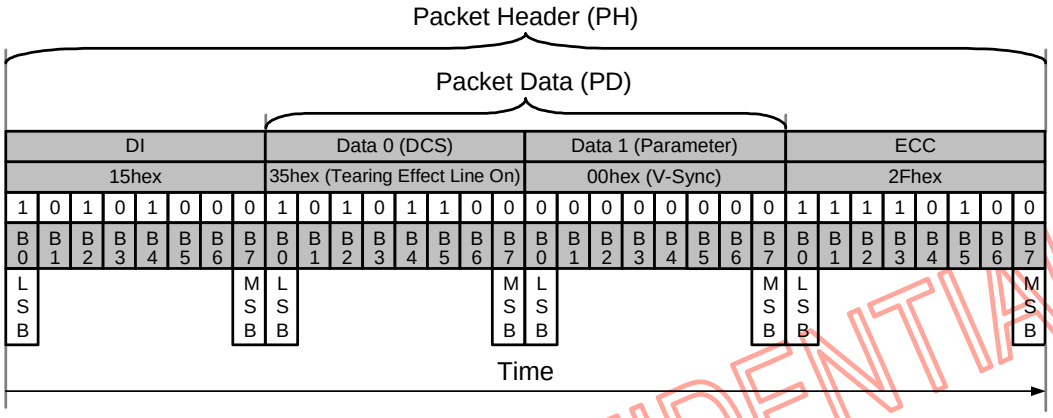


A Rising Edge of the V-sync and DSI-D0

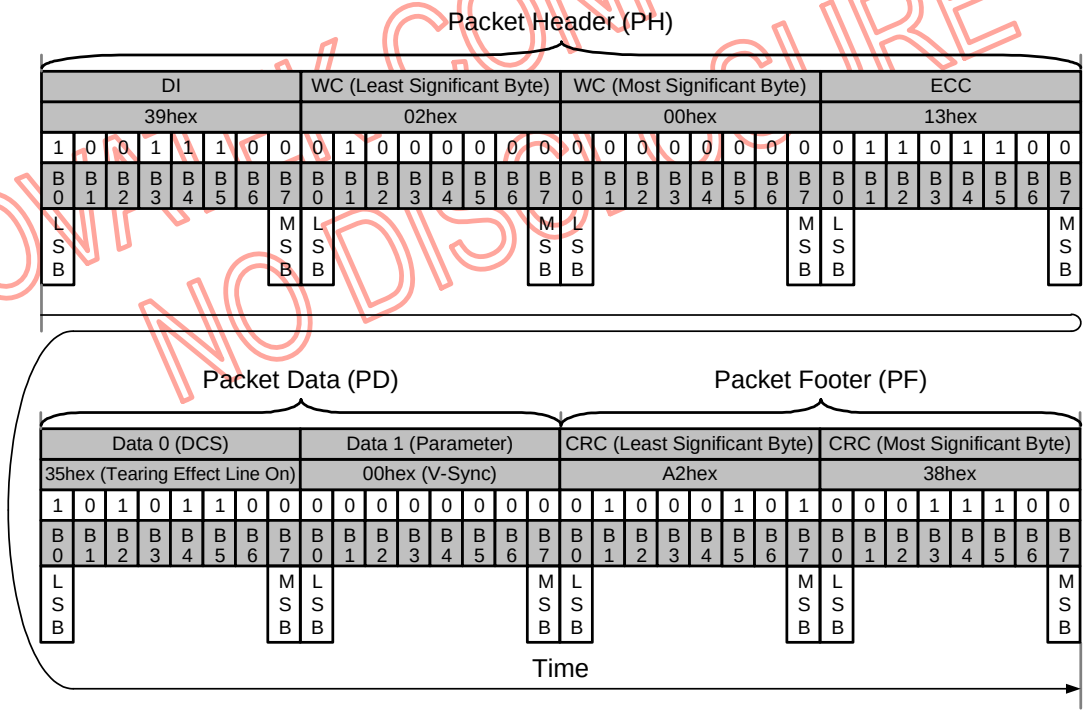
The Tearing Effect Bus Trigger can use in both DSI case with or without the TE line when the driver IC is sending the TE trigger if it received a correct tearing effect trigger request as this is described on section “5.10.2.3 Tearing Effect Bus Trigger Sequence”.

5.10.2.1 TEARING EFFECT BUS TRIGGER ENABLE

The MCU can enable the Tearing Effect Bus Trigger on the driver IC in 2 different ways when Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.:



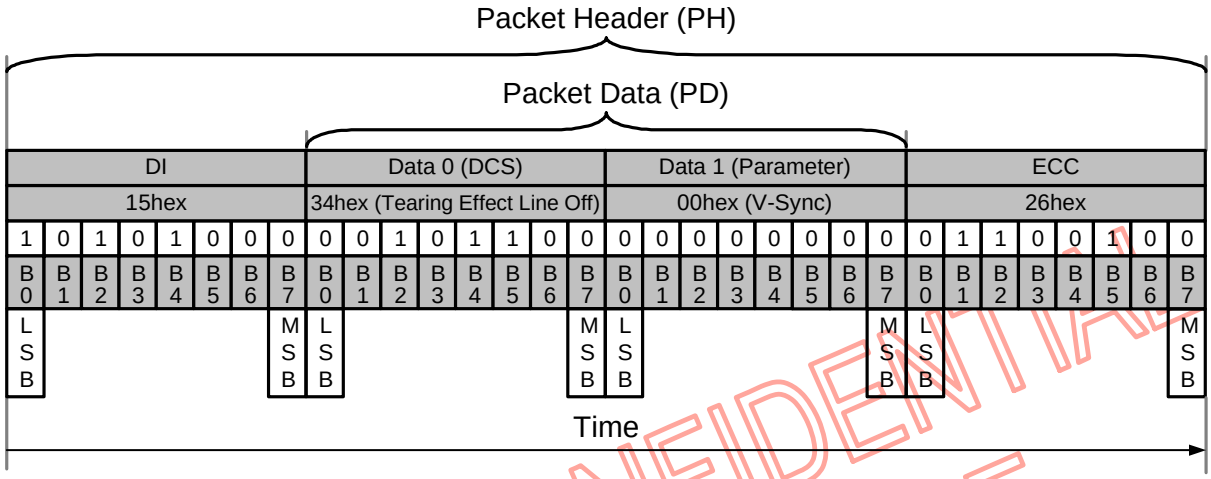
Tearing Effect Bus Trigger Enable (DCSW1-S) Short Packet (SPa)



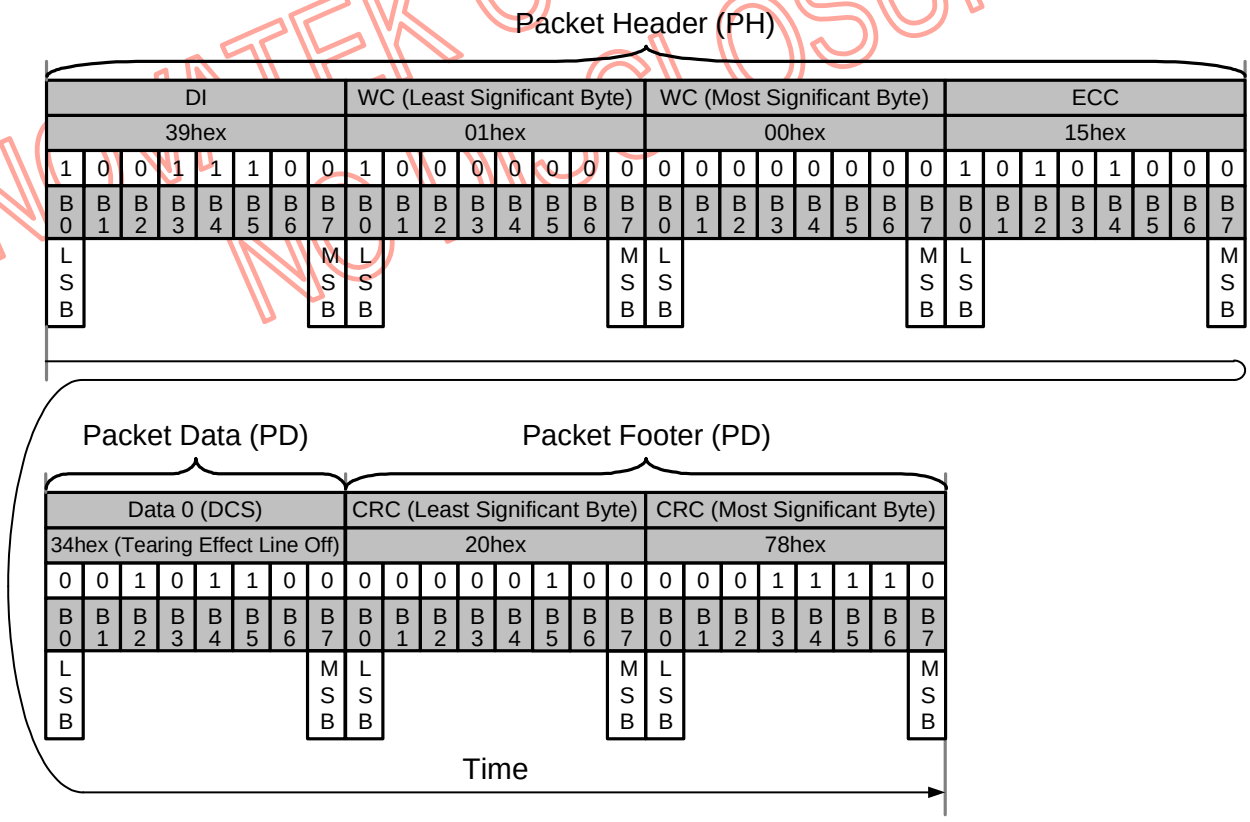
Tearing Effect Bus Trigger Enable (DCSW-L) Long Packet (LPa)

5.10.2.2 TEARING EFFECT BUS TRIGGER DISABLE

The MCU can disable the Tearing Effect Bus Trigger on the driver IC in 2 different ways when Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.:



Tearing Effect Bus Trigger Disable (DCSW1-S) Short Packet (SPa)



Tearing Effect Bus Trigger Disable (DCSW-L) Long Packet (LPa)

5.10.2.3 TEARING EFFECT BUS TRIGGER SEQUENCES

Tearing Effect Bus Trigger Enable Sequence – DCSW-L and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error is corrected by ECC => goto line 19 If error => goto line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
13	-	-	<=	LP-11	-	
14	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
24	-	-	<=	LP-11	-	
25	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
26	-	-	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
28	-	LP-11	=>	-	-	End

29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 34 If the MCU is forcing BTA => goto line 35
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information)
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 17 are needed for every frame.

2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW-L and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error is corrected by ECC => goto line 18 If error => goto line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
27	-	LP-11	=>	-	-	End

28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 33 If the MCU is forcing BTA => goto line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information)
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 16 are needed for every frame.

2. Bit 5 and Bit7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error is corrected by ECC => goto line 19 If error => goto line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
13	-	-	<=	LP-11	-	
14	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
24	-	-	<=	LP-11	-	
25	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
26	-	-	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
28	-	LP-11	=>	-	-	End

29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 34 If the MCU is forcing BTA => goto line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information)
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 17 are needed for every frame.

2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Enable Sequence – DCSW1-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error is corrected by ECC => goto line 18 If error => goto line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Sync
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
27	-	LP-11	=>	-	-	End

28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => goto line 33 If the MCU is forcing BTA => goto line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information)
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported)
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 ~ 16 are needed for every frame.

2. Bit 5 and Bit 7 of the AwER are applied.

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	=>	-	-	

Tearing Effect Bus Trigger Disable Sequence – DCSWN-S and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	

5.11 Checksum

The display module consists of two 8-bit checksum registers, which are used checksum calculations for “User Command Set” area registers (includes the frame memory), on the display module.

One of the checksum registers is “First Checksum” (FCS) and another is “Continue Checksum” (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on “User Command Set” area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on “User Command Set” area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on “User Command Set” area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on “User Command Set” area registers.

There is always updated a checksum comparison bit (See section: “Read Display Self-Diagnostic Result (0Fh)” and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

User can read FCS, CCS and Comparison bit D0 values. See section: “Read First Checksum (AAh)”, “Read Continue Checksum (AFh)” and ”Read Display Self-Diagnostic Result (0Fh)”.

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:
- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in “Sleep Out” mode and it is stopped in “Sleep In” mode.

Table 5.11.1 Checksum Sequence

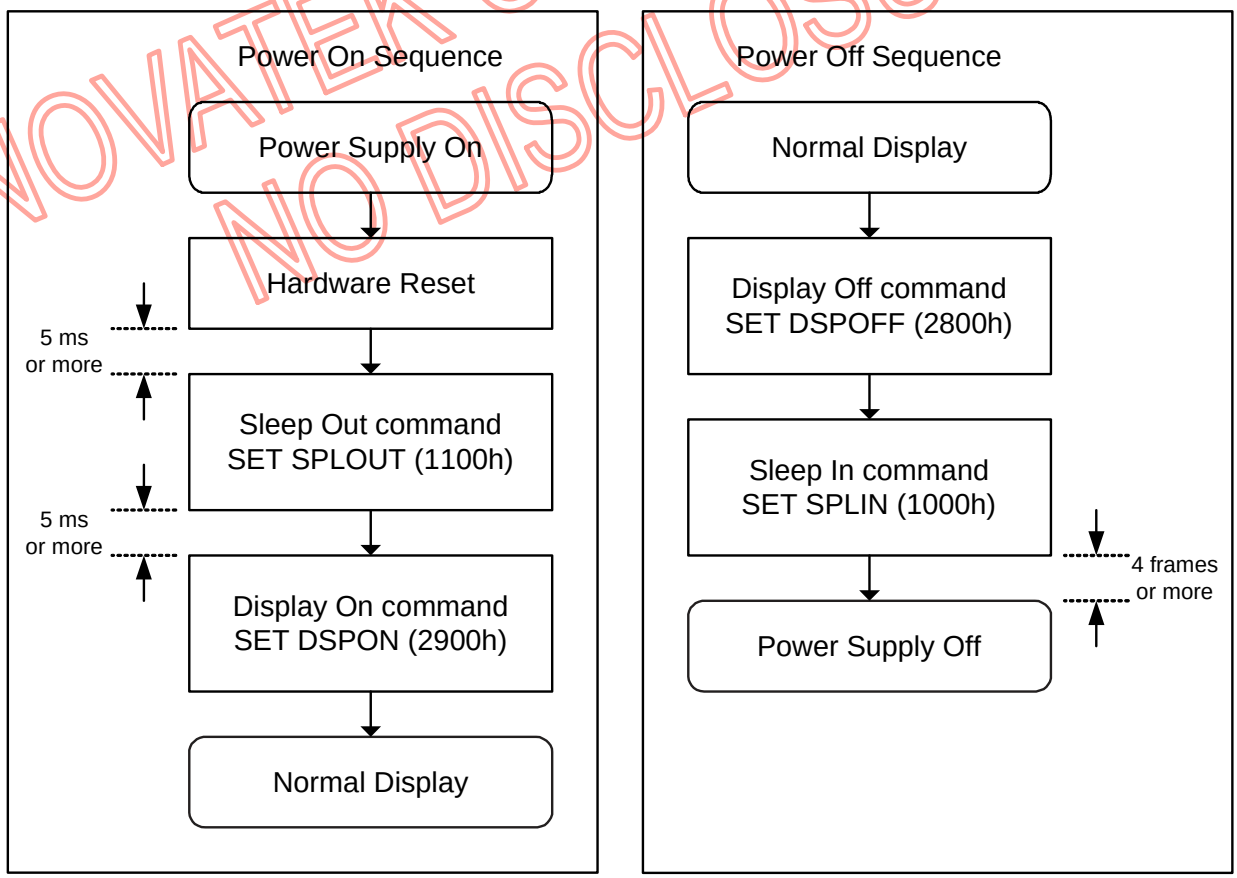
Step Note1	Time Note2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on “User Command Set” area registers => FCS an CCS registers are initialized
2	0 | 150ms	Continue sum of “User Command Set” area registers	Counting	-	-	The first register counting is running
3	150ms	Stores sum of registers on FCS register	Set to 00h after value is moved to FCS register	Stores sum of “User Command Set” area registers on FCS register	-	The result of the first register counting is stored on FCS register. The result of the FCS is available to the MPU
4	150ms | 300ms	Continue sum of “User Command Set” area registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
6	300ms | 450ms	Continue sum of “User Command Set” area registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
8	450 | 600ms	Continue sum of “User Command Set” area registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
10	etc	-	-	-	-	Same sequence continue e.g. step 4 and 5

5.12 Power On/Off Sequence

VDDI and VDD (VDDA) can be applied in any order.
VDD (VDDA) and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD (VDDA) and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA) can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.
Notes:

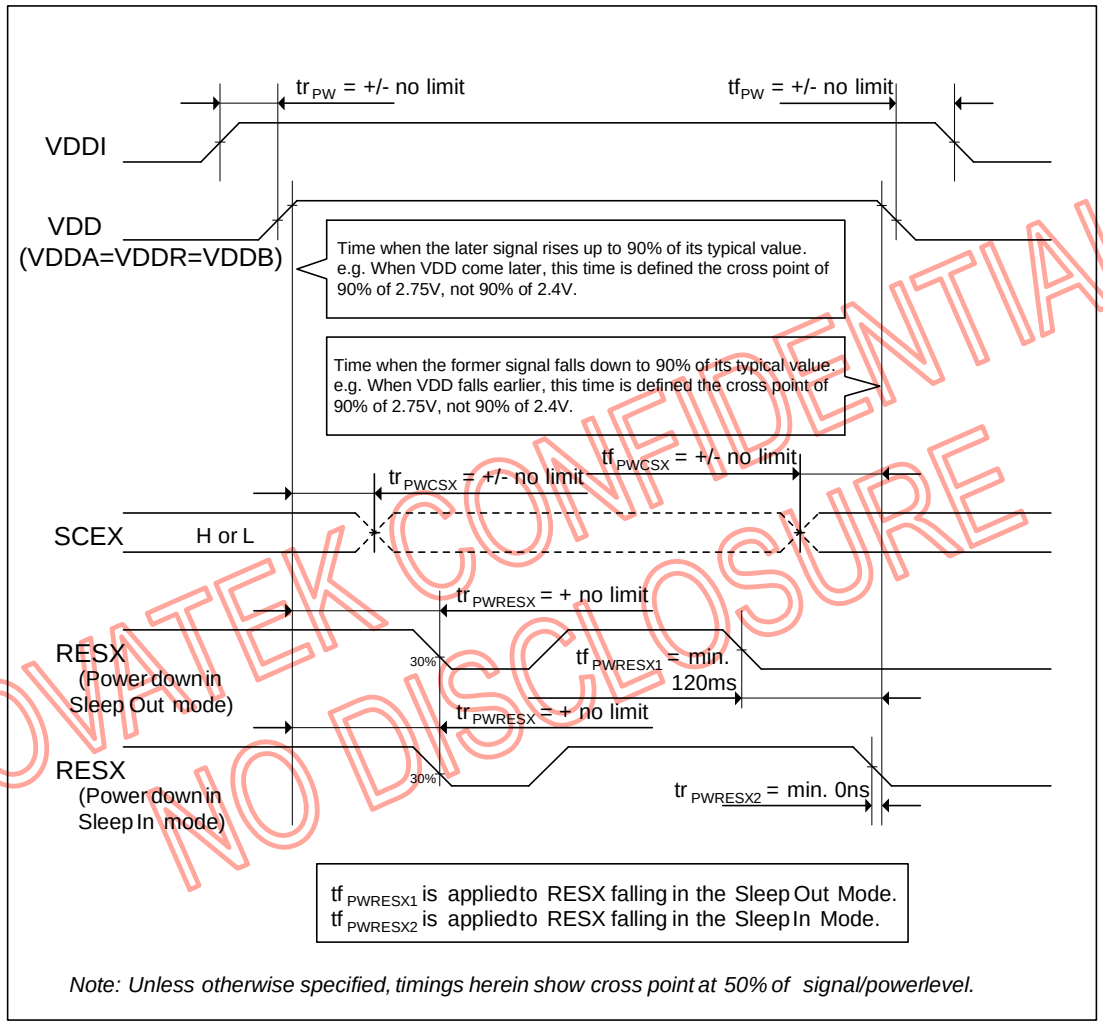
1. *There will be no damage to the display module if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.12.1 and 5.12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *There is not a limit for Rise/Fall time on VDDI and VDD (VDDA).*
6. *The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).*

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



5.12.1 Case 1 – RESX line is held High or Unstable by Host at Power On

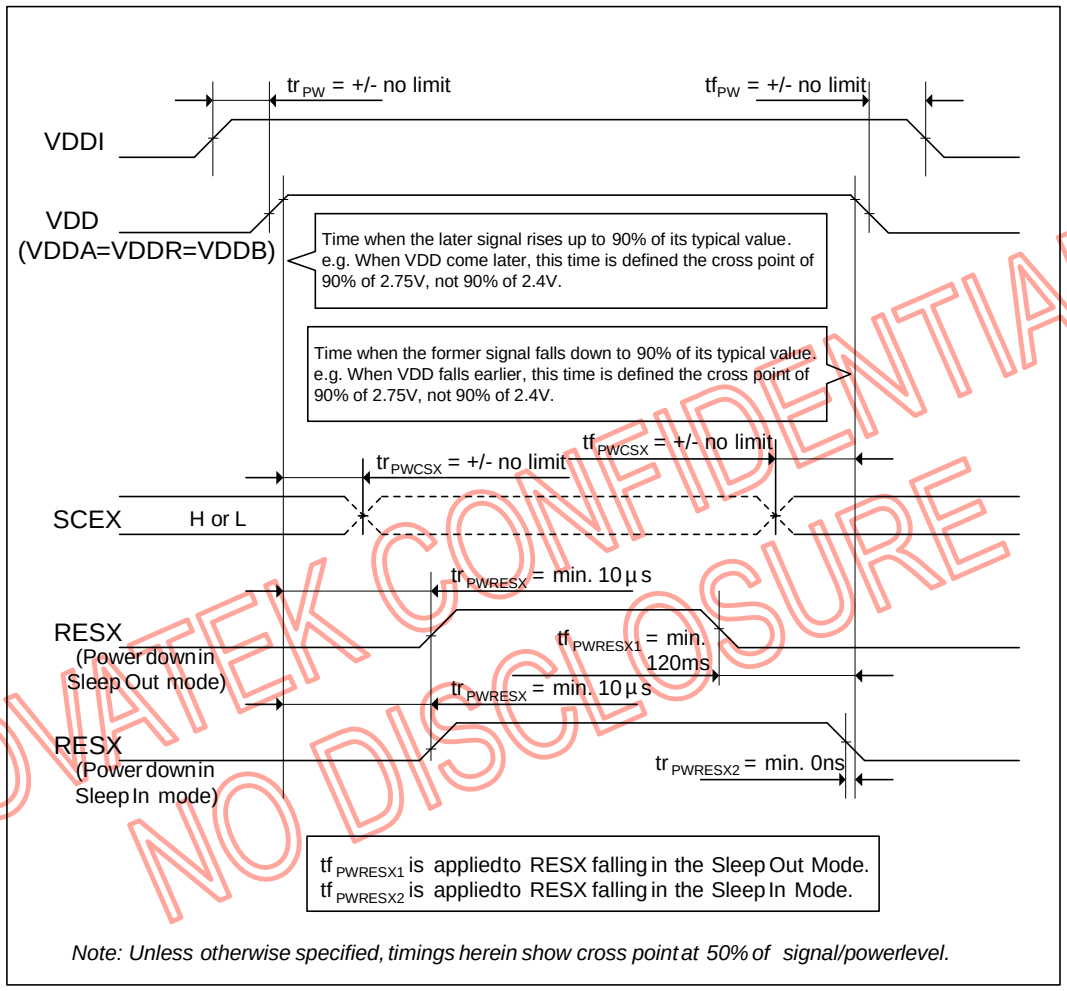
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/powerlevel.

5.12.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/powerlevel.

5.12.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.13 Power Level Modes

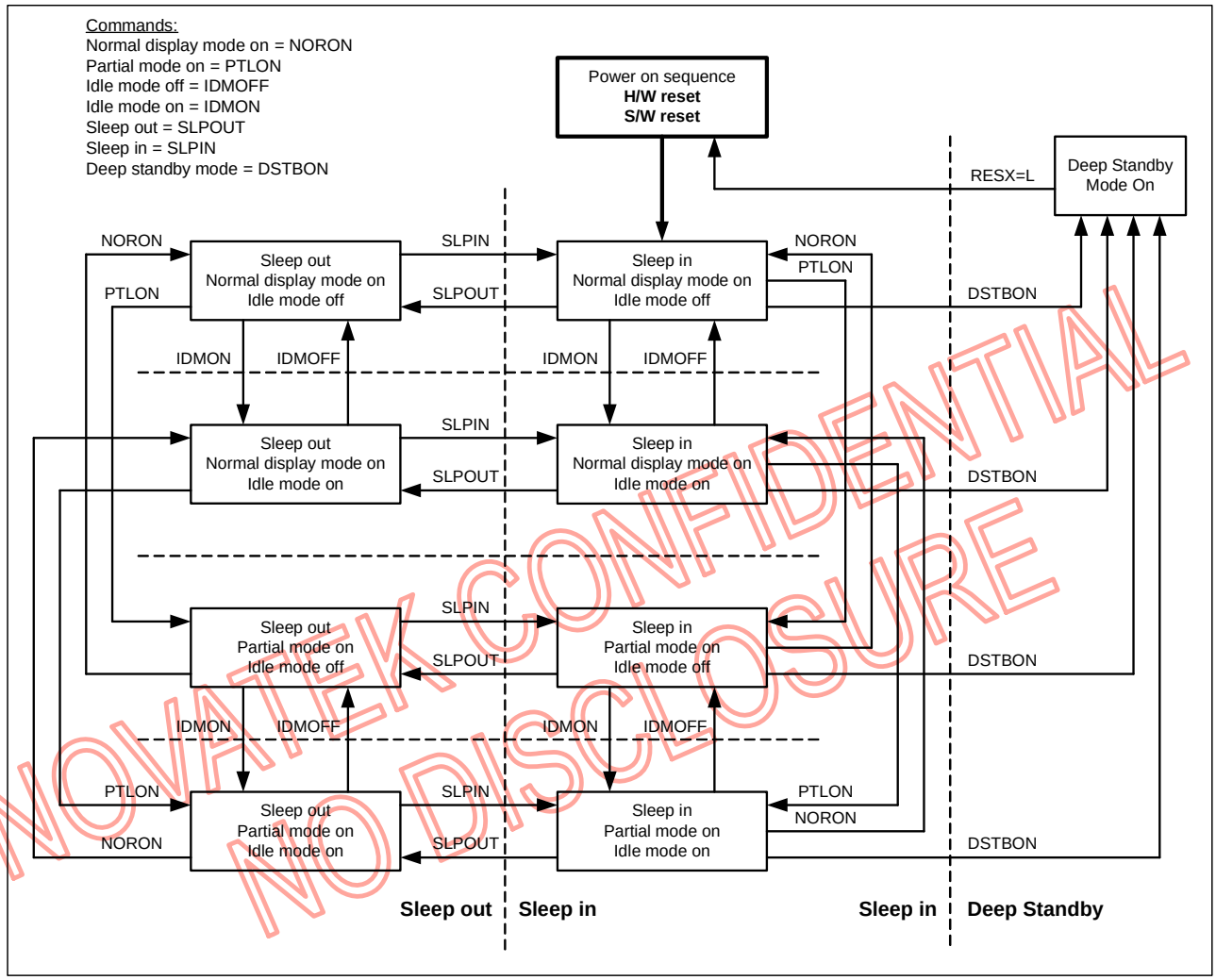
5.13.1 Definition

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.
6. Deep Standby Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory is random.
7. Power Off Mode
   In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

5.13.2 Power Level Mode Flow Chart



NOTES:

1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

The following table represents the SRAM and Registers its mode state.

Mode	SRAM	Register	Control	
			Enter	Exit
Sleep in mode 1 (RAMKP = 1)	Keep	Keep	Command	
Sleep in mode 2 (RAMKP = 0)	Loss	Keep	Command	
Deep-standby mode	Loss	Loss	Command	Reset pin
Reset=L	Loss	Keep (Default Value)	Reset (H/W)	

5.14 Reset function

5.14.1 Register Default Value

Table 5.14.1 Default Values for User Command Set

Item		After Power On	After Hardware Reset	After Software Reset
RDNUMPE (05h)		00h	00h	00h
RDDPM (0Ah)		08h	08h	08h
RDDMADCTR (0Bh)		00h	00h	00h
RDDCOLMOD (0Ch)		07h	07h	07h
RDDIM (0Dh)		00h	00h	00h
RDDSM (0Eh)		00h	00h	00h
RDDSDR (0Fh)		00h	00h	00h
Sleep In/Out (10h/11h)		In	In	In
Partial/Normal Display (12h/13h)		Normal	Normal	Normal
Display Inversion On/Off (21h/20h)		Off	Off	Off
All Pixel On/Off (23h/22h)		Off	Off	Off
Gamma setting (26h)		01h (GC0)	01h (GC0)	01h (GC0)
Display On/Off (29h/28h)		Off	Off	Off
Column: Start Address (XS, 2Ah)		0000h	0000h	0000h
Column: End Address (XE, 2Ah)	CGM[7:0]="70h" (480x864)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]="6Bh" (480x854)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]="50h" (480x800)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]="28h" (480x720)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]="00h" (480x640)	01DFh (479d)	01DFh (479d)	01DFh (479d)
Row: Start Address (YS, 2Bh)		0000h	0000h	0000h
Row: End Address (YE, 2Bh)	CGM[7:0]="70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)
	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)
	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)
	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)
Frame memory (2Ch, 2Eh, 3Ch, 3Eh)		Random	Random	Random
Partial: Start Address (PSL, 30h)		0000h	0000h	0000h
Partial: End Address (PEL, 30h)	CGM[7:0]="70h" (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)
	CGM[7:0]="6Bh" (480x854)	0355h (853d)	0355h (853d)	0355h (853d)
	CGM[7:0]="50h" (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)
	CGM[7:0]="28h" (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)
	CGM[7:0]="00h" (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)
Tearing: On/Off (35h/34h)		Off	Off	Off

Table 5.14.1 Default Values for User Command Set (Continuous)

Item		After Power On	After Hardware Reset	After Software Reset
Memory Data Access Control (36h) (MY/MX/MV/ML/RGB/MH/RSMX/RSMY)		00h	00h	00h
Idle Mode On/Off (38h/39h)		Off	Off	Off
Interface Pixel Color Format (3Ah)		77h	77h	77h
Set Tearing Effect Scan Line (44h)		0000h	0000h	0000h
Get Scan Line (45h)		N/A	N/A	N/A
DSTB mode (4Fh)		00h	00h	00h
Profile Value for Display (50h)		All values are FFh	All values are FFh	All values are FFh
Display Brightness (51h, 52h)		00h	00h	00h
CTRL Display (53h, 54h)		00h	00h	00h
CABC Control (55h, 56h)		00h	00h	00h
Write Hysteresis (57h)		All values are FFh	All values are FFh	All values are FFh
Write Gamma Setting (58h)		All values are 11h	All values are 11h	All values are 11h
RDFSVM (5Ah)		00h	00h	00h
RDFSVL (5Bh)		00h	00h	00h
RDMFFSVM (5Ch)		00h	00h	00h
RDMFFSVL (5Dh)		00h	00h	00h
RDLSCCM (65h, 66h)		80h	80h	80h
RDLSCCL (65h, 67h)		00h	00h	00h
Black/White Color Characteristics (70h~74h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
Red/Green Color Characteristics (75h~79h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
Blue/AColor Color Characteristics (7Ah~7Eh)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
DDB Start/Continue (A1h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
DDB Continue (A8h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
First/Continue Checksum (AAh, AFh)		00h	00h	00h
ID1 (DAh) ID2 (DBh) ID3 (DCh)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	ID1 = ”00h” ID2 = “80h” ID3 = “00h”	ID1 = ”00h” ID2 = “80h” ID3 = “00h”	ID1 = ”00h” ID2 = “80h” ID3 = “00h”

5.14.2 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins		After Power On	After Hardware Reset	After Software Reset
HSSI_DATA0_P, HSSI_DATA0_N		High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
TE		VSSI	VSSI	VSSI
SDO	Using SPI	VDDI	VDDI	VDDI
	Not using SPI	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
Source Driver Output		High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
GOUT1~GOUT32		AVSS	AVSS	AVSS

NOTE: There will be no output from TE, SDO, D23-D0, HSSI_DATA0_P/N and HSSI_DATA1_P/N during Power On/Off sequence, H/W Reset and S/W Reset

5.14.3 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 5.12	Input Valid	Input Valid	Input Valid	See Section 5.12
CSX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
D/CX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
WRX (SCL / I2C_SDA)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
RDX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
D23 to D0	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
SDI (I2C_SCL)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
VS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
PCLK	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
DE	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_CLK_P, HSSI_CLK_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA0_P, HSSI_DATA0_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA1_P, HSSI_DATA1_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid

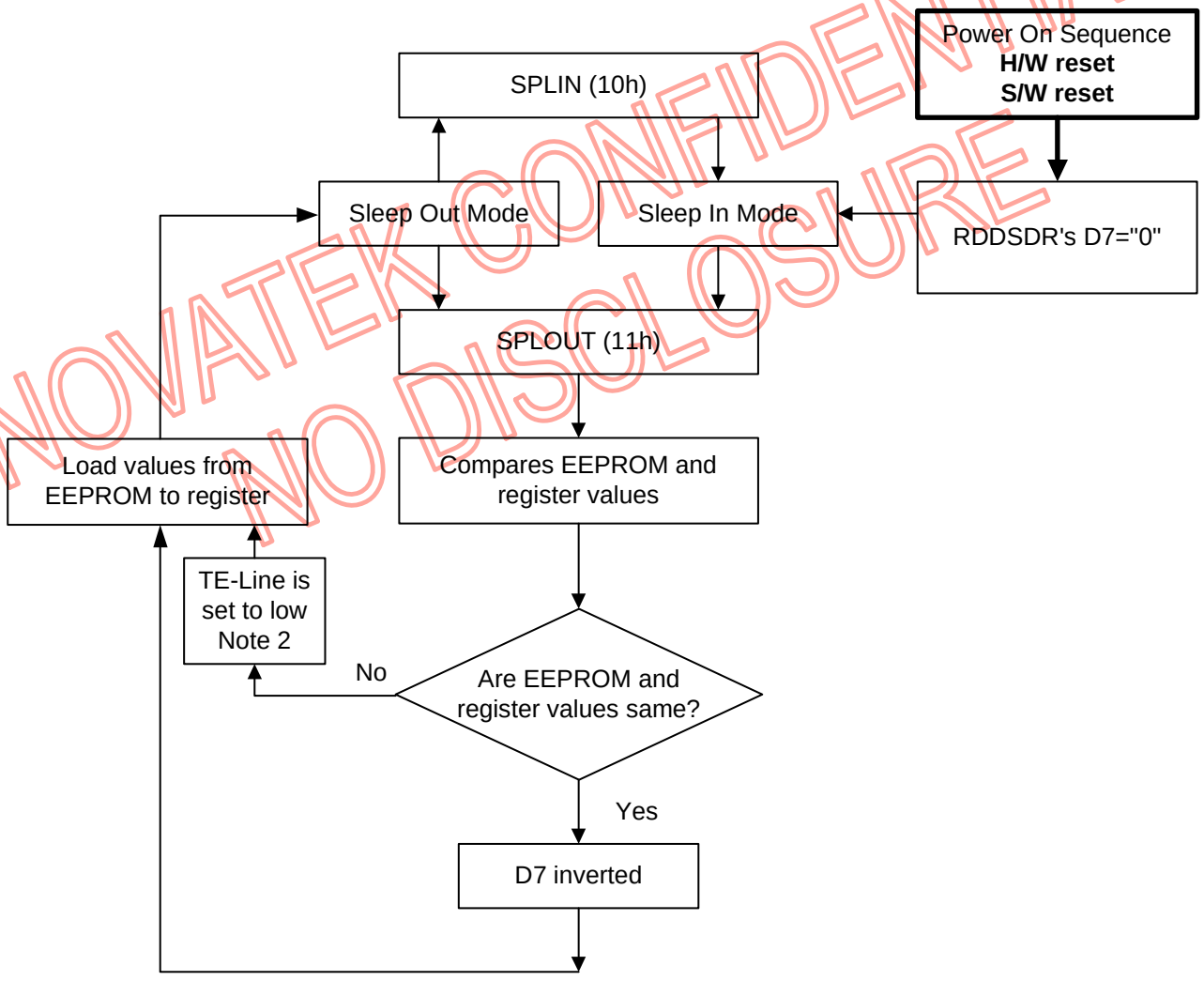
5.15 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.15.1 Register loading Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of these commands is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is following:



NOTES:

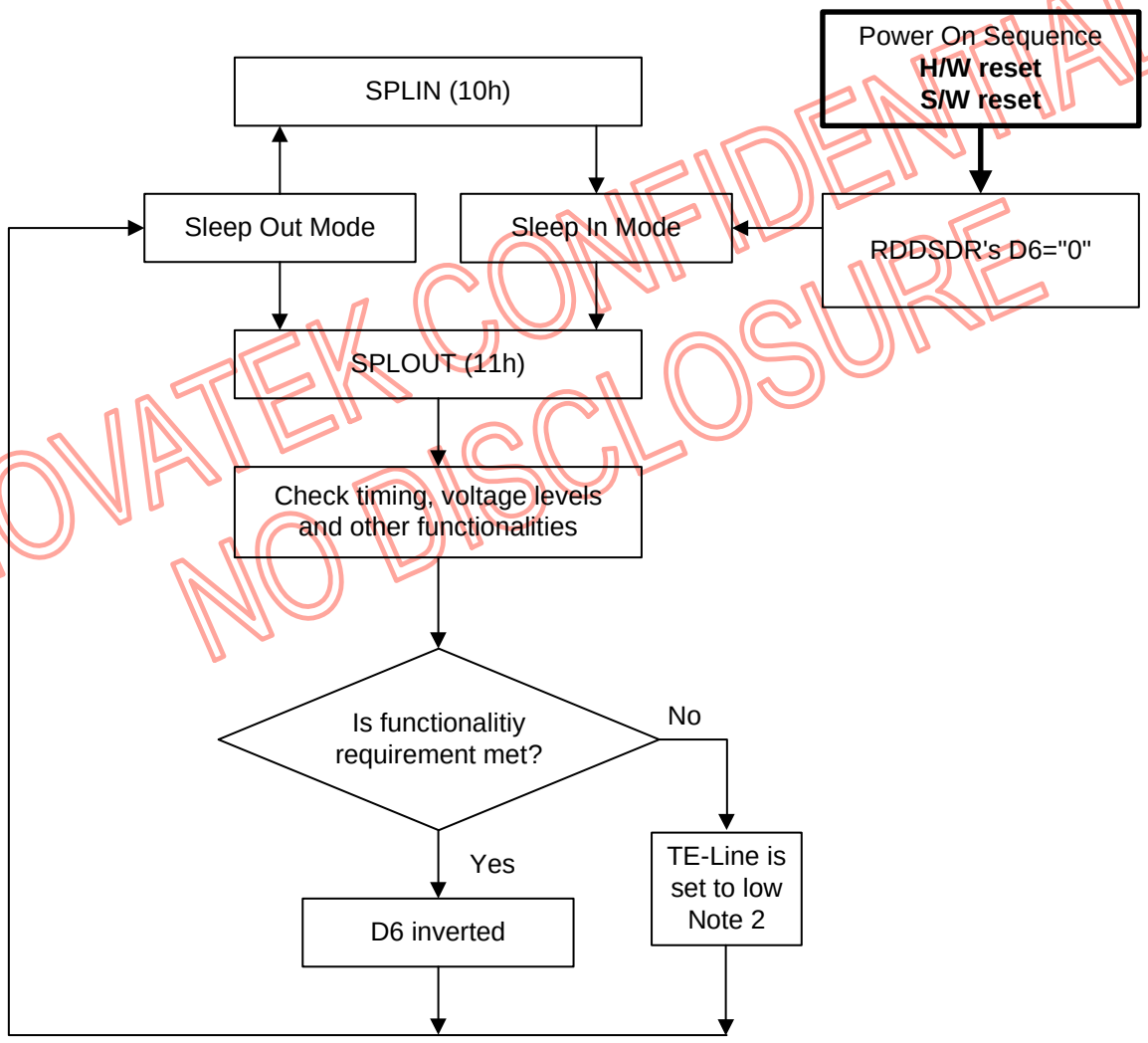
1. *There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DCh), by the display module.*
2. *This information is only used if TE line is used.*

5.15.2 Functionality Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of these commands is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is following:



NOTES:

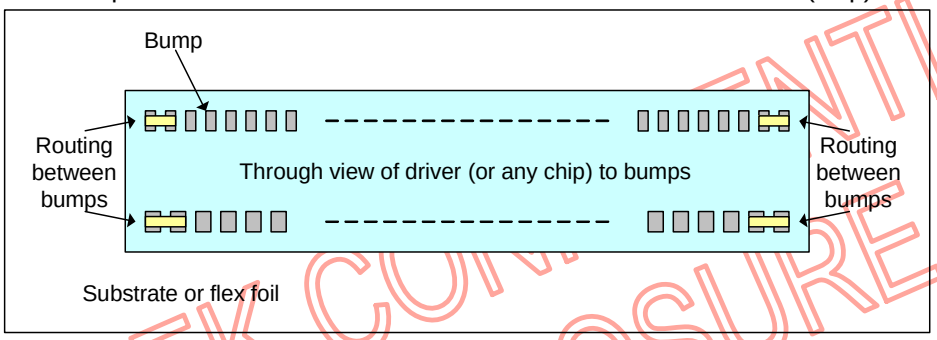
1. *There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.*
2. *This information is only used if TE line is used.*

5.15.3 Chip Attachment Detection

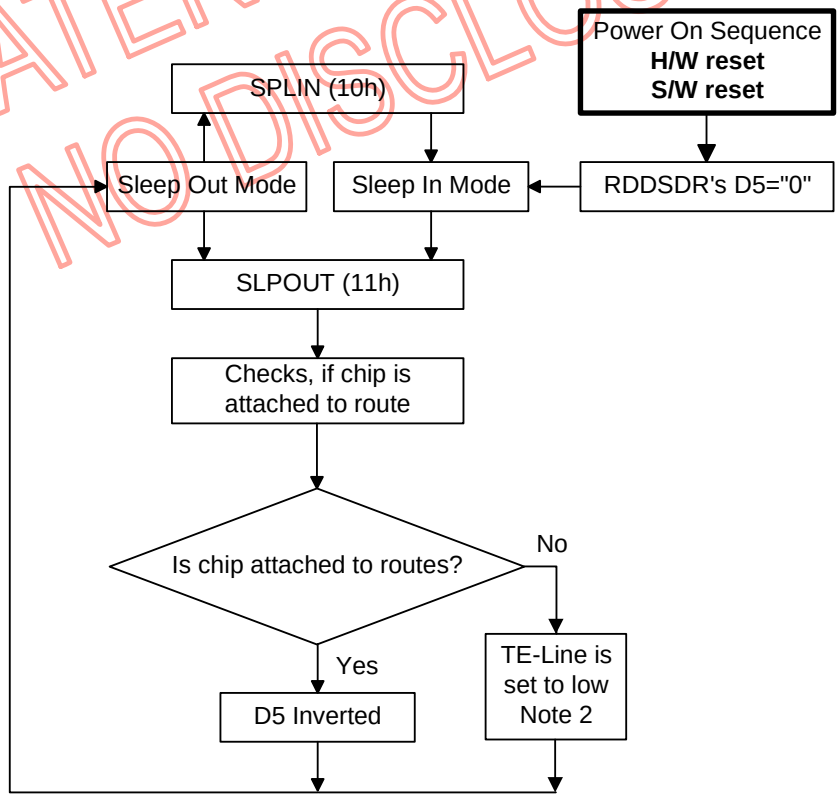
Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:



NOTE: This information is only used if TE line is used.

5.16 Display Panel Color Characteristics

Color characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel color characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted color outlook of the image on the display panel.

Used color characteristics can share 2 categories: Mandatory and Optional. The mandatory color characteristics are Black, White, Red, Green and Blue. The optional color characteristics is used if it is needed and it is called as A color (e.g. Cyan). The bits of the A color are set to '0's they are not used on the display module.

A read color characteristic value is based on 10 bit floating value where the MSB is 9^{th} bit and the LSB is 0^{th} bit. All power values of the bits are listed below:
- Bit 9: 2-1 = 0.5,
- Bit 8: 2-2 = 0.25,
- Bit 7: 2-3 = 0.125,
- Bit 6: 2-4 = 0.0625,
- Bit 5: 2-5 = 0.03125,
- Bit 4: 2-6 = 0.015625,
- Bit 3: 2-7 = 0.007813,
- Bit 2: 2-8 = 0.003906,
- Bit 1: 2-9 = 0.001953,
- Bit 0: 2-10 = 0.000977.

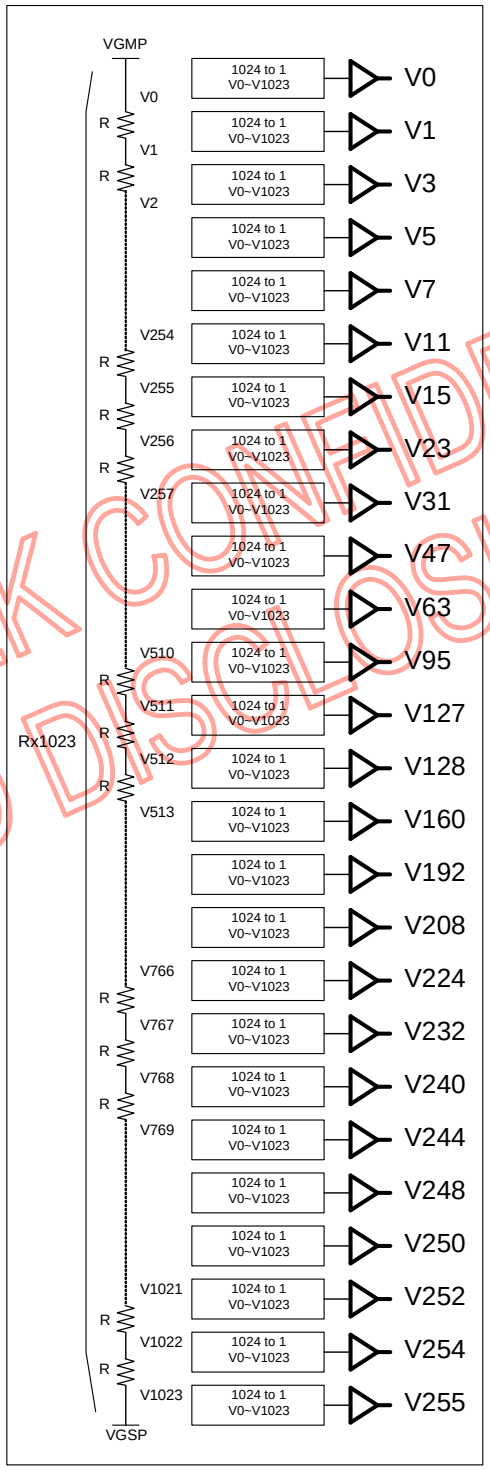
The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:
- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01 0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:
- Binary value: 10 1000 1111b
- Formula: Rx[9]x0.5+Rx[8]x0.25+Rx[7]x0.125+Rx[6]x0.0625+Rx[5]x0.03125+Rx[4]x0.015625+ Rx[3]x0.007813+Rx[2]x0.003906+Rx[1]x0.001953+R[0]x0.000977
- Use: 1x0.5+0x0.25+1x0.125+0x0.0625+0x0.03125+0x0.015625+1x0.007813+1x0.003906+ 1x0.001953+1x0.000977

See also sections:
"Read Black/White Low Bits (70h)", "Read Bkx (71h)", "Read Bky (72h)", "Read Wx (73h)", "Read Wy (74h)", "Read Red/Green Low bits (75h)", "Read Rx (76h)", "Read Ry (77h)", "Read Gx (78h)", "Read Gy (79h)", "Read Blue/AColor Low Bits (7Ah)", "Read Bx (7Bh)", "Read By (7Ch)", "Read Ax (7Dh)", "Read Ay (7Eh)".

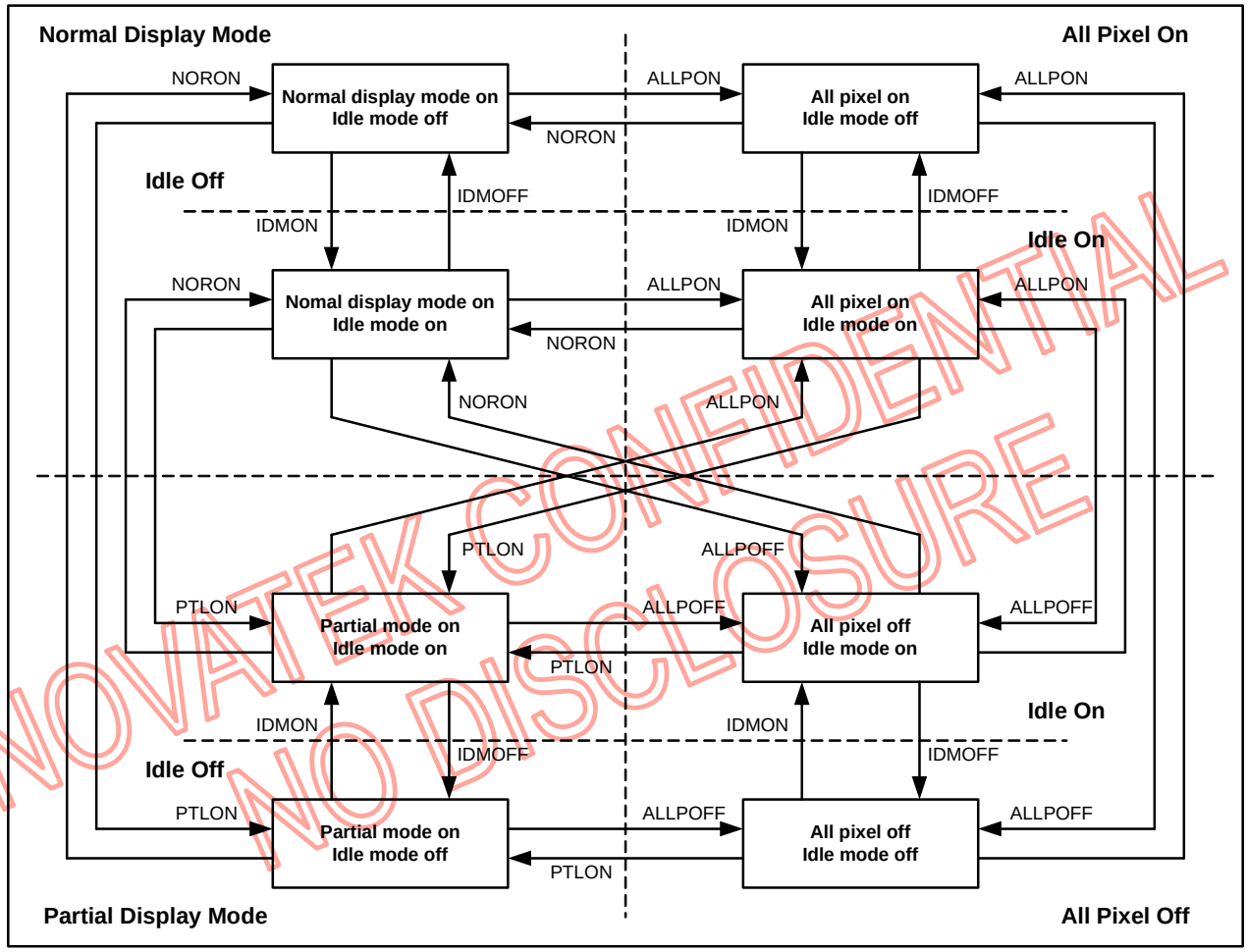
5.17 Gamma Function

The structure of grayscale amplifier is shown as below. The 26 voltage levels between VGMP and VGSP are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



5.18 Basic Display Mode

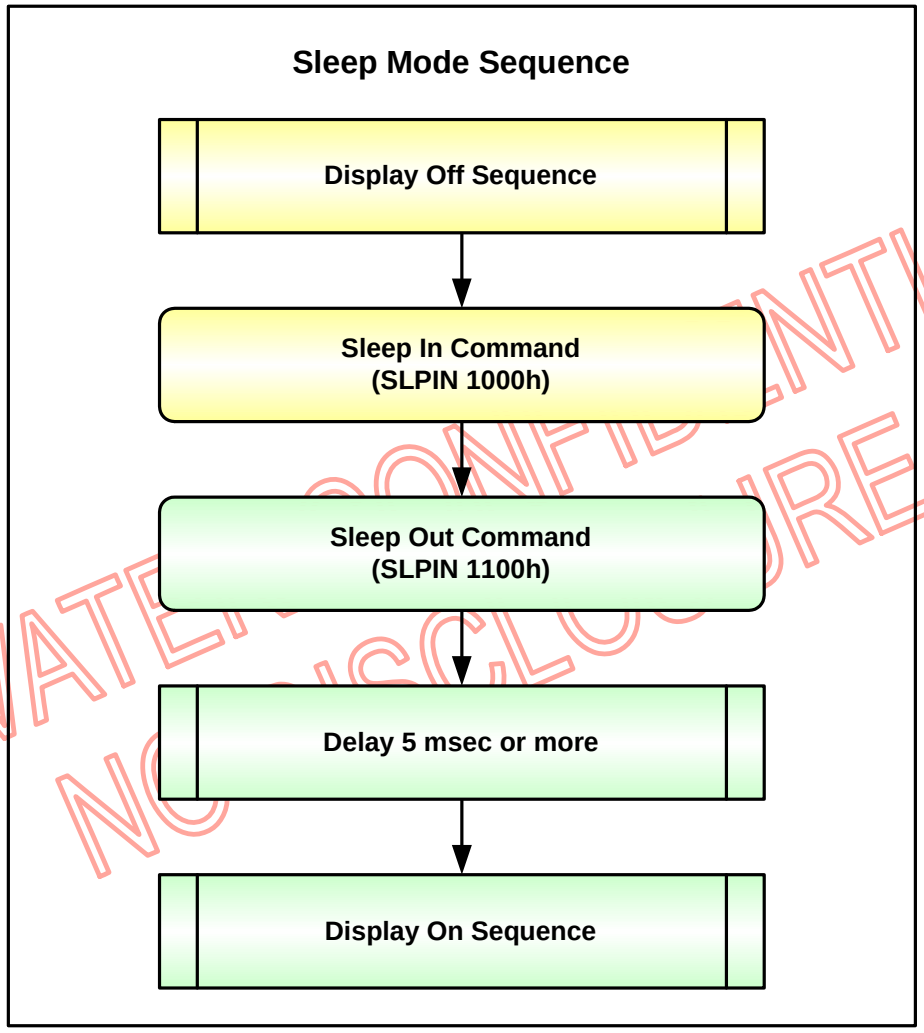
The NT35510 has some basic operation modes which are Normal Display Mode, Partial Display Mode, Idle Mode, All Pixel On and All pixel Off for panel display. User can change these display modes for each other is illustrated below.



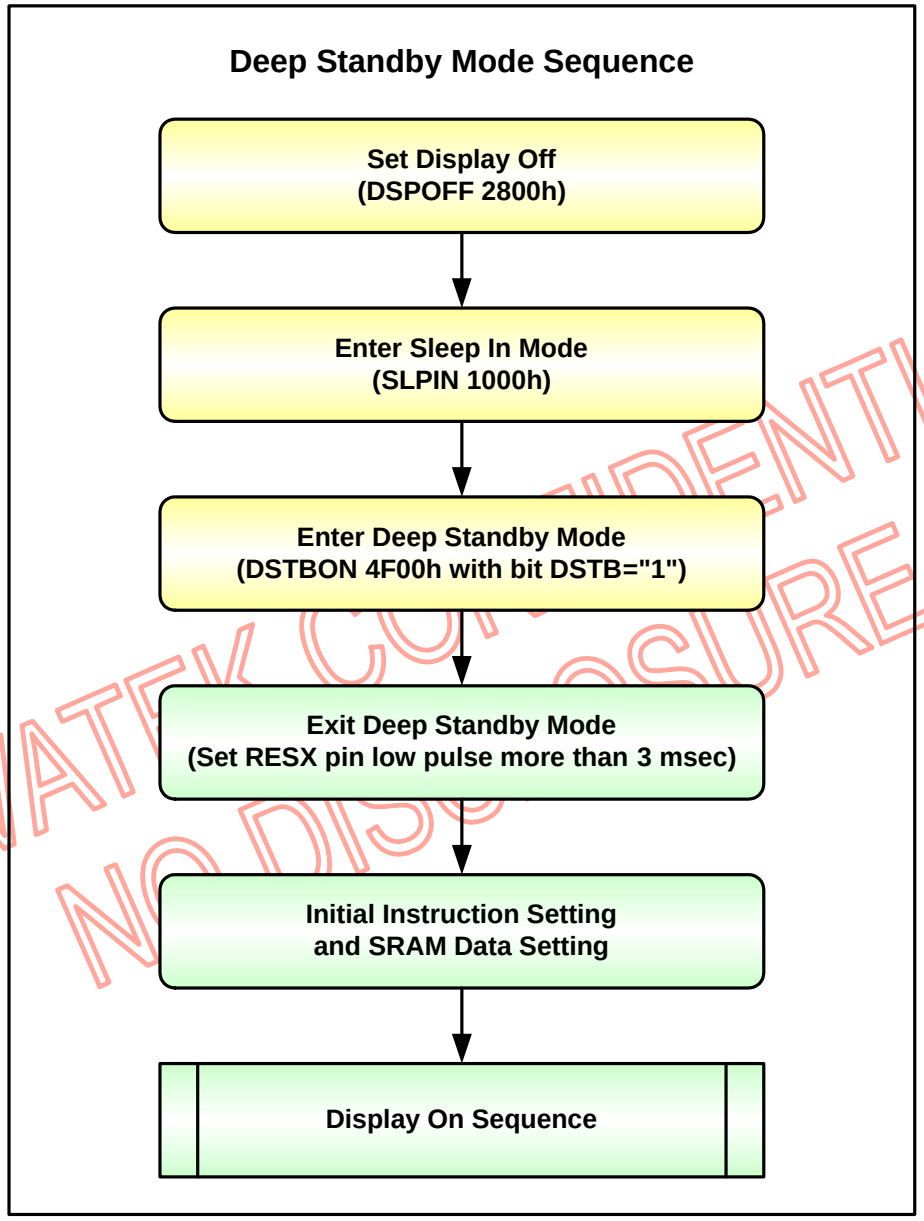
5.19 Instruction Setting Sequence

When setting instruction to the NT35510, the sequences shown in below figures must be followed to complete the instruction setting.

5.19.1 Sleep In/Out Sequence



5.19.2 Deep Standby Mode Enter/Exit Sequence



5.20 Instruction Setup Flow

5.20.1 Initializing with the Built-in Power Supply Circuits

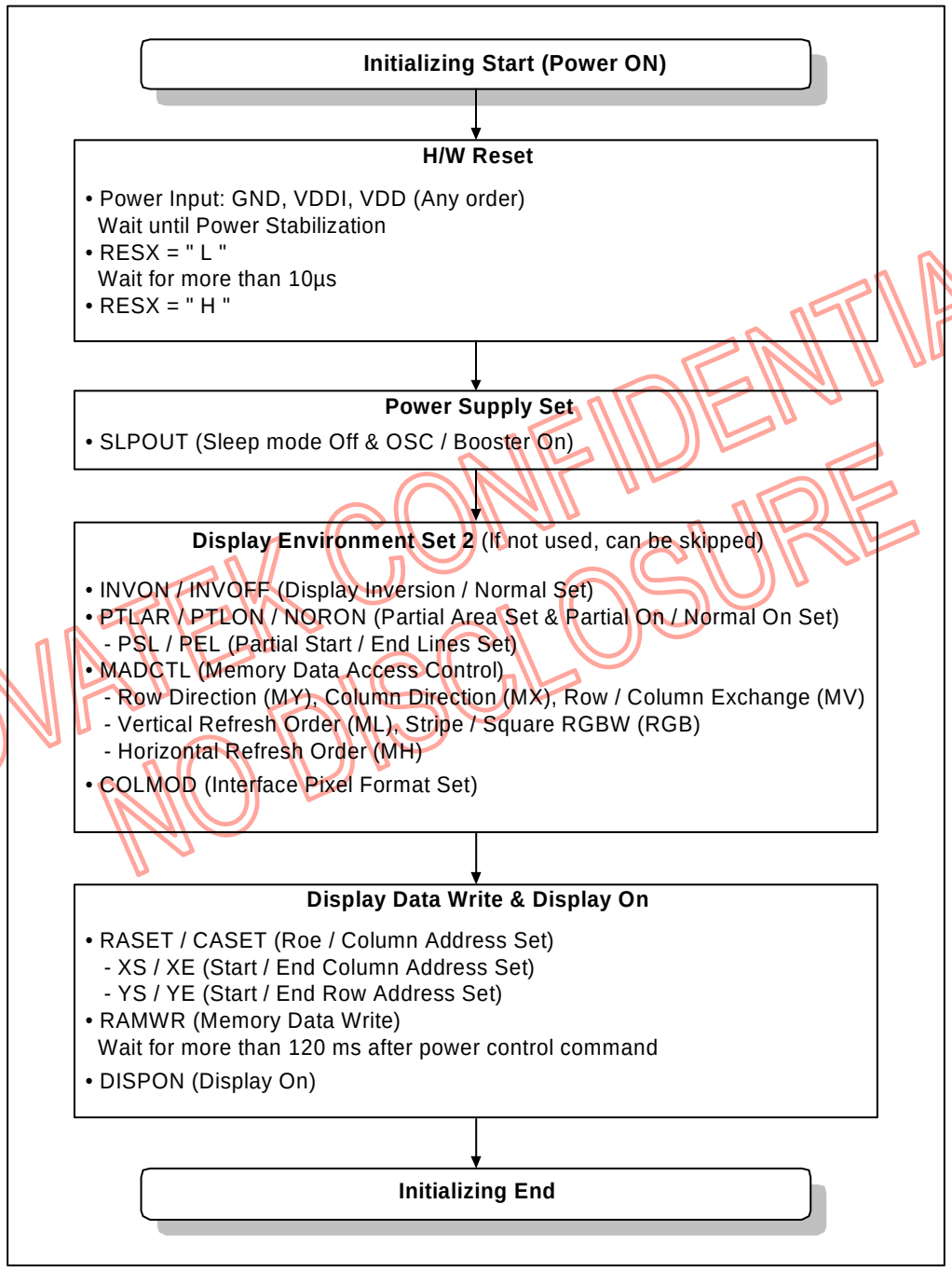


Fig. 5.20.1 Initializing with the built-in power supply circuit

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initializing.

5.20.2 Power OFF Sequence

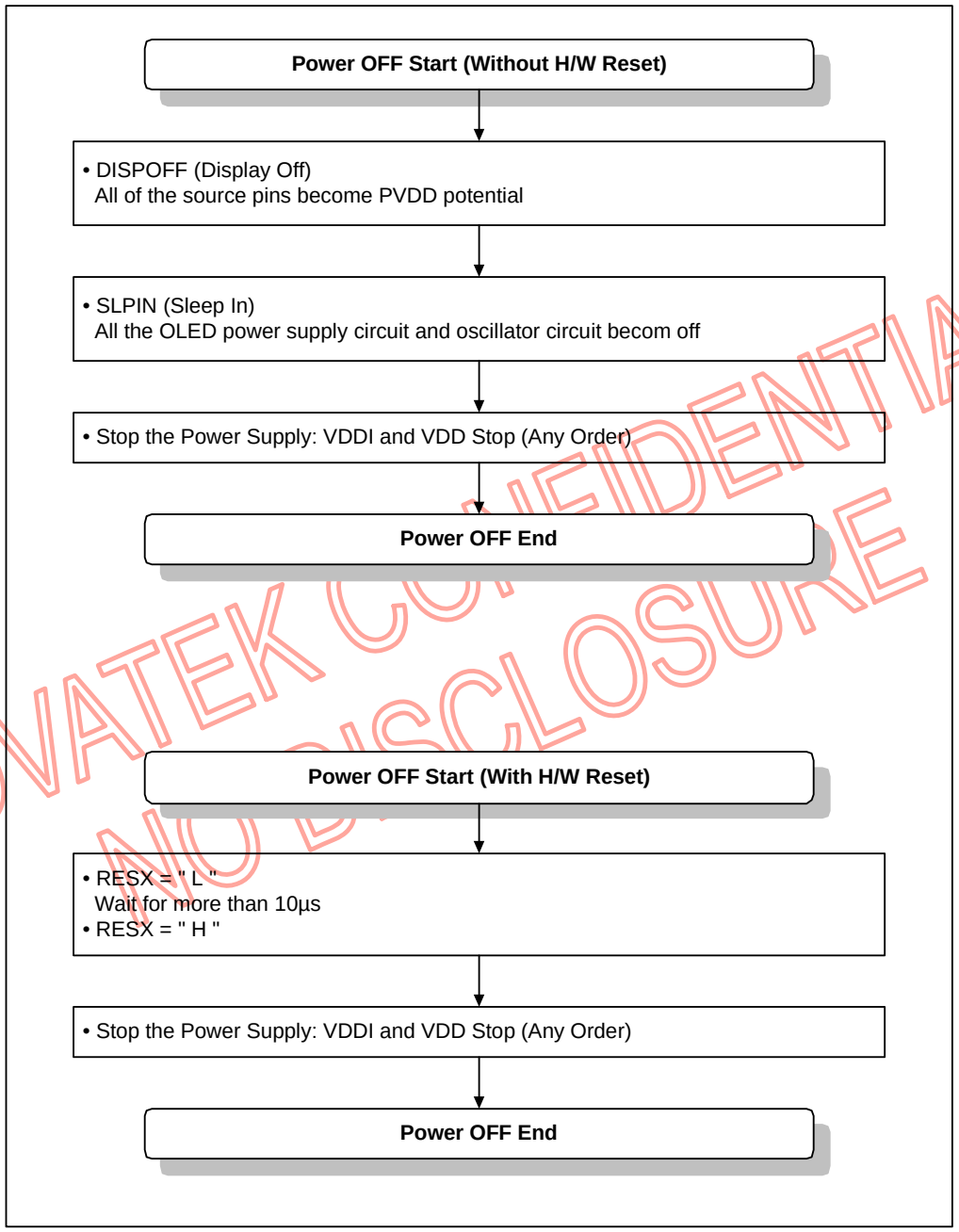
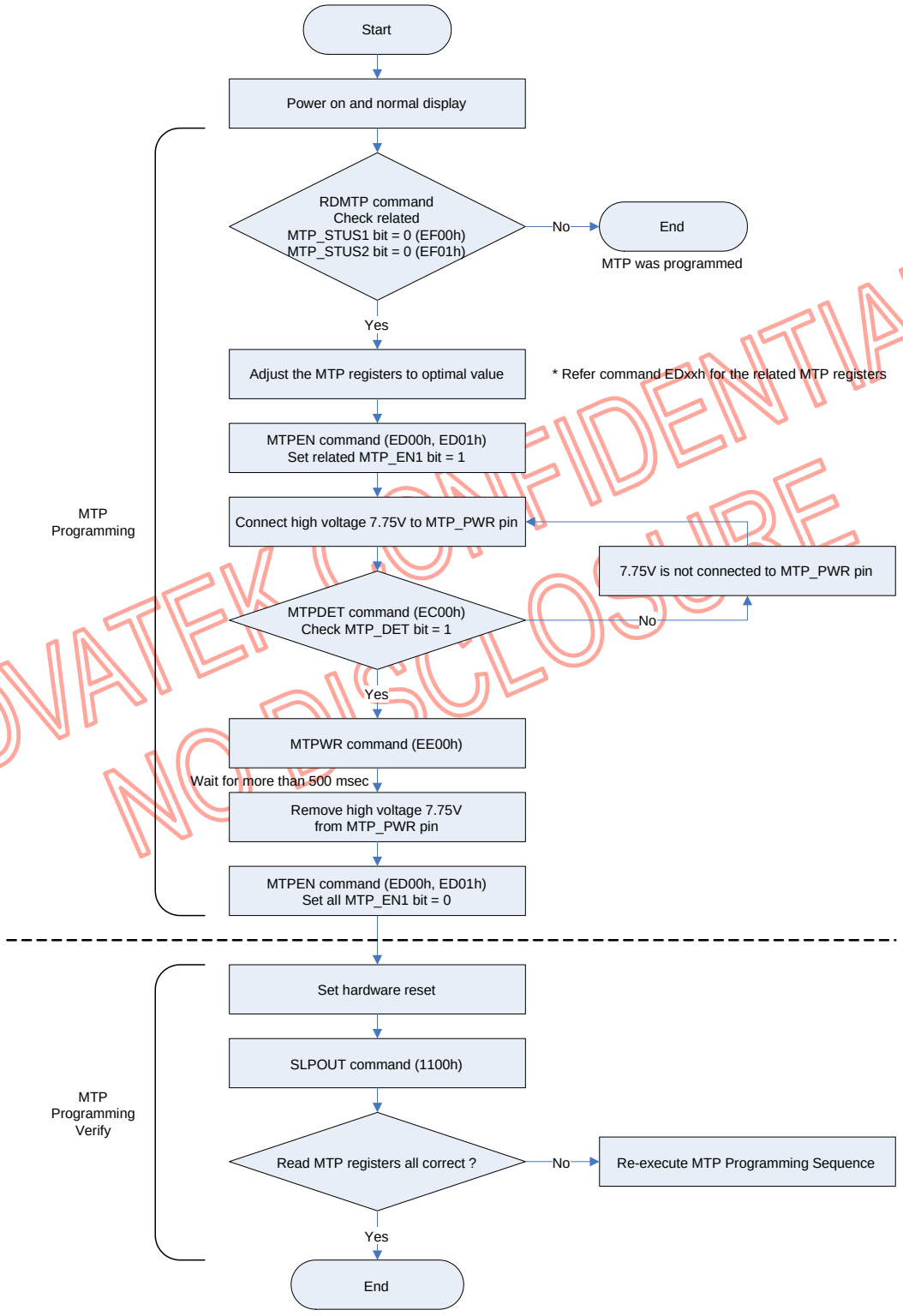


Fig. 5.20.2 Power off sequence

5.21 MTP Write Sequence



Note: The multi-times MTP must be programmed from the 1st time.
(ID1/2/3, VGMP/VGSP, VGMN/VGSN, VCOM, Gamma 2.2, VGMP/VGSP LUT)

5.22 Dynamic Backlight Control Function

The NT35510 embedded Content Adaptive Brightness Control (CABC) and Light-Sensor Automatic Brightness Control (LABC) functions. Both two functions are used to generate a proper PWM signal based on internal CABC and LABC algorithms. User could apply this PWM signal to control other device(s) (Such as power IC or LED driver IC). The function combined CABC with LABC, is simply called “Full-ABC”. When the CABC and LABC functions are enabled and cooperate with external circuits (such as LED driver circuit), the power consumption of backlight will be reduced with keeping acceptable display quality.

The CABC function of NT35510 is used to reduce the power consumption of display backlight. Contents adaptation means that the average gray level scale of image contents is increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus power consumption reduction depends on the contents of the image. The display image and brightness are dynamically processed by CABC block. The availability of this function ranges from moving picture such as TV image to still picture such as menu. However, in order to gain a better display quality and reduce the power consumption of the backlight, the NT35510 internally uses NOVATEK dynamic gamma algorithm to produce an optimal backlight control based on different image contents.

The LABC function of NT35510 is also applied to smoothly control the display backlight by sensing ambient light variation. This function includes several apparatus, such as “Flicker Removal Block” for eliminating external light source flicker (e.g. 50 and 60 Hz), and “Hysteresis Block” for preventing the luminance transient variation. The information of the ambient light is sent to the LABC block if user enables it. The user can read ambient light information or this information can be used for automatic brightness control by the LABC block. It is also available to control the brightness by adjusting PWM duty manually.

So combined the CABC with LABC processed results, the display output brightness is:

Display Backlight Brightness = LABC Backlight Brightness Ratio (or Manual Setting Ratio) x CABC Brightness Ratio

Table 5.22.1 Display Brightness Output When CABC and LABC Function are Enable

Example	A	B	A x B	Brightness Output of LEDPWM	Image Status
	Brightness Ratio (LABC or Manual)	Brightness Ratio (CABC or Manual)	Calculation Result		
Example 1	70%	50%	35%	35%	CABC Modified
Example 2	80%	100%	80%	80%	CABC Modified
Example 3	50%	30%	15%	15%	CABC Modified

One of Full-ABC applications is simply illustrated in the **Fig. 5.22.1**. This application is used to dynamic control the backlight power consumption. The LEDPWM is an output-type pin which can output a PWM signal to control the display backlight brightness. The “LEDON” pin can output a “Enable / Disable” signal if the external LED driver IC needs this signal. The PWM duty cycle of “LEDPWM” is determined by CABC and LABC processed results. The external LED driver ICs are necessary in order to transfer the PWM signal into driving power for LED backlight.

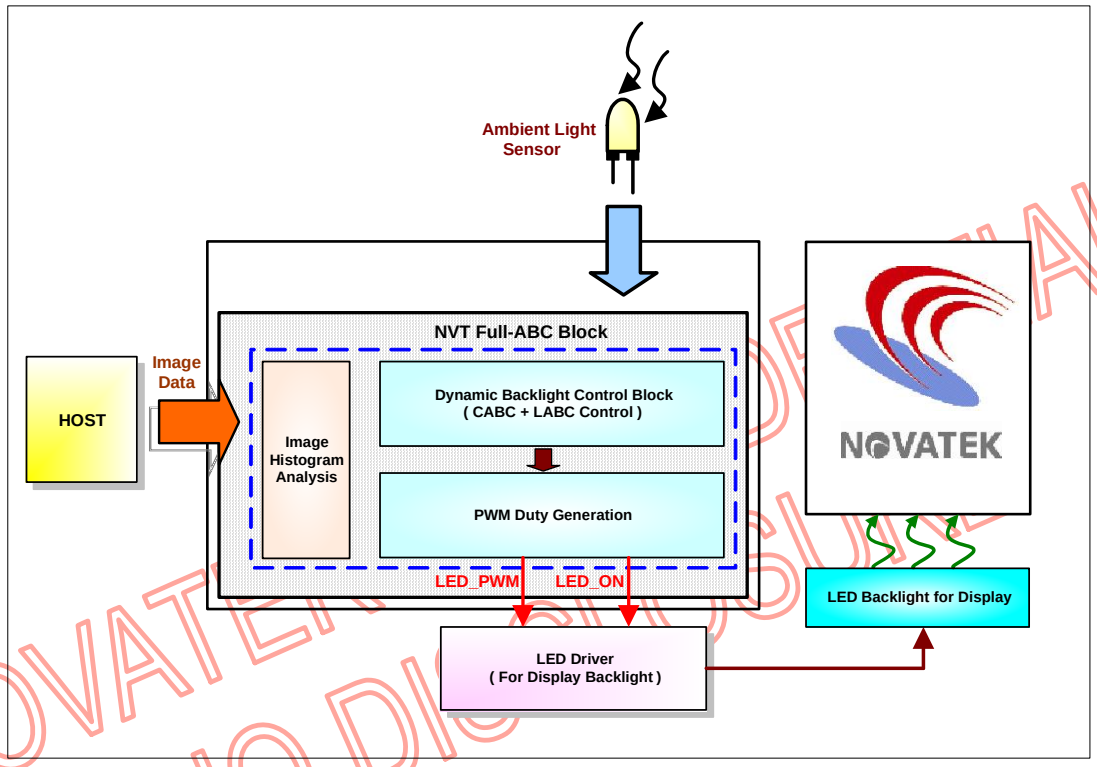


Fig. 5.22.1 One Application of Full-ABC Dynamic Backlight Brightness Control

5.22.1 PWM Control Architecture

PWM duty for LED backlight control is determined from CABC and LABC block. The below diagram illustrates the duty combination architecture and its corresponding control registers.

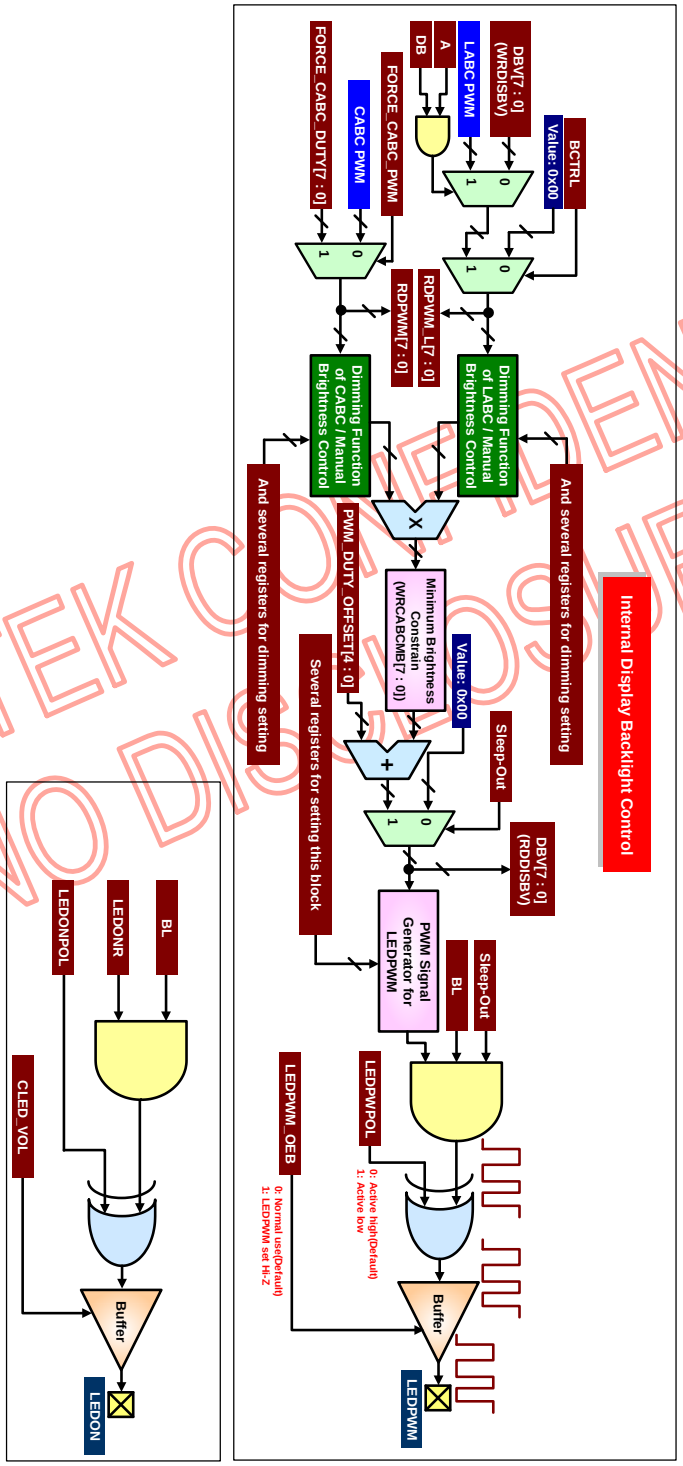


Fig. 5.22.2 Internal Display Backlight Control Combined with CABC and LABC

As shown in **Fig. 5.22.2**, the register bit “BL” is used to control the “LEDPWM” pin to output PWM signal. Normally, if user want to disable the display backlight completely and immediately, user can set “BL” = “0”. The below table shows some applications of register bit “LEDPWPOL”:

BL	LEDPWPOL	Status of LEDPWM Pin	Display Backlight Status
0	0	0 (Default)	Off
0	1	1	Off
1	0	Original polarity of PWM signal	On
1	1	Inversed polarity of PWM signal	On

In the same way, the register bits “LEDONPOL” and “BL”, are used to control the “LEDON” pin. See the below table.

BL	LEDONPOL	Status of LEDON Pin
0	0	0 (Default)
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

The setting bit “CLED_VOL” is applied to choose different output logical voltage level for LEDON, LEDPWM pins. This bit is valid when (1) DSTB_DEL=low or (2) DSTB_SEL=high, VDDI=1.65~3.3V and VSEL=high (The output level is VSSI to DIOPWR for other VDDI and VSEL conditions in DSTB_SEL=high). See below for the selection output level.

CLED_VOL	LEDON/LEDPWM Output Level
0	VSSI to VDDI
1	VSSI to VDDA

The setting bit “BCTRL” is used to enable / disable the display backlight control functions (such as LEDPWM). When user set “BCTRL” = “0”, then the backlight will be turned off with dimming function, and the value of register DBV[7:0] (RDDISBV) will be “00h” after dimming period.

BCTRL	Value of DBV[7:0] (RDDISBV)	Display Backlight Status
0	00h	Off
1	Determined by CABC and LABC estimations	On

The setting bit “A” is used to enable / disable the ambient light sensor and LABC functions. Sampling of ambient light started after setting the register bit “A”. First averaged value should be output for 500ms. The below table shows this function.

Diver IC State	A	DB	ADC_EN	The Statue of Internal A/D Converter	Display Brightness Control
Sleep-In	x	x	x	Disabled	Disable
Sleep-Out	0	0	0	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	0	0	1	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	0	1	0	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	0	1	1	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	1	0	0	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	1	0	1	Disable	Control by manual setting DBV[7:0] (Here means from WRDISBV)
Sleep-Out	1	1	0	Disable	Control by LABC function (See Note 1)
Sleep-Out	1	1	1	Enable	Control by LABC function (See Note 2)

NOTES:

1. User has to write the ambient light information into the register LS[15:0] via system interface..

2. The internal 10-bit ADC converter is enabled and the display backlight brightness is controlled automatically.

The setting bit “DB” is used to manual / automatic brightness control. When “DB”=”0”, the display backlight brightness can be affected by setting register DBV[7:0] (here means WRDISBV) manually. Here are listed some important applications with register bits “DB”, “A”, DBV[7:0] (WRDISBV), RDPWM[7:0], and RDPWM_L[7:0] in below table.

CABC Status: Off Mode (RDPWM[7:0] will be FFh) “FORCE_CABC_PWM”=“0”, WRCABCMB[7:0] = 00h, PWM_DUTY_OFFSET[4:0]=00h, “BL”=“1”, “BCTRL”=“1”, Sleep-Out Mode				
DB	**A**	**Value of RDPWM_L[7:0]**	**Value of RDPWM [7:0]**	**Display Backlight Brightness**
0	0	Determined by DBV[7:0] (Here means from WRDISBV)	FFh	Determined by DBV[7:0] manually (Here means from WRDISBV)
0	1	Determined by DBV[7:0] (Here means from WRDISBV)	FFh	Determined by DBV[7:0] manually (Here means from WRDISBV)
1	0	Determined by DBV[7:0] (Here means from WRDISBV)	FFh	Determined by DBV[7:0] manually (Here means from WRDISBV)
1	1	Determined by LABC Function	FFh	Determined by LABC Function

CABC Status: UI-Mode / Still-Mode / Moving-Mode “FORCE_CABC_PWM” = “0”, WRCABCMB[7:0]=00h, PWM_DUTY_OFFSET[4:0]=00h, “BL”=“1”, “BCTRL”=“1”, Sleep-Out Mode				
DB	**A**	**Value of RDPWM_L[7: 0]**	**Value of RDPWM [7: 0]**	**Display Backlight Brightness**
0	0	Determined by DBV[7:0] (Here means from WRDISBV)	Determined by CABC Function	Determined by DBV[7:0] x CABC Function (Here means DBV[7:0] from WRDISBV)
0	1	Determined by DBV[7:0] (Here means from WRDISBV)	Determined by CABC Function	Determined by DBV[7:0] x CABC Function (Here means DBV[7:0] from WRDISBV)
1	0	Determined by DBV[7:0] (Here means from WRDISBV)	Determined by CABC Function	Determined by DBV[7:0] x CABC Function (Here means DBV[7:0] from WRDISBV)
1	1	Determined by LABC Function	Determined by CABC Function	Determined by LABC Function x CABC Function

Writing the register DBV[7:0] (WRDISBV) in command address 5100h (51h for MIPI command address) is used o adjust the backlight brightness value when LABC function of the NT35510 is disabled (LABC function is disabled when register bit “A” is set as “0”). However, reading register DBV[7:0] (RDDISBV) from command address 5200h (52h for MIPI command address) is used to indicate the real PWM duty variation.

The register setting CMB[7:0] is used to limit the minimum PWM duty in order to prevent the backlight brightness too dark.

The register FORCE_CABC_DUTY[7:0] is used to perform a fixed PWM duty of CABC output while the register bit “FORCE_CABC_PWM” is set as “1”.

The “Sleep-Out” is a flag in order to indicate the driver IC is in “Sleep-Out” mode. Here are listed some conditions when driver IC is in Sleep-In or Sleep-Out status.

Driver IC Status	Sleep-Out Flag	CABC Function	LABC Function	Dimming Functions for CABC or LABC	Display Backlight Status
Sleep-In	0	Not Available	Not Available	Not Available	Turn-Off
Sleep-Out	1	Available	Available	Available	Controllable

The NT35510 provides one dimming function for CABC and LABC / Manual Brightness Control, and this dimming functions can be enabled / disabled by register bit DD as the following table.

Enable Control for CABC Dimming Function		Enable Control for LABC Dimming Function	
“DD” = “0”	Disable Dimming Function of CABC	“DD” = “0”	Disable Dimming Function of LABC
“DD” = “1”	Enable Dimming Function of CABC	“DD” = “1”	Enable Dimming Function of LABC

In other words, the dimming functions of CABC and LABC can be enabled / disabled together by setting register bit “DD”.

5.22.2 Dimming Function for LABC and Manual Brightness Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. The dimming function curves for LABC and Manual Brightness Control can be configured the same or not the same in increment and decrement directions. The basic idea is described below.

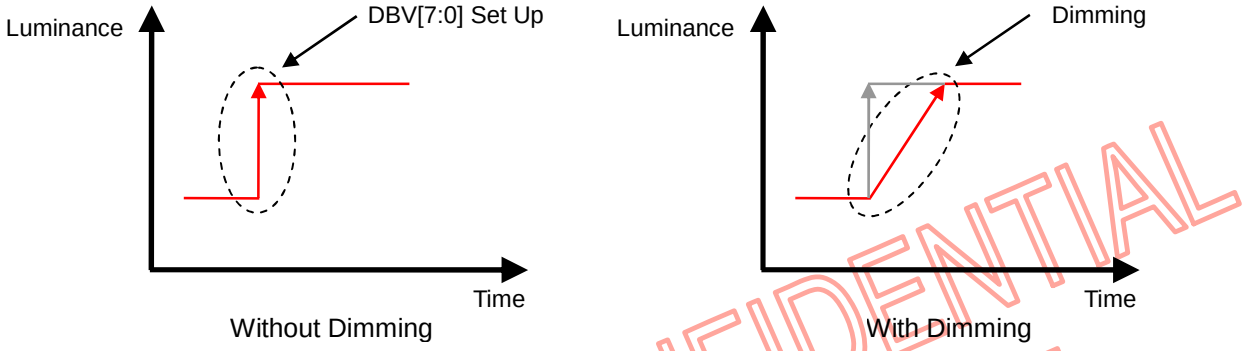


Fig. 5.22.3 Basic Concept of Dimming Function

The NT35510 provides two types PWM duty dimming mechanism for LABC and manual brightness control. One is called “Fixed-Time Dimming”, the other is called “Fixed-Slope Dimming”. The dimming type can be selected by register bit “SEL_IN” for rising dimming (increment dimming), and bit “SEL_DE” for falling dimming (decrement dimming).

SEL_IN	SEL_DE	Rising Dimming Type	Falling Dimming Type
0	0	Fixed-Time Dimming	Fixed-Time Dimming
0	1	Fixed-Time Dimming	Fixed-Slope Dimming
1	0	Fixed-Slope Dimming	Fixed-Time Dimming
1	1	Fixed-Slope Dimming	Fixed-Slope Dimming

Fixed-Time Dimming Type

The total dimming steps and each step time can be set by registers DMSTP_L[2:0], DM_IN[3:0], and DM_DE[3:0], respectively. These three registers can determine some characteristics of dimming curves. The **Fig. 5.22.4** illustrates the “Fixed-Time” dimming curves. The unit of registers DM_IN[3:0] and DM_DE[3:0] is “frame(s) per step”. The unit of register DMSTP_L[2:0] is “step(s)”

For Example:

If register bits “SEL_IN” = “0” (Fixed-Time dimming for rising dimming), another register bit “SEL_DE” = “1” (Fixed-Slope dimming for falling dimming), and

DM_IN[3:0] is set as 0x07 (means 8 frames time for each step)

DMSTP_L[2:0] is set as 0x01 (means total dimming steps is 4 steps)

So the total dimming time of “rising dimming” is 32-frames time length (8 frames x 4).

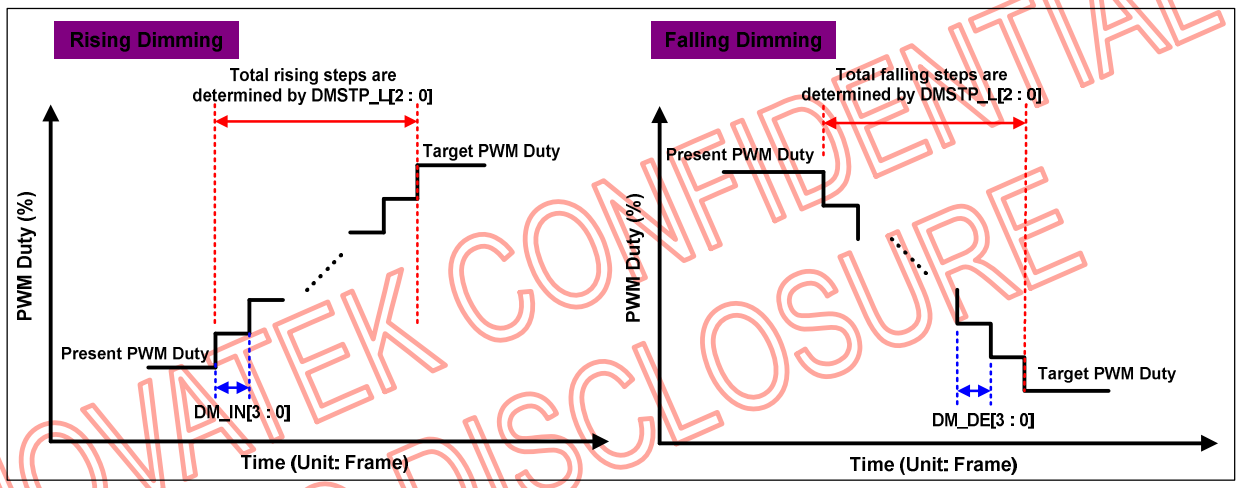


Fig. 5.22.4 Fixed-Time Dimming Curve for LEDPWM

Fixed-Slope Dimming Type

The increasing / decreasing PWM duty and each step time can be set by register STEP_IN[3:0], STEP_DE[3:0], DM_IN[3:0], and DM_DE[3:0], respectively. These three registers can determine some characteristics of dimming curves. The **Fig. 5.22.5** illustrates the “Fixed-Slope” dimming curves. The unit of registers STEP_IN[3:0] and STEP_DE [3:0] is “duty ratio” (FFh is 100%, and 00h is 0%). The unit of register DM_IN[3:0] and DM_DE[3:0] is “frame(s) per step”.

For Example:

If register bits “SEL_IN” = “0” (Fixed-Time dimming for rising dimming), another register bit “SEL_DE” = “1” (Fixed-Slope dimming for falling dimming), and

DM_DE[3:0] is set as 0x02 (means 3 frames time for each step)

STEP_DE[3:0] is set as 0x05 (means PWM decrement is 5)

When present PWM duty is 0x64 (100 in decimal), target PWM duty is 0x14 (20 in decimal), so the total dimming steps will be:

Total dimming steps = (Present PWM Duty - Target PWM duty) / (PWM decrement)
= (100 - 20) / 5
= 16 steps

So total dimming time for falling dimming is 48 frames (16 Steps x 3)

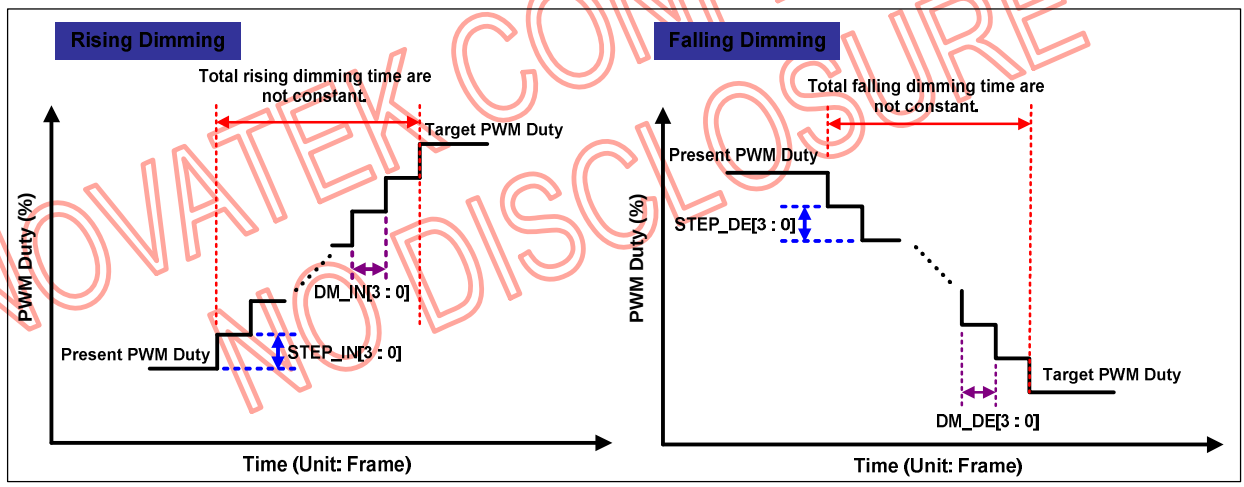


Fig. 5.22.5 Fixed-Slope Dimming Curve for LEDPWM

5.22.3 Dimming Function for CABC and Force PWM Function

The NT35510 provides “Fixed-Time” and “Fixed-Slope” dimming function for CABC and Force PWM Function. The “Fixed-Slope” dimming for all CABC mode and the “Fixed-Time” dimming for CABC Off-Mode/UI-Mode use the same registers as LABC for setting (refer to **Fig. 5.22.5** and **Fig. 5.22.4**). The **Fig. 5.22.6** and **Fig. 5.22.7** illustrate the “Fixed-Time” dimming curves for CABC Still-Mode and Moving-Mode respectively.

Dimming Type	CABC Mode	Registers for Rising Dimming Setting	Registers for Falling Dimming Setting
Fixed-Slope	All Modes	STEP_IN[3:0] and DM_IN[3:0]	STEP_DE[3:0] and DM_DE[3:0]
Fixed-Time	Off-Mode	DMSTP_L[2:0] and DM_IN[3:0]	DMSTP_L[2:0] and DM_DE[3:0]
Fixed-Time	UI-Mode	DMSTP_L[2:0] and DM_IN[3:0]	DMSTP_L[2:0] and DM_DE[3:0]
Fixed-Time	Still-Mode	DIM_STEP_STILL[2:0] and DM_IN[3:0]	DIM_STEP_STILL[2:0] and DM_IN[3:0]
Fixed-Time	Moving-Mode	DIM_STEP_MOV[2:0] and DM_IN[3:0]	DIM_STEP_MOV[2:0] and DM_IN[3:0]

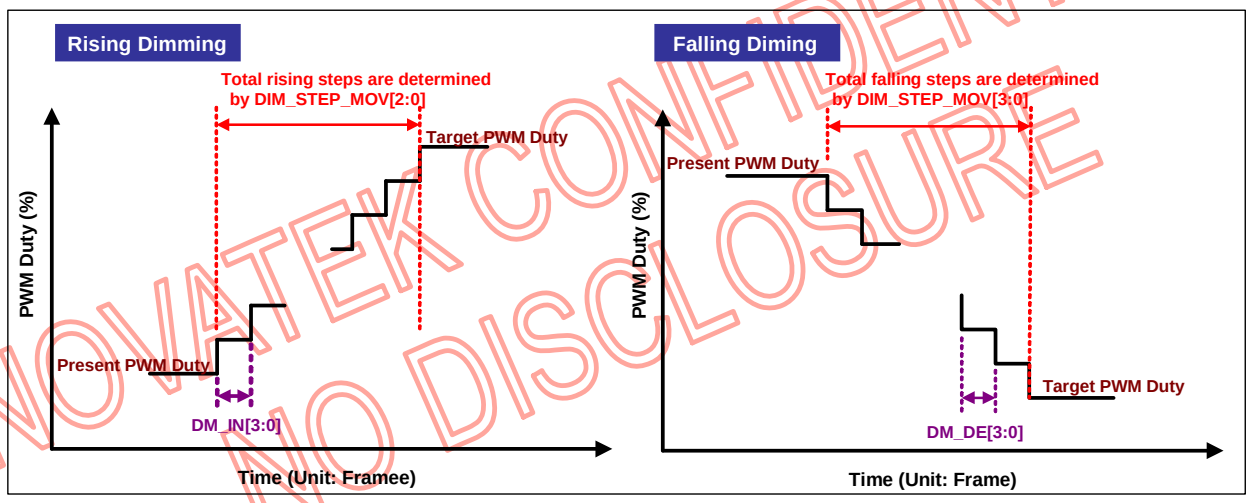


Fig. 5.22.6 Dimming Mechanism in CABC Still-Mode

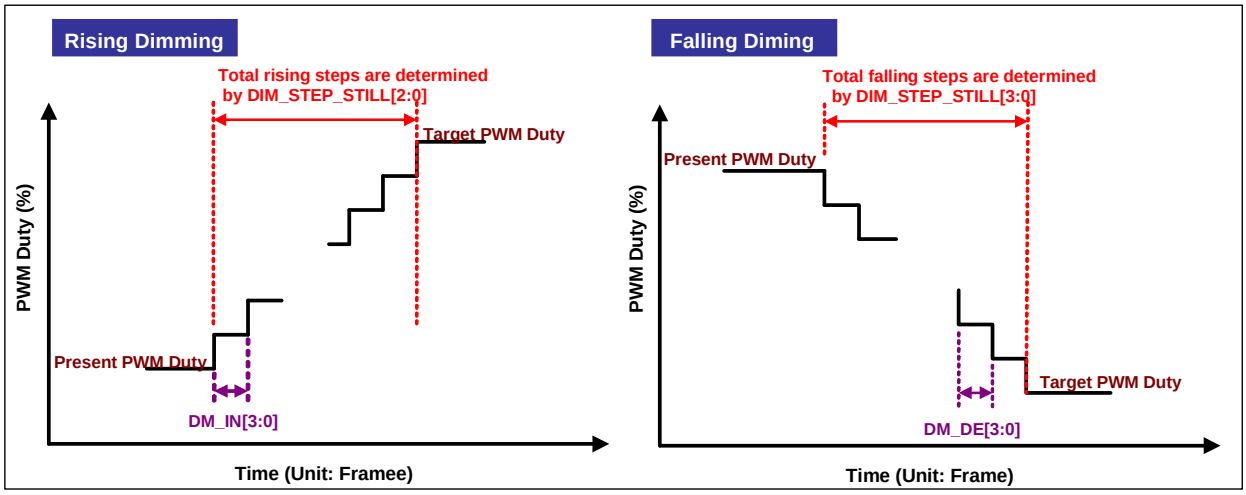


Fig. 5.22.7 Dimming Mechanism in CABC Moving-Mode

5.22.4 PWM Signal Setting for CABC and LABC

The registers PWMDIV[7:0] and PWM_DUTY_OFFSET[4:0] can change the frequency and duty compensation of the PWM signal. The PWM operation frequency "FOSC" is "not" the real PWM frequency, the "FOSC" is used to provide clock source for the internal PWM circuit. Two PWM operation frequency can be chosen by setting register "PWMF", and the real PWM frequency can be quickly estimated by the bellow formula.

PWMF Setting	PWM Operation Frequency (FOSC)	Real PWM Frequency of LEDPWM
0	5 MHz	$\text{PWM Frequency} = \frac{5\,\text{MHz}}{256 \times \text{PWMDIV}[7:0]}$
1	10 MHz	$\text{PWM Frequency} = \frac{10\,\text{MHz}}{256 \times \text{PWMDIV}[7:0]}$

For Example:

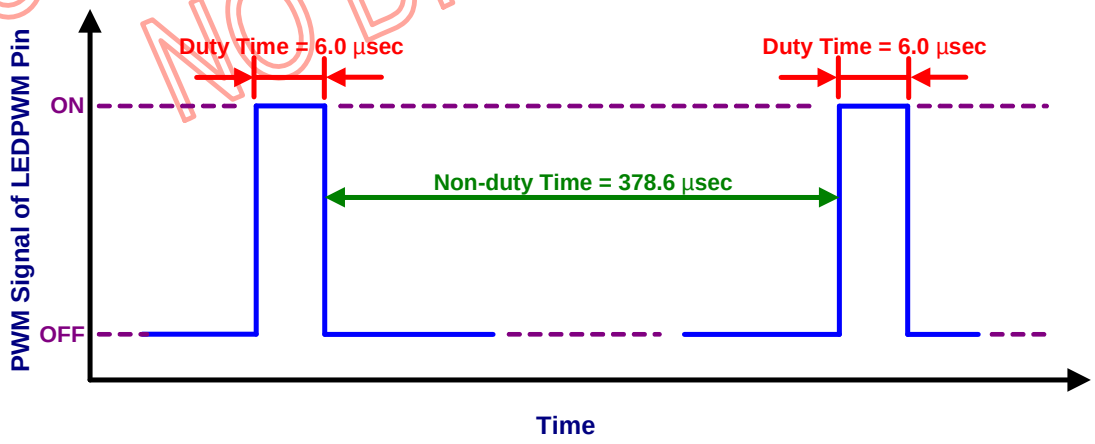
If the "PWMDIV[7:0]" = 0x0F, and "PWMF" = "1", then

$$\text{PWM Frequency} = \frac{10\,\text{MHz}}{256 \times \text{PWMDIV}[7:0]} = \frac{10\,\text{MHz}}{256 \times 15} \approx 2.60\,\text{KHZ}$$

In this condition, when PWM duty is estimated as "4" (Reading the register "DBV[7:0]" = 03h from RDDISBV), then the duty time of the PWM signal can be estimated as shown in below.

$$\text{PWM Duty Time} = \frac{4}{256} \times \frac{1}{2.60\,\text{KHz}} = 6.0\,\mu\text{sec}$$

$$\text{PWM Non-Duty Time} = \frac{(256-4)}{256} \times \frac{1}{2.60\,\text{KHz}} = 378.6\,\mu\text{sec}$$



The same, when PWM frequency is 2.60 KHz, and PWM duty of LEDPWM is 256 (Reading the register "DBV[7:0]" = FFh from RDDISBV), then the duty time can be estimated as shown in below.

$$\text{PWM Duty Time} = \frac{256}{256} \times \frac{1}{2.60\,\text{KHz}} = 384.6\,\mu\text{sec}$$

Because the external LED driver needs some stable time to drive the LED backlight, this necessary stable time will reduce the effective PWM duty period, so the PWM_DUTY_OFFSET[4:0] is used to compensate effective PWM duty.

An example is shown in **Fig. 5.22.8**. When PWM duty of LEDPWM signal is 60%, the backlight brightness should be 60% of original. But user may find that the backlight brightness is 57% of original. So user can set PWM_DUTY_OFFSET[4:0] and let the backlight brightness becomes 60% of original.

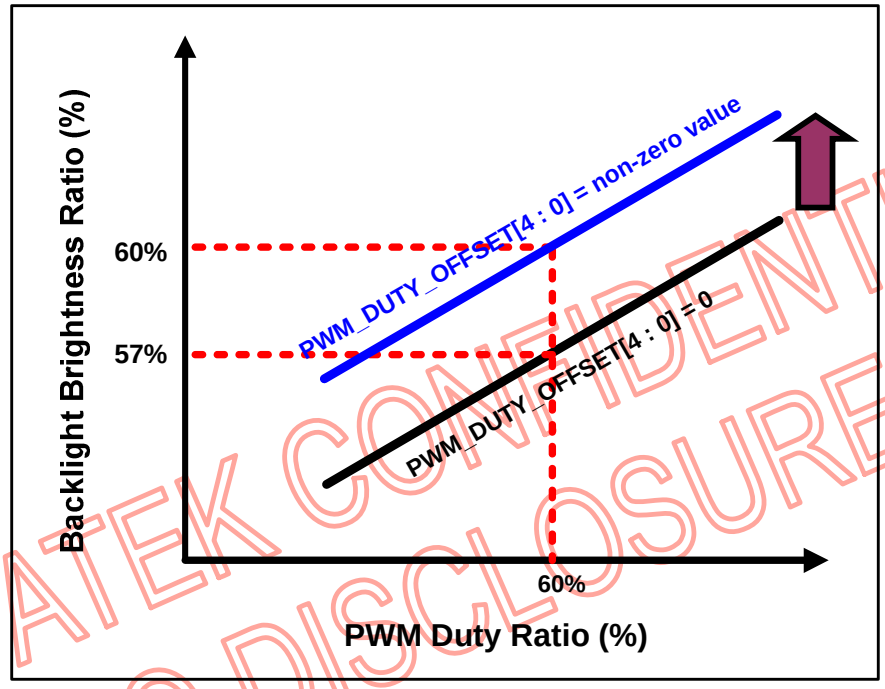
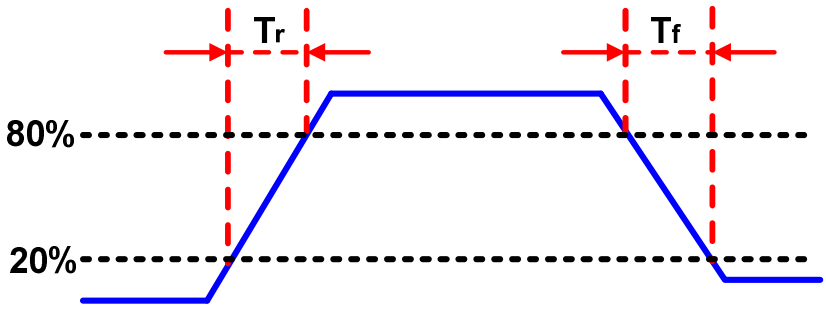


Fig. 5.22.8 Duty Compensation of PWMLED Signal

NOTE: The rising time (Tr) and falling time (Tf) of the "LEDPWM" signal are stipulated to be equal to or less than 15ns when maximum load is 30pF.



5.22.5 Content Adaptive Brightness Control (CABC)

A Content Adaptive Brightness Control (CABC) function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously decreasing brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. The NOVATek CABC algorithm can adjust the brightness of each gray level without changing the original image contents.

The NOVATek CABC function provides four operation modes, and these modes can be selected by the register 5500h. See command “Write Content Adaptive Brightness Control (5500h)” (bit C[1:0]) for more information. These four modes are described as below.

- Off Mode

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, the NT35510 will use the original Gamma 2.2 registers setting for display. And if the function of “forced PWM duty” is turn-off (i.e. “FORCE_CABC_PWM” is set as “0”), the brightness ratio of CABC is 100% (“RDPWM[7:0]” = FFh).

- UI [User interface] Image Mode (UI-Mode)

This mode is applied to optimize for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio is 10% or less. NT35510 provides flexible configuration for UI-Mode by setting the registers CABC_UI_PWM0[7:0] ~ CABC_UI_PWM3[7:0] to setting prefer brightness.

- Still Picture Mode (Still-Mode)

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. Ideal power consumption reduction ratio is more than 30%. The NT35510 will automatically estimate a better gamma setting and PWM duty based on different image contents, so the reduction ratio of the power consumption of backlight is not a constant ratio, this ratio will vary between 10% ~ 40% with different image contents.

- Moving Image Mode (Moving-Mode)

User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. Idea power consumption reduction ratio is more than 30%.

5.22.6 Ambient Light Sensor and Automatic Brightness Control (LABC)

The LABC function of NT35510, includes several function blocks and illustrated in below diagram.

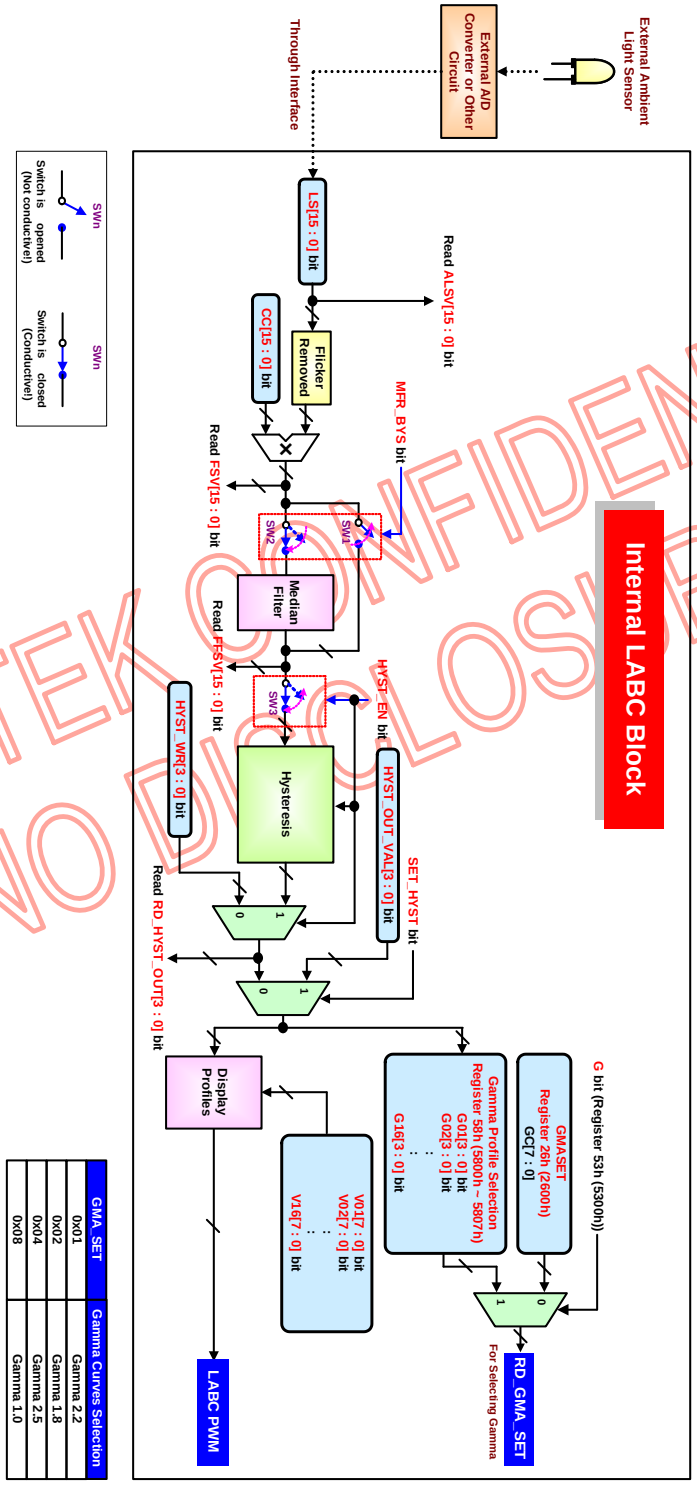
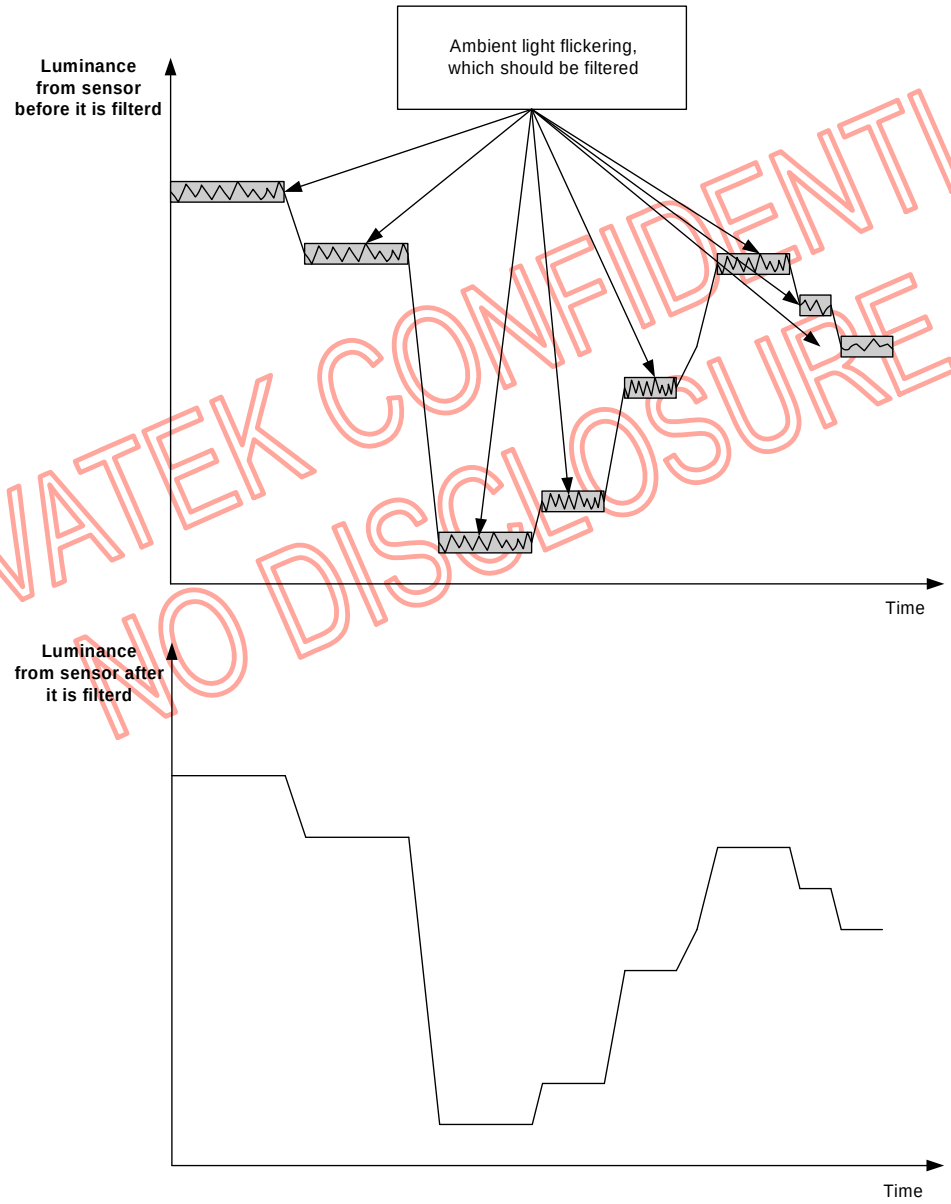


Fig. 5.22.9 LABC Architecture

5.22.6.1 50/60HZ FLICKER REMOVAL

Ambient Light from Front Side is measuring white spectrum. These measured values are used as an input for “50/60 Hz flicker removal” block. “50/60 Hz flicker removal” block converts sensor values from analog to a digital if needed. Same block is for filtering external light source flicker (e.g. 50Hz and 60 Hz), which maybe present in ambient light source measurements. This functionality is possible to implement with e.g. an averaging filter, 10 samples with 220Hz sampling frequency. These samples are pipelined so that the oldest value is dropped out when a new value is entered (First In- First Out queue). Sampling of ambient light is started after receiving “Write CTRL Display (5300h)” command with applicable parameters. First averaged value is outputted for 500ms. It is copied to all registers for median filter.

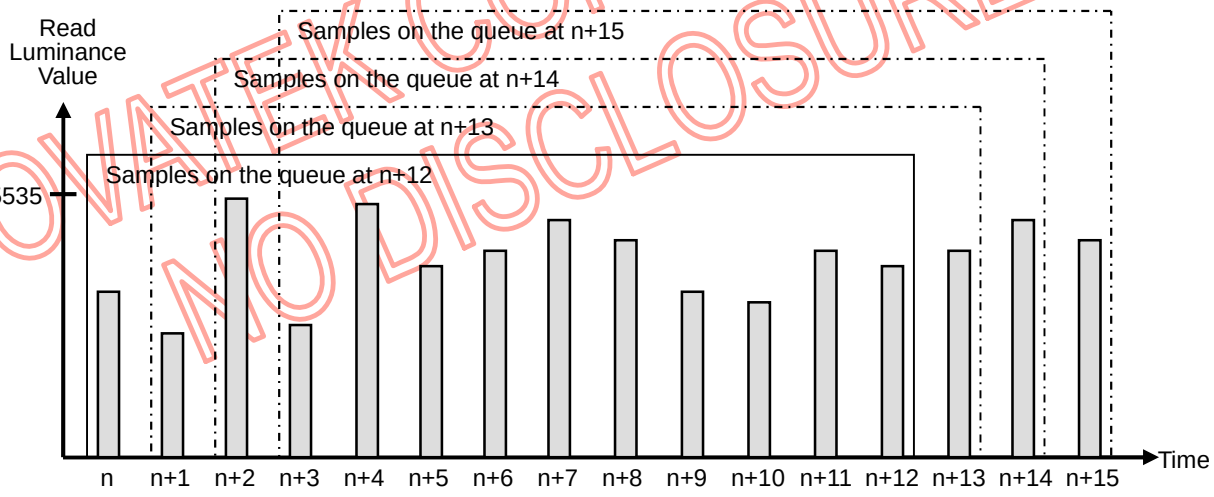


5.22.6.2 LIGHT GUIDE COMPENSATION

Filtered luminance value is inputted into “Apply calibration and light guide compensation” block. “Apply calibration and light guide compensation” block is to calibrate measured luminance and to compensate variation of light guide which is covered on the ambient light sensor. Compensated luminance value can be read by the user (16 bit value, see chapters: “Read MSBs of FSV Value (5A00h)” and Read LSBs of FSV Value (5B00h)” without a delay at any time. This doesn’t apply 120ms for SW / HW reset wait time and 500 ms for activated Ambient light sensing with “Write CTRL Display (5300h)” command after power on sequence. First measurement is started after the command. This means that display module must apply flicker removal, calibration and compensation into measured values within 500 ms after the activation. 500ms is the maximum sampling time of the ambient light (the same meaning as median filter input). Output is applied flicker removal, calibration and compensation.

5.22.6.3 MEDIAN FILTER

Filtered luminance value is inputted into “Apply calibration and light guide compensation” block. “Apply calibration and light guide compensation” block is to calibrate measured luminance and to compensate variation of light guide which is covered on the ambient light sensor. Compensated luminance value can be read by the user (16 bit value, see chapters: “Read MSBs of FSV Value (5A00h)” and Read LSBs of FSV Value (5B00h)” without a delay at any time. This doesn’t apply 120ms for SW / HW reset wait time and 500 ms for activated Ambient light sensing with “Write CTRL Display (5300h)” command after power on sequence. First measurement is started after the command. This means that display module must apply flicker removal, calibration and compensation into measured values within 500 ms after the activation. 500ms is the maximum sampling time of the ambient light (the same meaning as median filter input). Output is applied flicker removal, calibration and compensation.



Luminance values of this example are defined on the following table.

Time	Read Luminance Value (0 – 65535)	Time	Read Luminance Value (0 – 65535)
n	40960	n+8	53760
n+1	30720	n+9	40960
n+2	64000	n+10	38400
n+3	32768	n+11	51200
n+4	62720	n+12	47360
n+5	47360	n+13	51200
n+6	51200	n+14	58880
n+7	58880	n+15	53760

Queues (Read Luminance Values) of this example are defined below.

An Example: Read Queued Luminance Values													
Time / Queue	Values of Queue												
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th
n+6	40960	30720	64000	32768	62720	47360	51200	58880	53760	40960	38400	51200	47360
n+7	30720	64000	32768	62720	47360	51200	58880	53760	40960	38400	51200	47360	51200
n+8	64000	32768	62720	47360	51200	58880	53760	40960	38400	51200	47360	51200	58880
n+9	32768	62720	47360	51200	58880	53760	40960	38400	51200	47360	51200	58880	53760

The median filter will sort these values (Read Luminance Values) in ascending order. Sorted example values are as fellows.

An Example: Sorted Queued Luminance Values													
Time	Sorted Values in the Order of Magnitude												
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th
n+6	30720	32768	38400	40960	40960	47360	47360	51200	51200	53760	58880	62720	64000
n+7	30720	32768	38400	40960	47360	47360	51200	51200	51200	53760	58880	62720	64000
n+8	32768	38400	40960	47360	47360	51200	51200	51200	53760	58880	58880	62720	64000
n+9	32768	38400	40960	47360	47360	51200	51200	51200	53760	53760	58880	58880	62720

The median filter selects one of those values based on order of magnitude. Selected value is the 7th value (values highlighted on the table).

5.22.6.4 HYTERESIS

Hysteresis defines when to change between brightness values. Different values are used to define increment and decrement limits. The user can program these steps, see “Write Hysteresis (5700h)”, and “Write Profile Values for Display (5000h)”.

For each step number “n”, the following values are required:

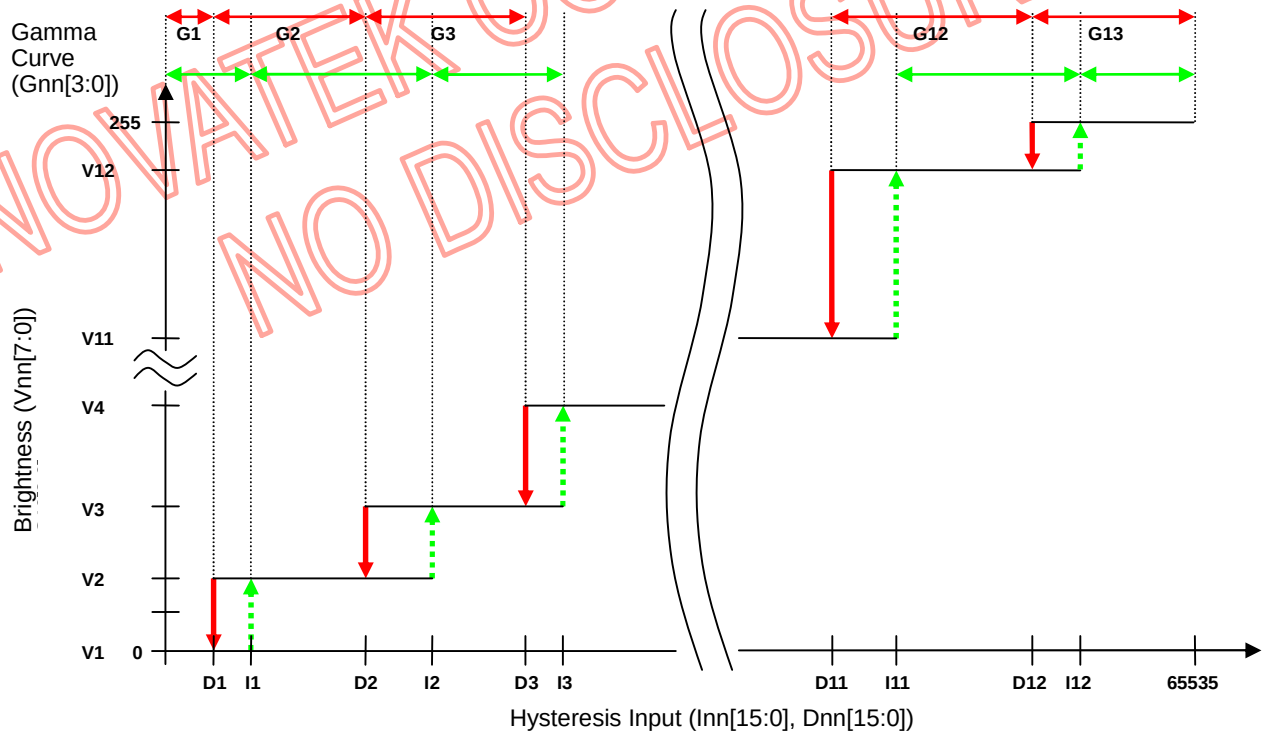
- An 8-bit value (Vnn[7:0]) which sets the display brightness.
- A 16-bit value (Inn[15:0]) “increment step” value.

  If the output value of the median filter is greater than the previous one, then the Inn values represent the transition from the step “n” to step “n + 1”.
- A 16-bit value (Dnn[15:0]) “decrement step” value.

  If the output value of the median filter is smaller than the previous one, then the Dnn values represent the transition from the step “n” to step “n + 1”.
- An 4-bit value (Gnn[3:0]) “gamma curve select” value.

  This uses 1-hot encoding to select which gamma curve will be used for each step.
- Maximum step number (n) is 16.

The bellow diagram shows a graph of hysteresis input value vs. display backlight output for an arbitrary hysteresis curve. For this graph, step 12 is before the last step in the current profile, and so doesn’t have any increment or decrement step values associated with it.



NOTE: For the last step both increment and decrement values are set to 65535 (FFFFh). E.g. D13 and I13 are set to 65535 (FFFFh) in the case of the below diagram.

This curve can be split into two separate cases, one for increasing input, and one for decreasing input. Once the hysteresis is known to be increasing or decreasing, the diagram shown in above can be separated into the two curves. Once the correct graph is chosen, it is relatively simple to go through each of the levels in turn, checking against the increment or decrement values as necessary. The following table is specified the relationship between each parameters and step number using 6 steps (6 increment and 6 decrement) for hysteresis 6.

Example: Relationship between each parameters, steps and hysteresis.

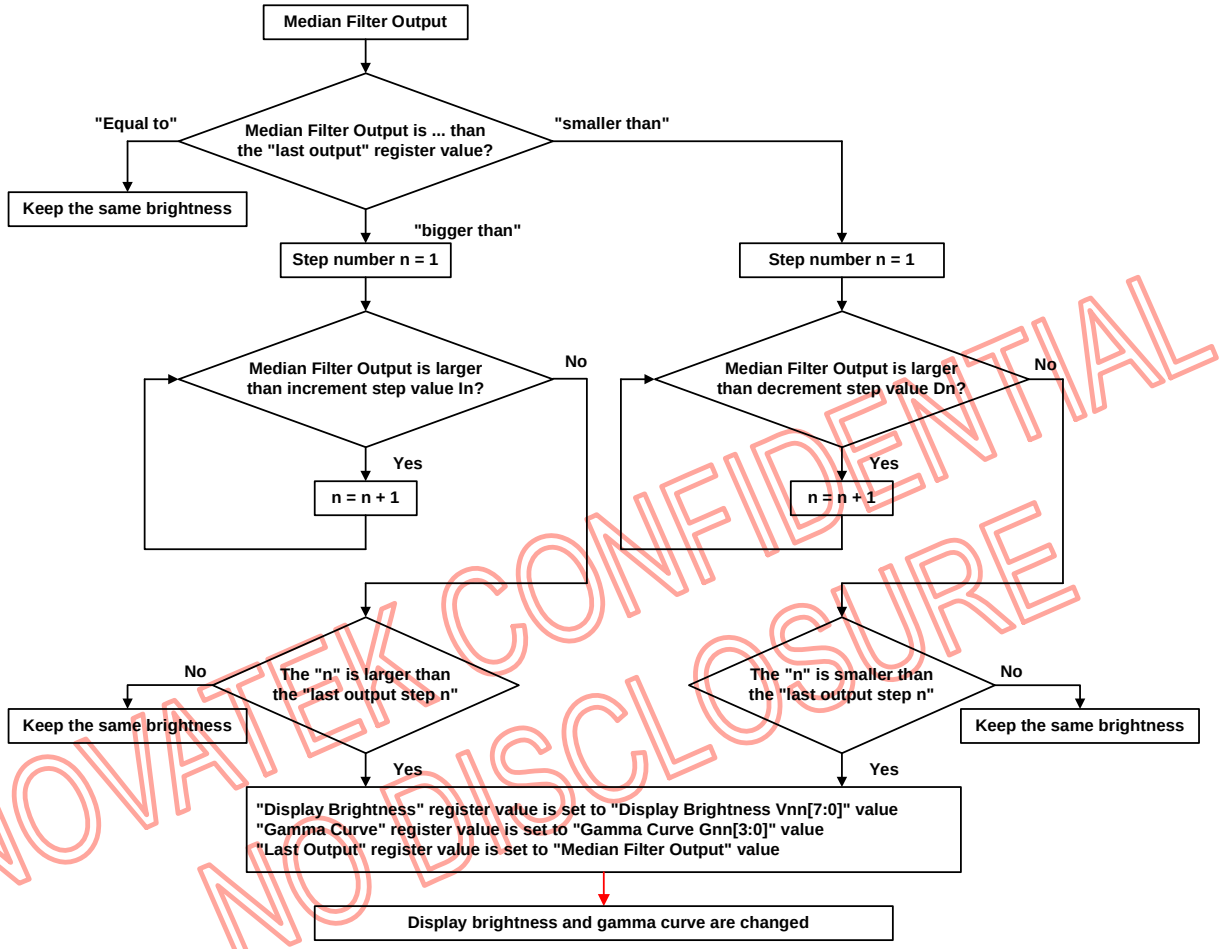
Step Number (n)	Increment Value (Inn)	Decrement Value (Dnn)	Display Brightness (Vnn)
1	3840 (F00h)	2560 (A00h)	20 (14h)
2	16896 (4200h)	14336 (3800h)	40 (28h)
3	25600 (6400h)	20480 (5000h)	80 (50h)
4	35840 (8C00h)	33280 (8200h)	130 (82h)
5	48896 (BF00h)	43776 (AB00h)	200 (C8h)
6	65535 (FFFFh)	65535 (FFFFh)	0
7	x	x	x
8	x	x	x
9	x	x	x
10	x	x	x
11	x	x	x
12	x	x	x
13	x	x	x
14	x	x	x
15	x	x	x
16	x	x	x

Step number of increment-value and decrement-value is 16 steps.

Don’t care about the parameter values after “65535 (FFFFh)” of increment value and decrement value, e.g. “x” in the above table. The 16th increment and decrement values are always set to “65535 (FFFFh)” internally, if increment and decrement values before 16th parameters are less than “65535 (FFFFh)”.

Once the hysteresis curve has been stored using the commands above, the flowchart is used to select the correct hysteresis level after getting median filter output as a reference. Supplier can decide the sequence.

Once the hysteresis curve has been stored using the commands above, the flowchart is used to select the correct hysteresis level after getting median filter output as a reference. Supplier can decide the sequence.



5.23 Column, 1-Dot, 2-Dot, 3-Dot and 4-Dot Inversion (VCOM DC Drive)

The NT35510, in addition to the frame-inversion liquid crystal drive, supports the column, 1–dot, 2-dot, 3-dot and 4-dot inversion driving methods to invert the polarity of liquid crystal. The column, 1–dot, 2-dot, 3-dot and 4-dot inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

6 COMMAND DESCRIPTIONS

6.1 User Command Set

Table 6.1.1 User Command Set

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Dir	W	00h	0000h	No Argument (0000h in MDDI I/F)									No Operation
SWRESET	Cnd1	W	01h	0100h	No Argument (0000h in MDDI I/F)									Software reset
RDDID	Dir	R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
				0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
				0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
RDNUMPE	Dir	R	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Errors on DSI only
RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode
RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTR
RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Pixel Format
RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode
RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Signal Mode
RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result
SLPIN	DVS	W	10h	1000h	No Argument (0000h in MDDI I/F)									Sleep in & booster off
SLPOUT	Dir	W	11h	1100h	No Argument (0000h in MDDI I/F)									Sleep out & booster on
PTLON	DVS	W	12h	1200h	No Argument (0000h in MDDI I/F)									Partial mode on
NORON	DVS	W	13h	1300h	No Argument (0000h in MDDI I/F)									Partial off (Normal)
INVOFF	DVS	W	20h	2000h	No Argument (0000h in MDDI I/F)									Display inversion off (normal)
INVON	DVS	W	21h	2100h	No Argument (0000h in MDDI I/F)									Display inversion on
ALLPOFF	DVS	W	22h	2200h	No Argument (0000h in MDDI I/F)									All pixel off (black)
ALLPON	DVS	W	23h	2300h	No Argument (0000h in MDDI I/F)									All pixel on (white)
GAMSET	DVS	W	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select
DISPOFF	DVS	W	28h	2800h	No Argument (0000h in MDDI I/F)									Display off
DISPON	DVS	W	29h	2900h	No Argument (0000h in MDDI I/F)									Display on
CASET	Dir	W	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Column address set XS[15:0]: column start address XE[15:0]: column end address
				2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
				2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
				2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
RASET	Dir	W	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Row address set YS[15:0]: row start address YE[15:0]: row end address
				2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
				2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
				2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
RAMWR	Dir	W	2Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0	Memory write
RAMRD	Dir	R	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read
PTLAR	DVS	W	30h	3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	Partial start/end address set PSL[15:0]: partial start address PEL[15:0]: partial end address
				3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
				3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
				3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
TEOFF	DVS	W	34h	3400h	No Argument (0000h in MDDI I/F)									Tearing effect line off
TEON	DVS	W	35h	3500h	00h	-	-	-	-	-	-	-	M	Tearing effect mode set & on
MADCTL	Cnd2	W	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY	Memory data access control
IDMOFF	DVS	W	38h	3800h	No Argument (0000h in MDDI I/F)									Idle mode off
IDMON	DVS	W	39h	3900h	No Argument (0000h in MDDI I/F)									Idle mode on

Table 6.1.1 User Command Set (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	Dir	W	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format
RAMWRC	Dir	W	3Ch	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory write Continue
RAMRDC	Dir	R	3Eh	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read Continue
STESL	DVS	W	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line
				4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
GSL	Dir	R	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line
				4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
DSTBON	DVS	W	4Fh	4F00h	00h	0	0	0	0	0	0	0	DSTB	Deep standby mode on
WRPFD	DVS	W	50h	5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010	Write profile value for display
				5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020	
				:	:	:	:	:	:	:	:	:	:	
				500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150	
				500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160	
WRDISBV	DVS	W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value
WRCTRLD	DVS	W	53h	5300h	00h	0	0	BCTRL	A	DD	BL	DB	G	Write control display
RDCTRLD	Dir	R	54h	5400h	00h	0	0	BCTRL	A	DD	BL	DB	G	Read control display value
WRCABC	DVS	W	55h	5500h	00h	0	0	0	0	0	0	C1	C0	Write CABC mode
RDCABC	Dir	R	56h	5600h	00h	0	0	0	0	0	0	C1	C0	Read CABC mode
WRHYSTE	DVS	W	57h	5700h	00h	I017	I016	I015	I014	I013	I012	I011	I010	Write hysteresis
				5701h	00h	I027	I026	I025	I024	I023	I022	I021	I020	
				:	:	:	:	:	:	:	:	:	:	
				570Eh	00h	I157	I156	I155	I154	I153	I152	I151	I150	
				570Fh	00h	I167	I166	I165	I164	I163	I162	I161	I160	
				5710h	00h	D017	D016	D015	D014	D013	D012	D011	D010	
				5711h	00h	D027	D026	D025	D024	D023	D022	D021	D020	
				:	:	:	:	:	:	:	:	:	:	
				571Eh	00h	D157	D156	D155	D154	D153	D152	D151	D150	
				571Fh	00h	D167	D166	D165	D164	D163	D162	D161	D160	
WRGAMMSET	DVS	W	58h	5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010	Write gamma setting
				5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030	
				:	:	:	:	:	:	:	:	:	:	
				5806h	00h	G143	G142	G141	G140	G133	G132	G131	G130	
				5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150	
RDFSVM	Dir	R	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8	Read FS value MSBs
RDFSVL	Dir	R	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0	Read FS value LSBs
RDMFFSVM	Dir	R	5Ch	5C00h	00h	FFSV15	FFSV14	FFSV13	FFSV12	FFSV11	FFSV10	FFSV9	FFSV8	Read median filter FS value MSBs
RDMFFSVL	Dir	R	5Dh	5D00h	00h	FFSV7	FFSV6	FFSV5	FFSV4	FFSV3	FFSV2	FFSV1	FFSV0	Read median filter FS value LSBs
WRCABCMB	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness
RDCABCMB	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness

Table 6.1.1 User Command Set (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRLSCC	DVS	W	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Write light sensor compensation coefficient
				6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	
RDLSCCM	Dir	R	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Read LSCC value MSBs
RDLSCCL	Dir	R	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Read LSCC value LSBs
RDBWLB	Dir	R	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	Read Black/White low bit
RDBkx	Dir	R	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	Read Bkx
RDBky	Dir	R	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	Read Bky
RDWx	Dir	R	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
RDWy	Dir	R	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	Dir	R	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green low bit
RDRx	Dir	R	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	Dir	R	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	Dir	R	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	Dir	R	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	Dir	R	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Read Blue/AColor low bit
RDBx	Dir	R	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	Dir	R	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2	Read By
RDAx	Dir	R	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	Dir	R	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	Read Ay
RDDDBS	Dir	R	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB start
				A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
				A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A104h	00h	1	1	1	1	1	1	1	1	
RDDDBC	Dir	R	A8h	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB continue
				A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
				A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A804h	00h	1	1	1	1	1	1	1	1	
RDFCS	Dir	R	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	Read first checksum
RDCCS	Dir	R	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	Read continue checksum
RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:

1. The following description is indicates the executing time of instructions.

<table>
<tr><th>No.</th><th>Symbol</th><th>Executing Time</th></tr>
<tr><td>1</td><td>Dir (Direct)</td><td>At the received a completed instruction and parameter</td></tr>
<tr><td>2</td><td>DVS (Display Vertical Sync.)</td><td>Synchronized with the next frame</td></tr>
<tr><td>3</td><td>DHS (Display Horizontal Sync.)</td><td>Synchronized with the next line</td></tr>
<tr><td>4</td><td>Cnd1 (By Conditional 1)</td><td><table><tr><th>State</th><th>Executing time</th></tr><tr><td>When Sleep In</td><td>Dir</td></tr><tr><td>Other</td><td>DHS</td></tr></table></td></tr>
<tr><td>5</td><td>Cnd2 (By Conditional 2)</td><td><table><tr><th>State</th><th>Executing time</th></tr><tr><td>B7, B6, B5</td><td>Dir</td></tr><tr><td>B4, B3, B2, B1, B0</td><td>DVS</td></tr></table></td></tr>
</table>

2. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "5.6 DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32 (In case of other interfaces, parameters of command 2A00h~2A03h are stored on relative registers while command 2A00h~2A03h are executed completely and same for command 2B00h~2B03h, 3000h~3003h and 4000h~4001h).

3. When using the commands without parameter (No Argument) in MDDI interface, a dummy parameter must be followed after command address. For example, command SPLOUT can be executed as 0x11 only in MIPI, MPU and SPI interfaces but should be executed as 0x1100 + 0x0000 in MDDI interface.

NOP (0000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NOP	Write	00h	0000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write, RAM data read, RAM data write continue or RAM data read continue as described in RAMWR (Memory Write), RAMRD (Memory Read), RAMWRC (Memory Write Continue) and RAMRDC (Memory Read Continue) and parameter write commands.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	-

SWRESET: Software Reset (0100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SWRESET	Write	01h	0100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description)
The display is blank immediately.
Note: The Frame Memory content is kept or not by this command.

Restriction

It will be necessary to wait 5msec before sending new command following software reset.
The display module loads all display supplier's factory default values to the registers during this 5msec.
If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.
Software Reset command cannot be sent during Sleep Out sequence.

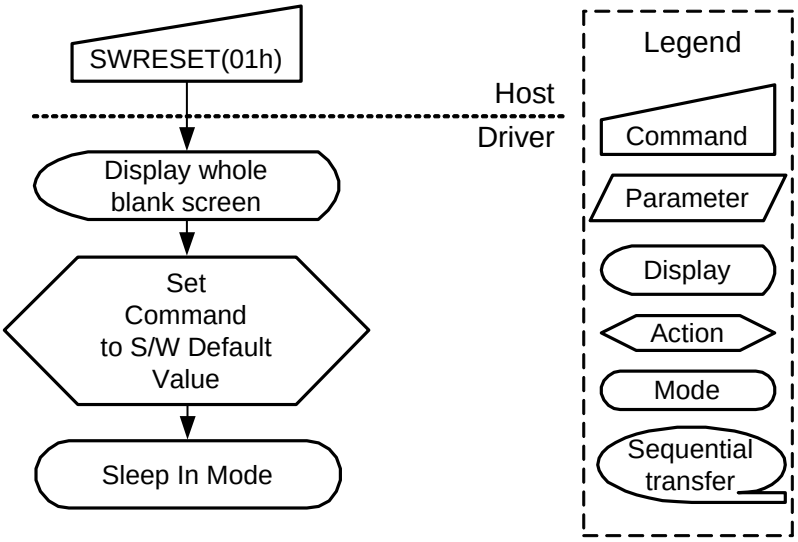
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



RDDID: Read Display ID (0400h~0402h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDID	Read	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
			0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
			0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

Description

This read byte returns 24-bit display identification information.
The 1st parameter (ID1): the module's manufacture ID.
The 2nd parameter (ID2): the module/driver version ID.
The 3rd parameter (ID3): the module/driver ID.
Note: Commands RDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameter 1, 2, 3 of the command 04h, respectively.

Restriction

-

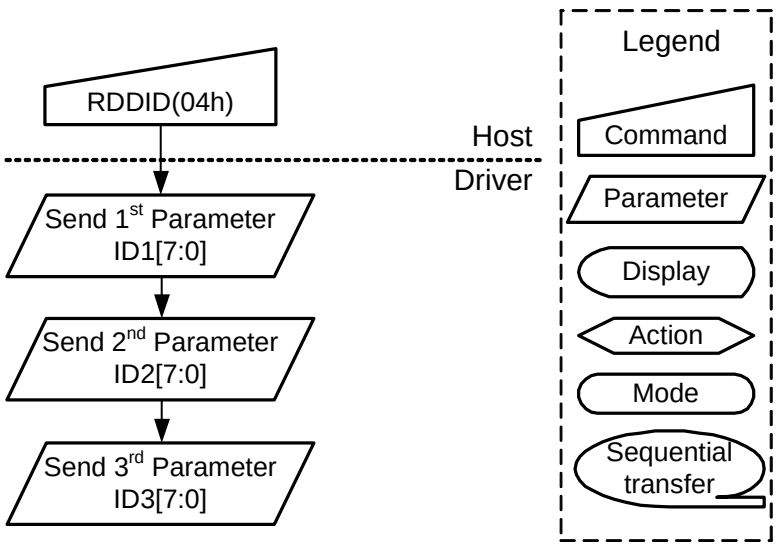
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Values	ID1=00h, ID2=80h, ID3=00h
S/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h
H/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h

Flow Chart



RDNUMED: Read Number of Errors on DSI (0500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDNUMED	Read	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0

NOTE: "-" Don't care

Description

The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.
P[6..0] bits are telling a number of the parity errors.
P[7] is set to "1" if there is overflow with P[6..0] bits.
P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed).
See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh.
This command is used for MIPI DSI only. It is no function for others interface operation.

Restriction

-

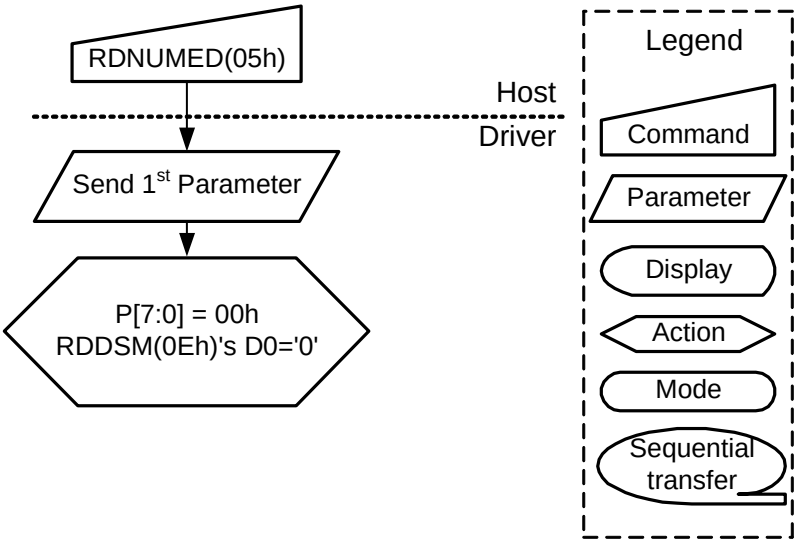
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDPM: Read Display Power Mode (0A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDPM	Read	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster On, "0"=Booster Off
D6	Idle Mode On/Off	"1"=Idle Mode On, "0"=Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out Mode, "0" = Sleep In Mode
D3	Display Normal Mode On/Off	"1" = Display Normal On, "0" = Display Normal Off
D2	Display On/Off	"1" = Display is On, "0" = Display is Off
D1	Not Defined	Set to "0" (not used)
D0	Not Defined	Set to "0" (not used)

Restriction

-

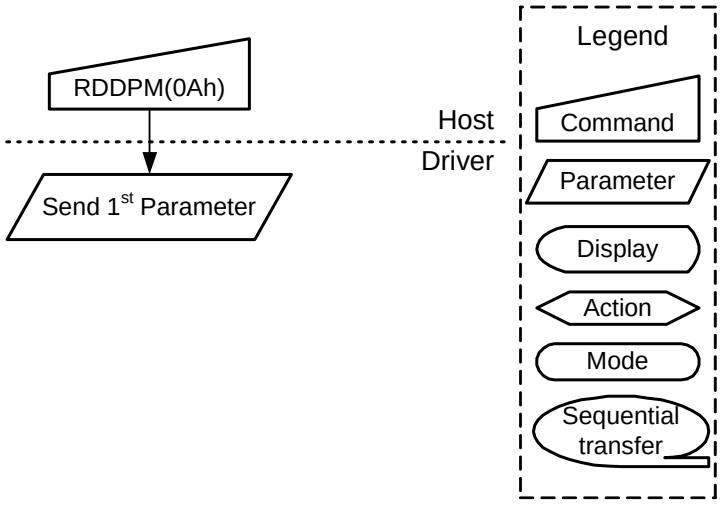
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



RDDMADCTL: Read Display MADCTL (0B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDMADCTL	Read	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order (MY)	"0" = Increment , "1" = Decrement
D6	Column Address Order (MX)	"0" = Increment , "1" = Decrement
D5	Row/Column Exchange (MV)	"0"= Normal , "1"= Row/column exchange
D4	Vertical refresh Order (ML)	"0" = Increment , "1" = Decrement
D3	RGB-BGR Order	"0" = RGB color sequence "1" = BGR color sequence
D2	Horizontal refresh Order (MH)	"0" = Increment , "1" = Decrement
D1	Flip horizontal (RSMX)	"0" = Normal , "1" = Horizontal flip
D0	Flip vertical (RSMY)	"0" = Normal , "1" = Vertical flip

Restriction

-

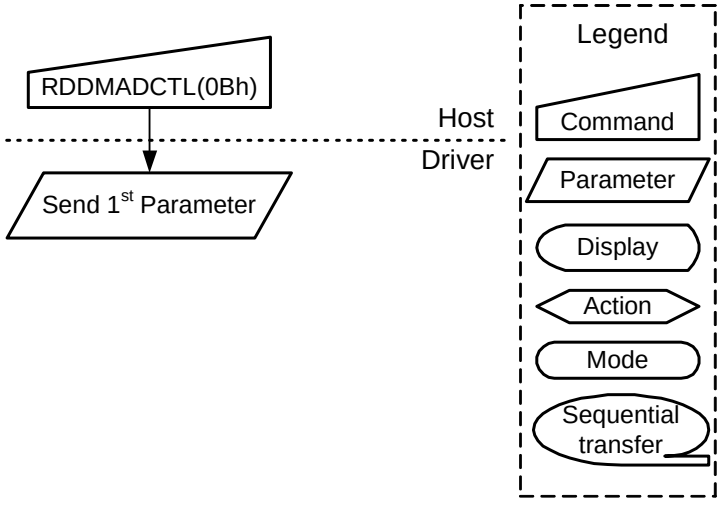
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDCOLMOD: Read Display Pixel Format (0C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDCOLMOD	Read	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Defined	Set to "0" (not used)
D6 ~ D4	RGB Interface Color Format	"101" = 16-bit / pixel "110" = 18-bit / pixel "111" = 24-bit / pixel
D3	Not Defined	Set to "0" (not used)
D2 ~ D0	Control Interface Color Format	"101" = 16-bit / pixel "110" = 18-bit / pixel "111" = 24-bit / pixel

Restriction

-

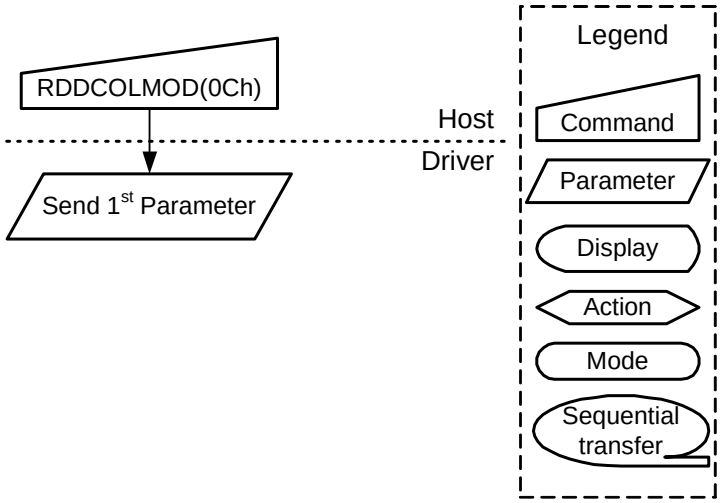
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



RDDIM: Read Display Image Mode (0D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDIM	Read	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	Set to "0" (not used)
D6	Horizontal Scrolling On/Off	Set to "0" (not used)
D5	Inversion On/Off	"1" = Inversion On, "0" = Inversion Off
D4	All Pixel On	"1" = White display, "0" = Normal display
D3	All Pixel Off	"1" = Black display, "0" = Normal display
D2 ~ D0	Gamma Curve Selection	"000" = GC0, "001" = GC1 "010" = GC2, "011" = GC3 "100" to "111" = not defined

Restriction

-

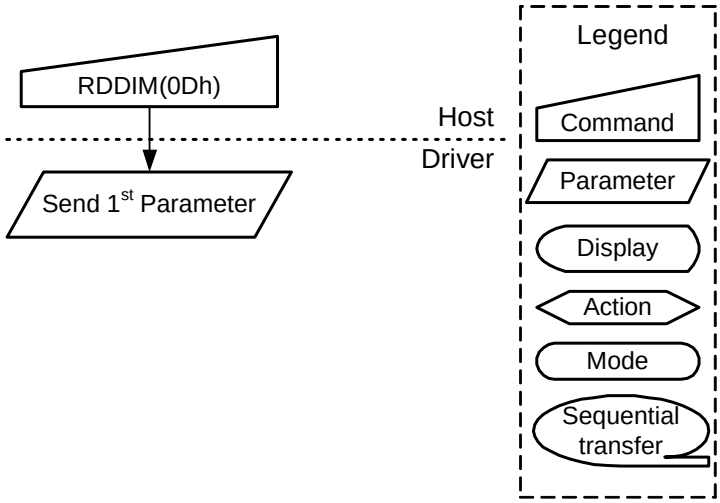
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDSM: Read Display Signal Mode (0E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDSM	Read	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing Effect Line Mode	"1" = Mode 2, "0" = Mode 1
D5	Horizontal Sync. (HS, RGB I/F)On/Off	"1" = HS bit is "1", "0" = HS bit is "0"
D4	Vertical Sync. (VS, RGB I/F)On/Off	"1" = VS bit is "1", "0" = VS bit is "0"
D3	Pixel Clock (PCLK, RGB I/F)On/Off	"1" = PCLK line is On, "0" = PCLK line is Off
D2	Data Enable (DE, RGB I/F)On/Off	"1" = DE bit is "1", "0" = DE bit is "0"
D1	Not Defined	Set to "0" (not used)
D0	Error on DSI	"1" = Error, "0" = No Error

Note: Bit D5 to D2 indicate current status of the lines when this command has been sent.

Restriction

-

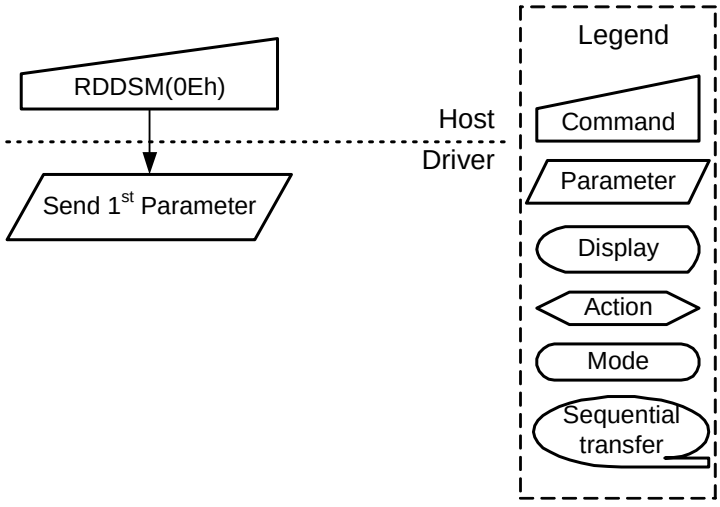
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDSDR: Read Display Self-Diagnostic Result (0F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDSDR	Read	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section 5.15
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Defined	Set to "0" (not used)
D2	Not Defined	Set to "0" (not used)
D1	Not Defined	Set to "0" (not used)
D0	Checksums Comparison	"0": Checksums are the same "1": Checksums are not the same

Restriction

-

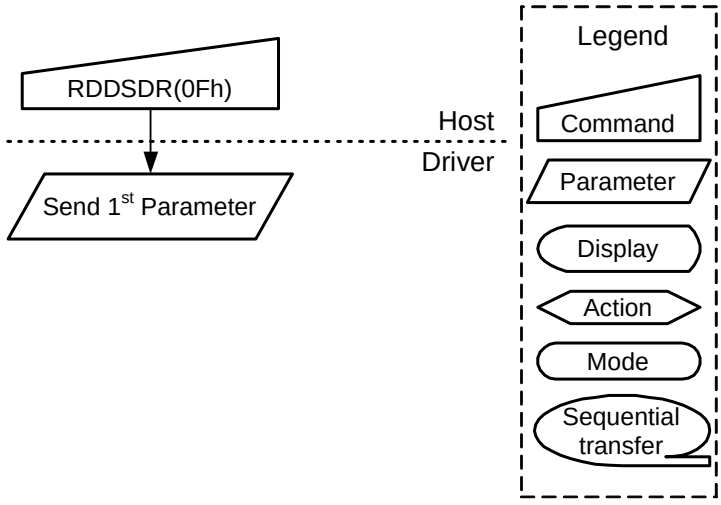
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



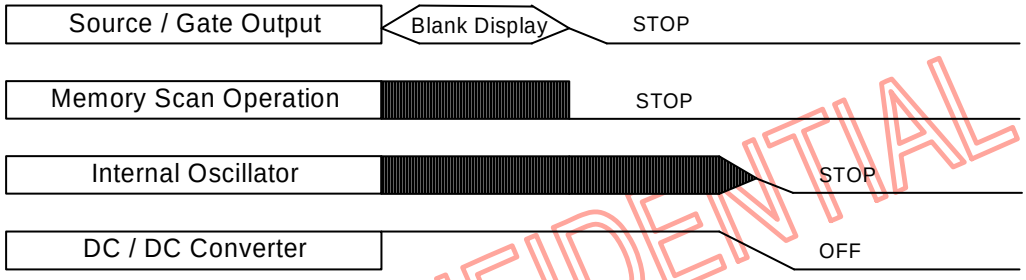
SLPIN: Sleep In (1000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	Write	10h	1000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command causes the TFT LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



Control Interface as will as memory and registers are still working and the memory keeps (RAMKP="1") or loses (RAMKP="0") its contents.
User can send PCLK, HS and VS information on RGB I/F for blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode.
Dimming function does not work when there is changing mode from Sleep Out to Sleep In.
There is used an internal oscillator for blank display.

Restriction

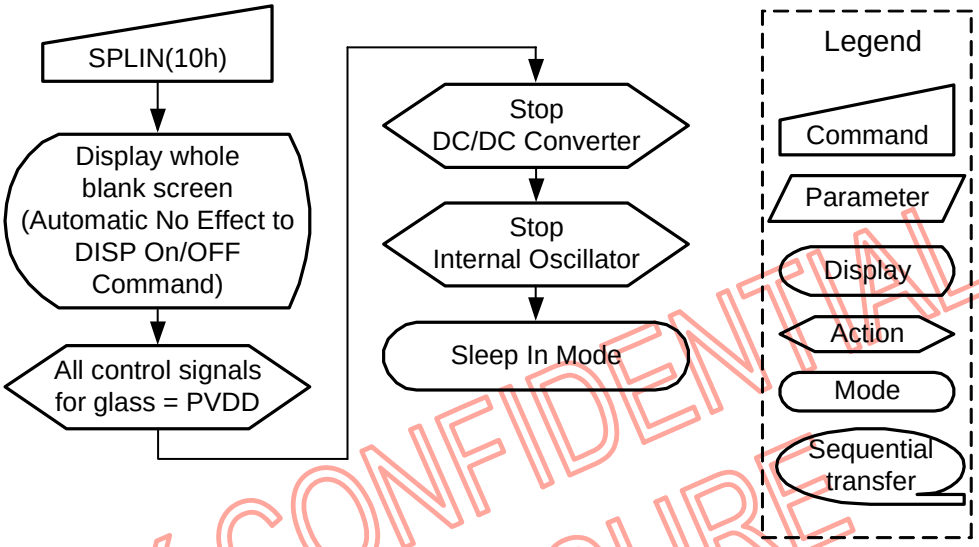
This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (0Ah) command D7. 

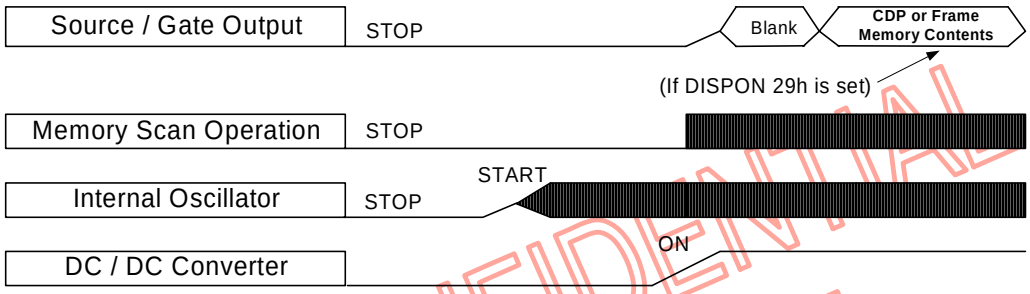
SLPOUT: Sleep Out (1100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	Write	11h	1100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



User can start to send PCLK, HS and VS information on RGB I/F before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In-mode to Sleep Out-mode in Normal Mode On.
There is used an internal oscillator for blank display.
NT35510 will do sequence control about gate control signals when sleep out.

Restriction

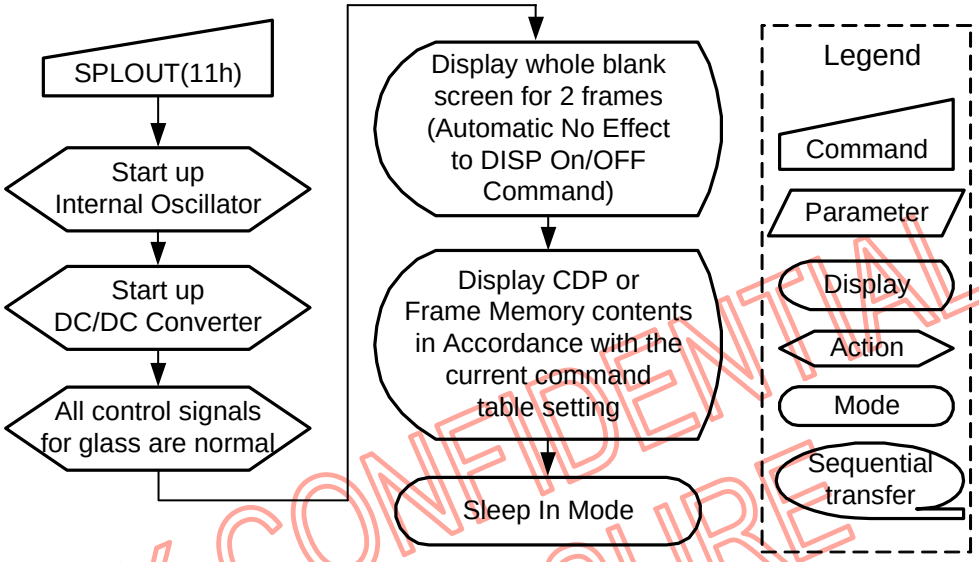
Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W reset command (01h) or H/W reset.
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
NT35510 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT35510 is already Sleep Out –mode.
NT35510 is doing self-diagnostic functions during this 5msec. See also section 5.15.
It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (0Ah) command D7. 

PTLON: Partial Display Mode On (1200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PTLON	Write	12h	1200h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On to Partial mode On.
Restriction	This command has no effect when Partial Display mode is active.
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Normal Mode On S/W Reset: Normal Mode On H/W Reset: Normal Mode On
Flow Chart	See Partial Area (30h)

NORON: Normal Display Mode On (1300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NORON	Write	13h	1300h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area Definition Descriptions for details of when to use this command

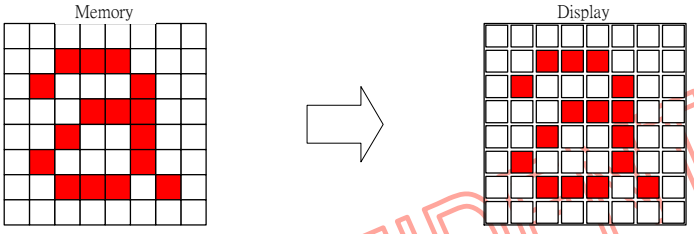
INVOFF: Display Inversion Off (2000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVOFF	Write	20h	2000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already in Inversion Off mode.

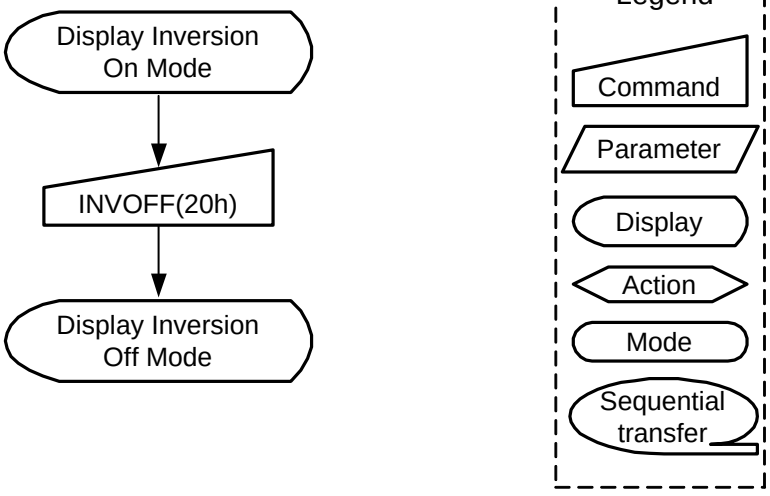
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



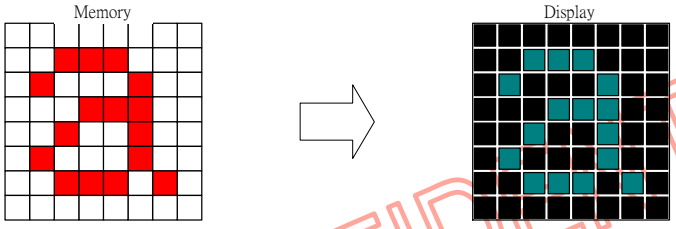
INVON: Display Inversion On (2100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVON	Write	21h	2100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to enter display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.
(Example)



Restriction

This command has no effect when module is already in Inversion On mode.

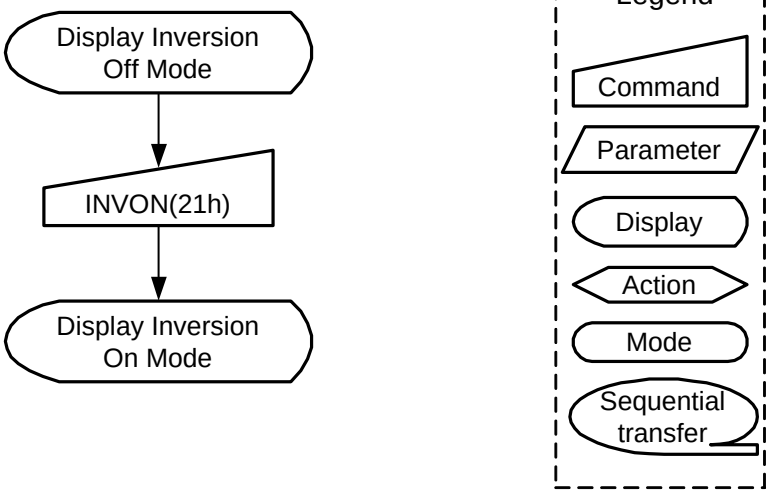
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



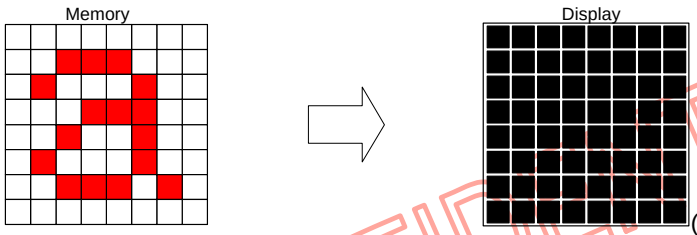
ALLPOFF: All Pixel Off (2200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	Write	22h	2200h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.
This command makes no change of contents of frame memory.
This command does not change any other status.



(Example)

"All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode.
The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.

Restriction

This command has no effect when module is already in All Pixel Off mode.

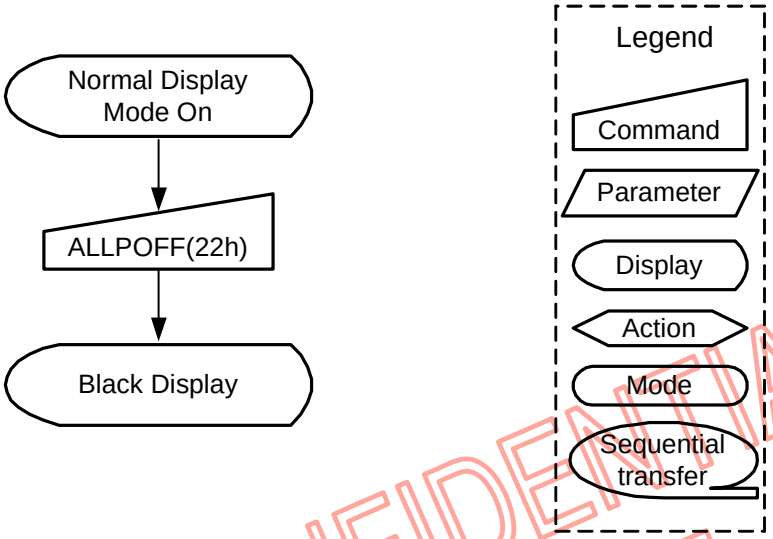
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

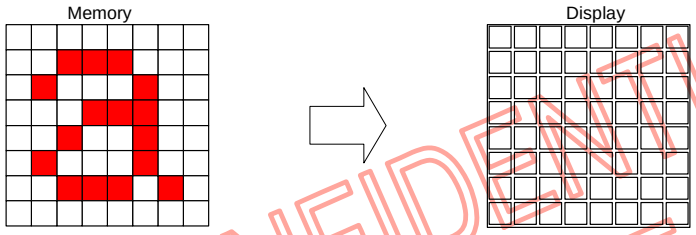
Flow Chart



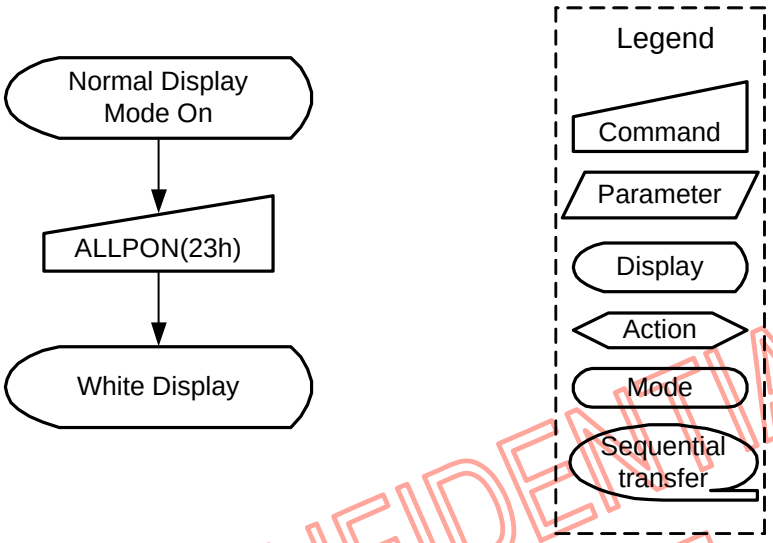
ALLPON: All Pixel On (2300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	Write	23h	2300h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example)  "All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.
Restriction	This command has no effect when module is already in all Pixel On mode.
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: All pixel off S/W Reset: All pixel off H/W Reset: All pixel off

Flow Chart



GAMSET: Gamma Set (2600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GAMSET	Write	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

NOTE: "-" Don't care

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G=2.2)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.

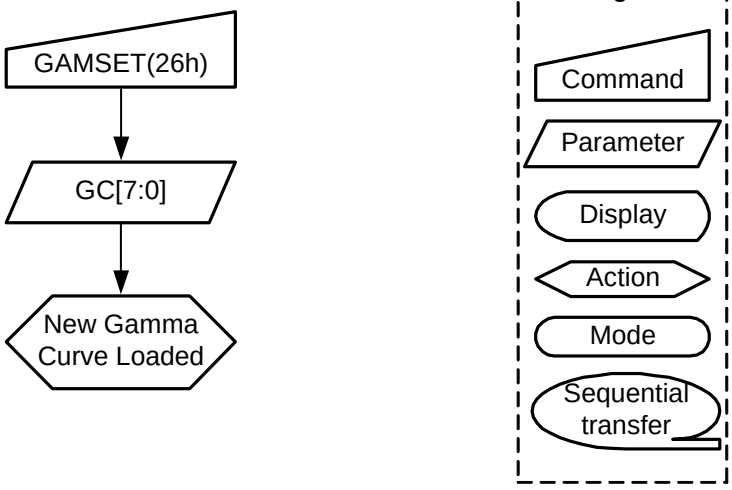
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



DISPOFF: Display Off (2800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	Write	28h	2800h	No Argument (0000h in MDDI I/F)								

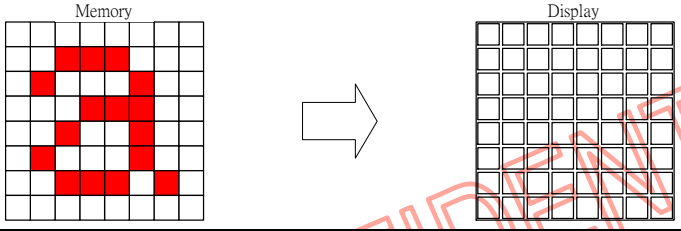
NOTE: "-" Don't care

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

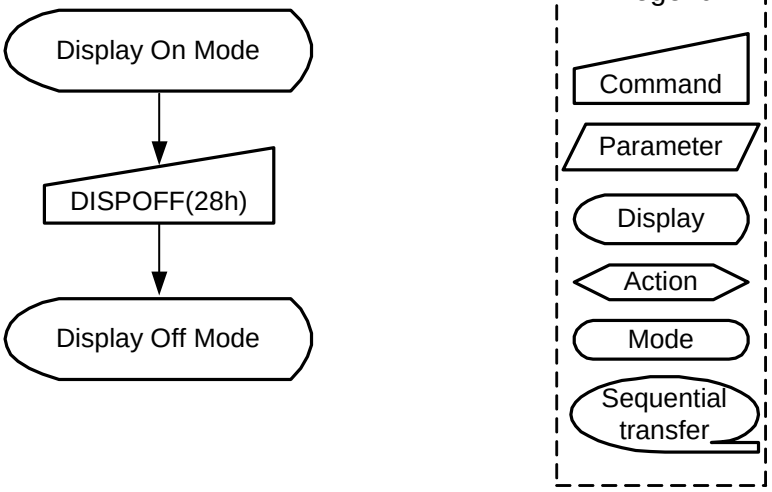
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



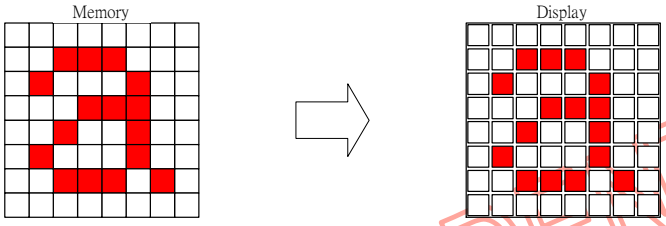
DISPON: Display On (2900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	Write	29h	2900h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to recover from DISPLAY OFF mode. Output from Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already in Display On mode.

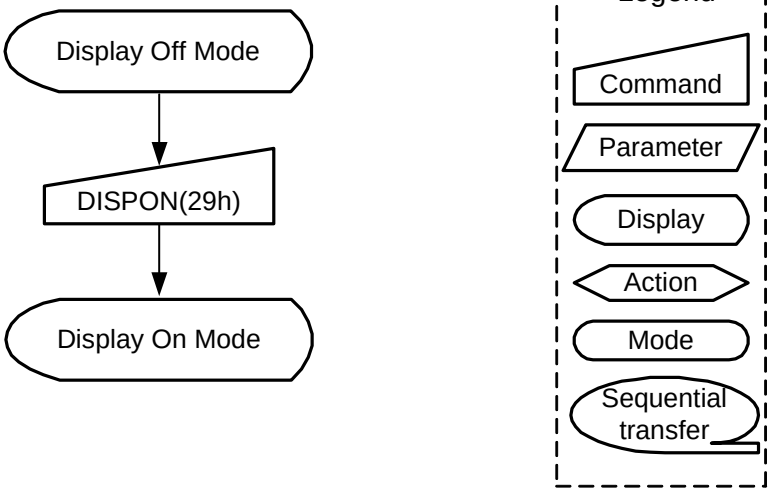
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



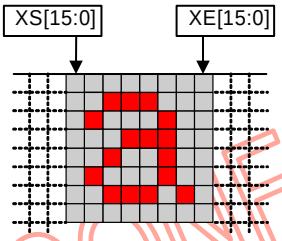
CASET: Column Address Set (2A00h~2A03h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
CASET	Write	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8
			2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
			2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8
			2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0

NOTE: "-" Don't care

Description

This command is used to define area of frame memory where MPU can access.
This command makes no change on the other driver status.
Each value represents one column line in the Frame Memory.
(Example)



Restriction

XS[15:0] always must be equal to or less than XE[15:0]
When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be ignored.
For CGM[7:0] = "70h" (480 x 864 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 863 (035Fh)
For CGM[7:0] = "6Bh" (480 x 854 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 853 (0355h)
For CGM[7:0] = "50h" (480 x 800 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 799 (031Fh)
For CGM[7:0] = "28h" (480 x 720 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 719 (02CFh)
For CGM[7:0] = "00h" (480 x 640 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 639 (027Fh)

Register Availability

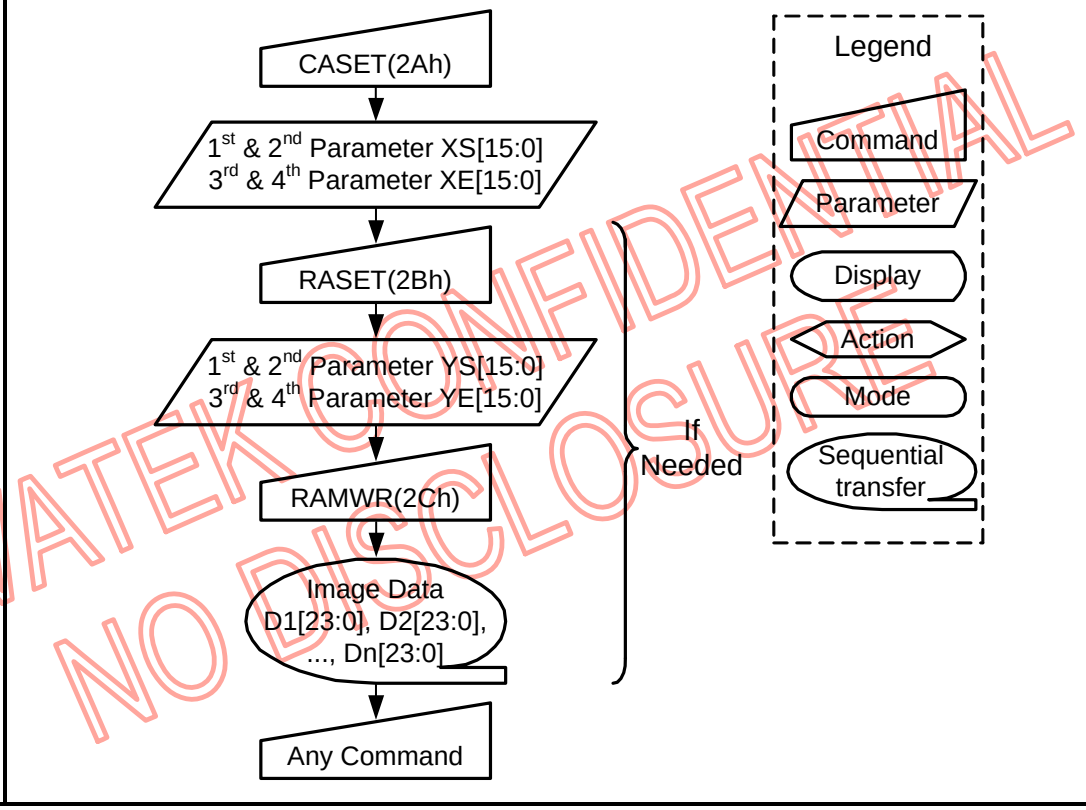
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For CGM[7:0] = “70h”, “6Bh”, “50h”, “28h”, “00h” , “FEh” (480x864/854/800/720/640 resolution)

Status	Default Value	
	XS[15:0]	XE[15:0]
Power On Sequence	0000h	01DFh (479d)
S/W Reset	0000h	01DFh (479d)
H/W Reset	0000h	01DFh (479d)

Flow Chart



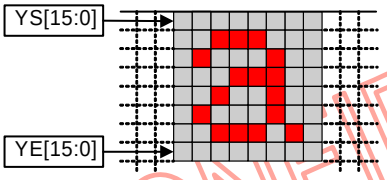
RASET: Row Address Set (2B00h~2B03h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RASET	Write	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8
			2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
			2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8
			2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0

NOTE: "-" Don't care

Description

This command is used to define area of frame memory where MPU can access.
This command makes no change on the other driver status.
Each value represents one column line in the Frame Memory.
(Example)



Restriction

YS[15:0] always must be equal to or less than YE[15:0]
When YS[15:0] or YE[15:0] is greater than maximum address like below, data of out of range will be ignored.
For CGM[7:0] = "70h" (480 x 864 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 863 (035Fh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
For CGM[7:0] = "6Bh" (480 x 854 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 853 (0355h)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
For CGM[7:0] = "50h" (480 x 800 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 799 (031Fh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
For CGM[7:0] = "28h" (480 x 720 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 719 (02CFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
For CGM[7:0] = "00h" (480 x 640 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 639 (027Fh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)

Register Availability

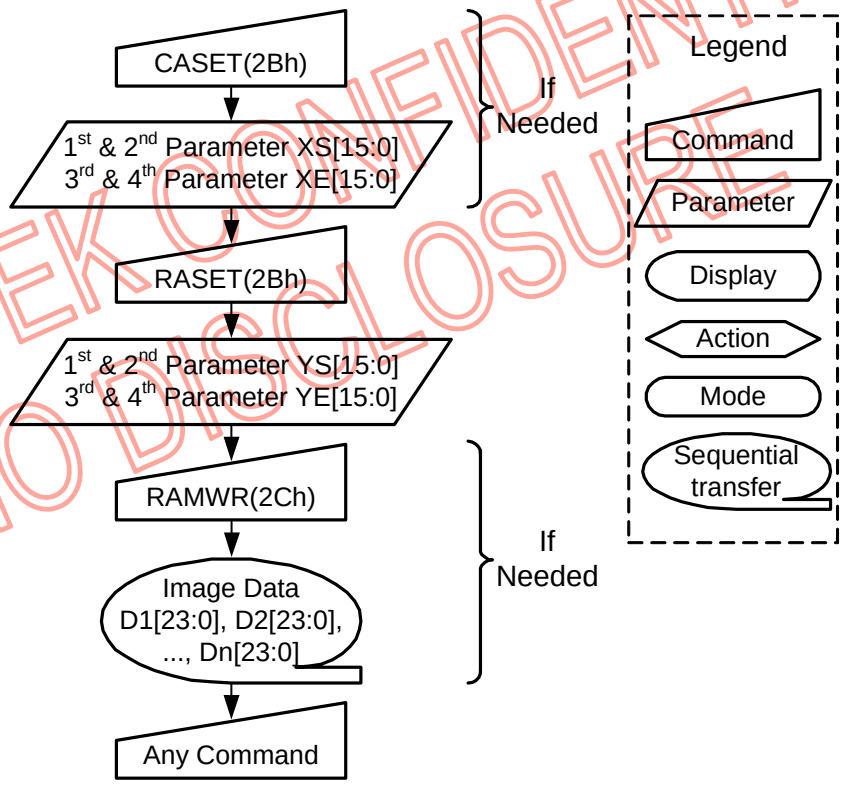
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For CGM[7:0] = “70h”, “6Bh”, “50h”, “28h”, “00h” , “FEh” (480x864/854/800/720/640 resolution)

Status	Default Value	
	YS[15:0]	YE[15:0]
Power On Sequence	0000h	035Fh (863d)
S/W Reset	0000h	035Fh (863d) if CGM[7:0]=”70h” 0355h (853d) if CGM[7:0]=”6Bh” 031Fh (799d) if CGM[7:0]=”50h” 02CFh (719d) if CGM[7:0]=”28h” 027Fh (639d) if CGM[7:0]=”00h” 0167h (359d) if CGM[7:0]=”FEh”
H/W Reset	0000h	035Fh (863d)

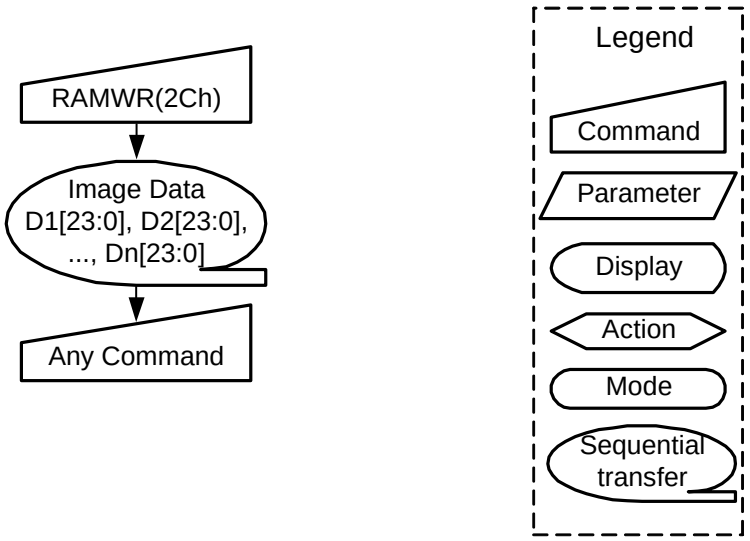
Flow Chart



RAMWR: Memory Write (2C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWR	Write	2Ch	2C00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command is used to transfer data from MPU interface to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTL setting Then D[23:0] is stored in frame memory and the column register and the row register incremented. Sending any other command can stop Frame Write.
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / Contents of memory is set randomly S/W Reset / Contents of memory is set randomly H/W Reset / Contents of memory is set randomly
Flow Chart	

RAMRD: Memory Read (2E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	Read	2Eh	2E00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

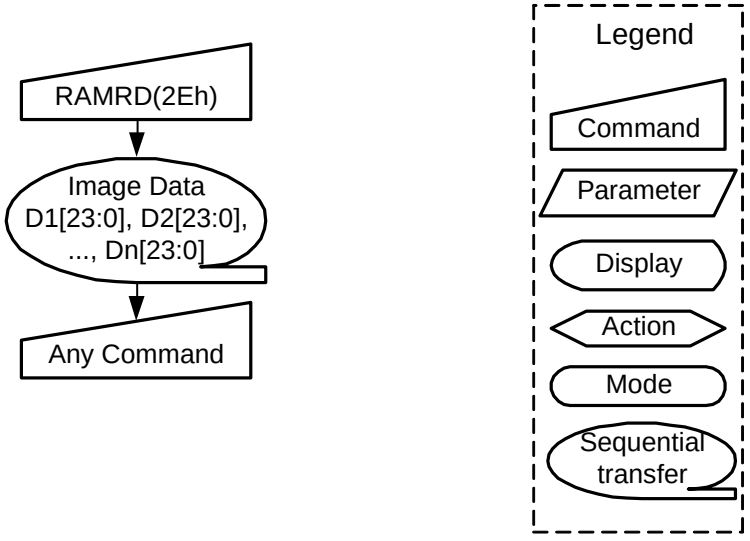
Description	This command is used to transfer data from frame memory to MPU interface. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D[23:0] is read back from the frame memory and the column register and the row register incremented Frame Read can be canceled by sending any other command.
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



PTLAR: Partial Area (3000h~3003h)

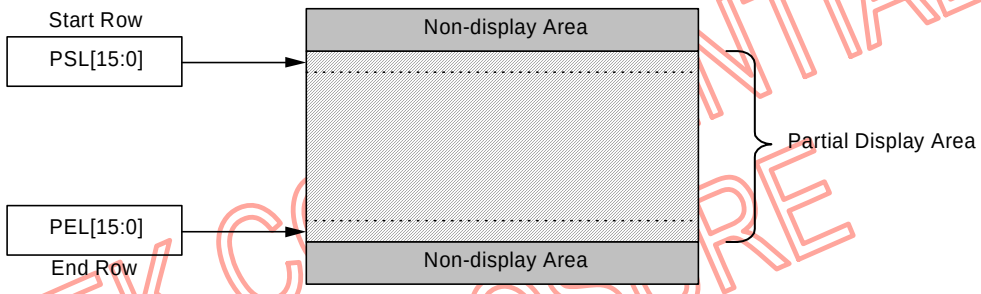
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PTLAR	Write	30h	3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8
			3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
			3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8
			3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0

NOTE: "-" Don't care

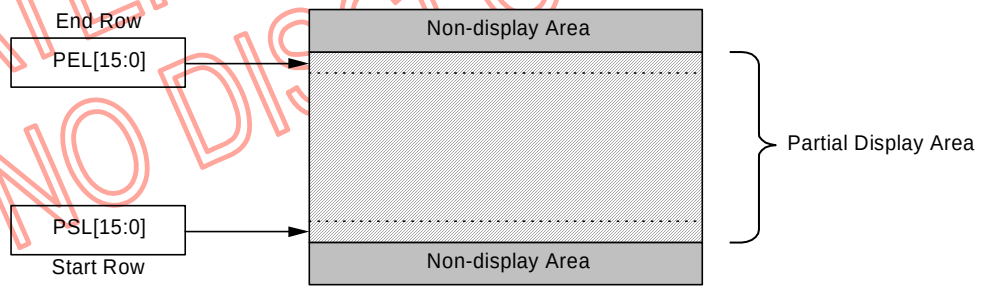
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

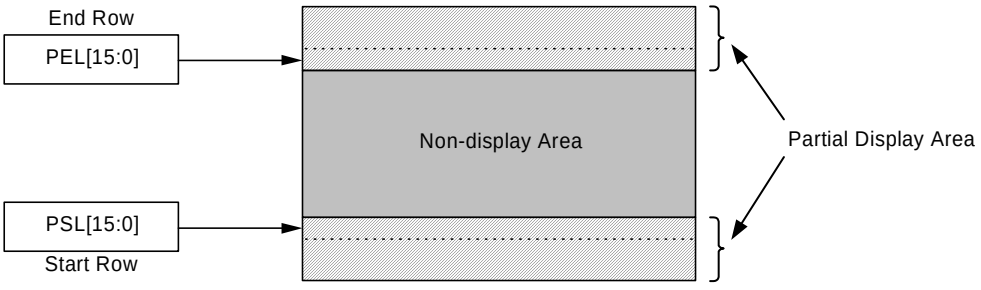
If End Row > Start Row when MADCTL ML=0:



If End Row > Start Row when MADCTL ML=1:



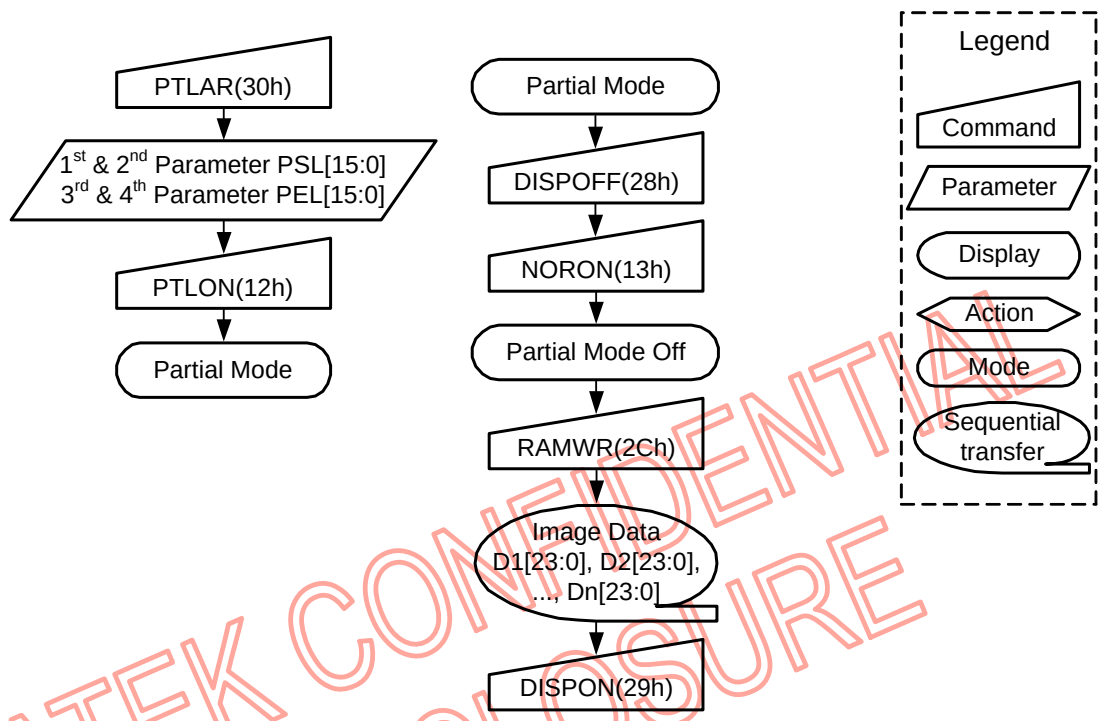
If End Row < Start Row when MADCTL ML=0:



If End Row = Start Row then the Partial Area will be one row deep.

<table>
<tr><td>Restriction</td><td>PSL[15:0] and PEL[15:0] should have below range
CGM[7:0] = ”70h” (480 x 864): 0 ≦ PSL[15:0], PEL[15:0] ≦ 863 (035Fh), |PEL–PSL| ≦ 863 (035Fh)
CGM[7:0] = ”6Bh” (480 x 854): 0 ≦ PSL[15:0], PEL[15:0] ≦ 853 (0355h), |PEL–PSL| ≦ 853 (0355h)
CGM[7:0] = ”50h” (480 x 800): 0 ≦ PSL[15:0], PEL[15:0] ≦ 799 (031Fh), |PEL–PSL| ≦ 799 (031Fh)
CGM[7:0] = ”28h” (480 x 720): 0 ≦ PSL[15:0], PEL[15:0] ≦ 719 (02CFh), |PEL–PSL| ≦ 719 (02CFh)
CGM[7:0] = ”00h” (480 x 640): 0 ≦ PSL[15:0], PEL[15:0] ≦ 639 (027Fh), |PEL–PSL| ≦ 639 (027Fh)</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PSL[15:0]</th><th>PEL[15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
</table>
</td></tr>
</table>

Flow Chart



TEOFF: Tearing Effect Line OFF (3400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
TEOFF	Write	34h	3400h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

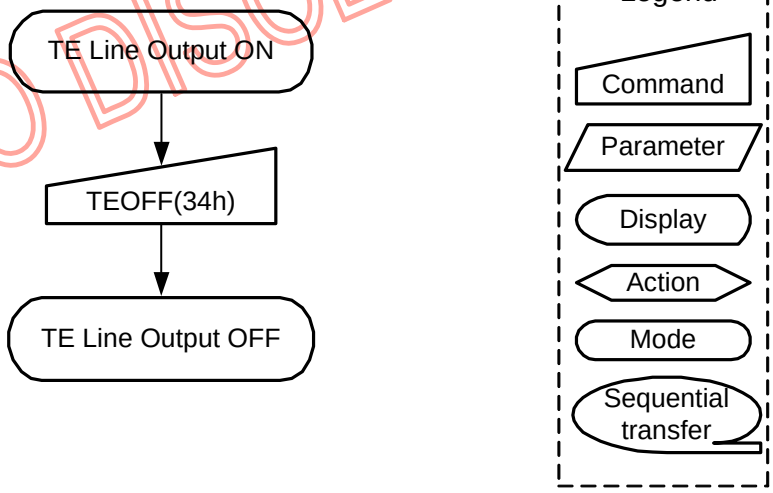
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



TEON: Tearing Effect Line ON (3500h)

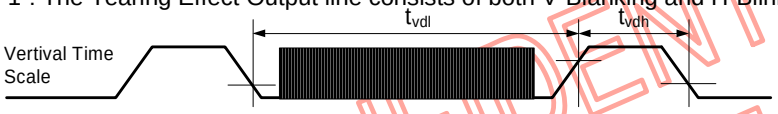
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	M

NOTE: "-" Don't care

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-" = Don't Care).
When M = "0": The Tearing Effect Output line consists of V-Blanking information only.

When M = "1": The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Lofw.

Restriction

This command has no effect when Tearing Effect output is already ON.

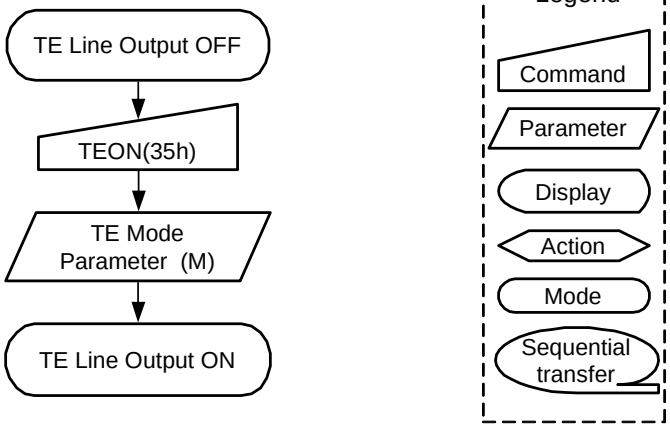
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



MADCTL: Memory Data Access Control (3600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	Write	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY

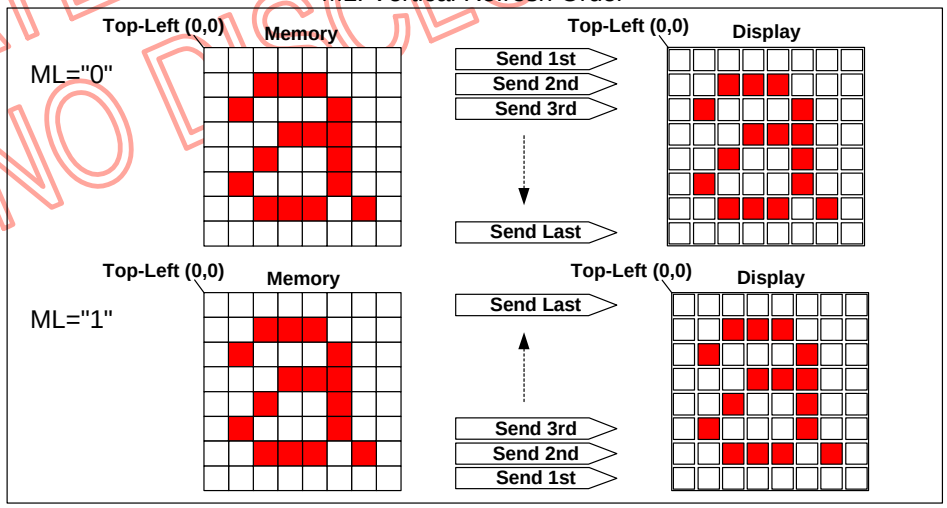
NOTE: "-" Don't care

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

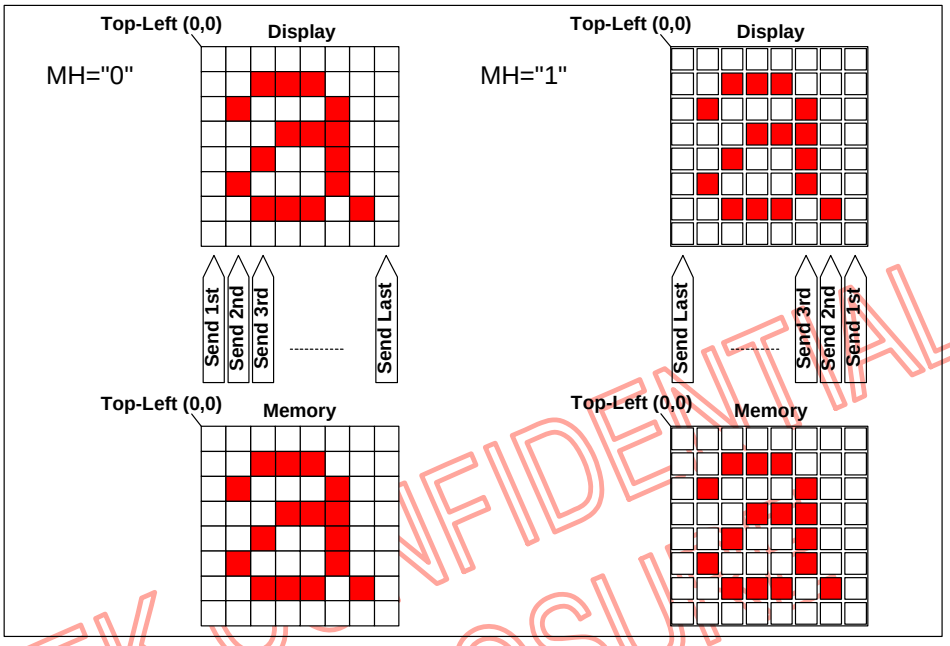
Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3 bits controls interface to memory write/read direction. The behavior on display after pattern changed.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	TFT LCD Vertical refresh direction control. Immediately behavior on display.
RGB	RGB-BGR Order	Color selector switch control "0" = RGB color sequence, "1" = BGR color sequence Immediately behavior on display
MH	Horizontal Refresh Order	TFT LCD Horizontal refresh direction control Immediately behavior on display.
RSMX	Flip Horizontal	Flips the display image left to right. Immediately behavior on display.
RSMY	Flip Vertical	Flips the display image top to down. Immediately behavior on display.

ML: Vertical Refresh Order



Description

MH: Horizontal Refresh Order



Restriction

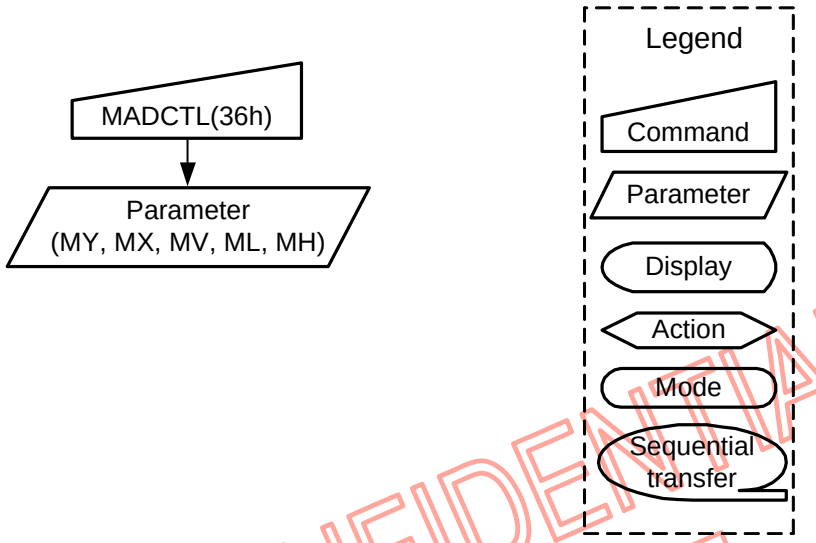
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

IDMOFF: Idle Mode Off (3800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	Write	38h	3800h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is used to recover from Idle mode on In the idle off mode, display panel can display maximum 16.7M colors.
Restriction	This command has no effect when module is already in Idle Off mode.

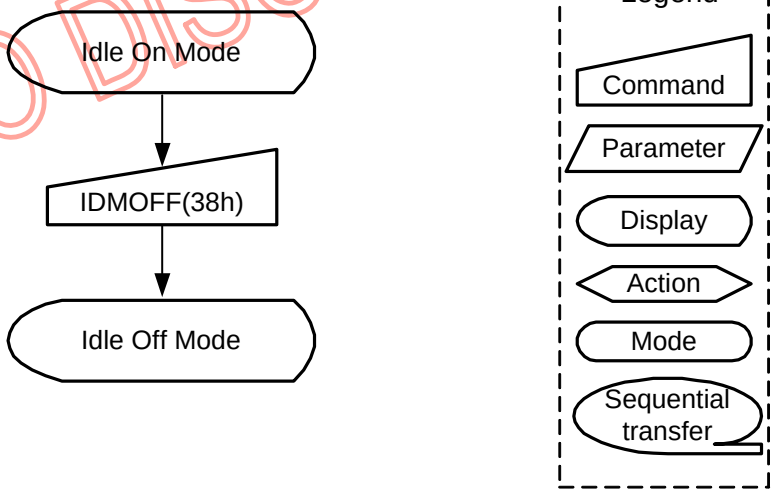
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart



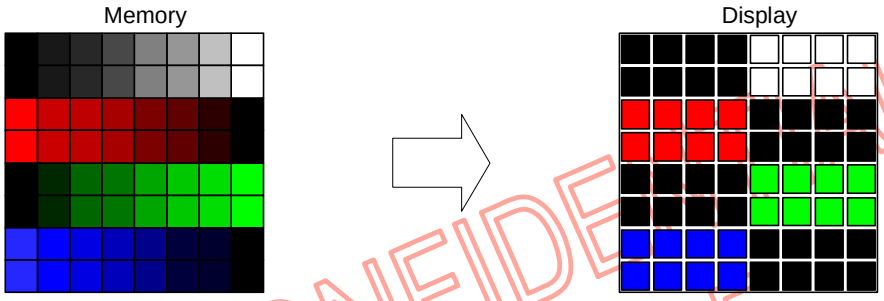
IDMON: Idle Mode On (3900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMON	Write	39h	3900h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Colors			
	$R_7R_6R_5R_4R_3R_2R_1R_0$	$R_7G_6G_5G_4G_3G_2G_1G_0$	$B_7B_6B_5B_4B_3B_2B_1B_0$
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Restriction

This command has no effect when module is already in Idle On mode

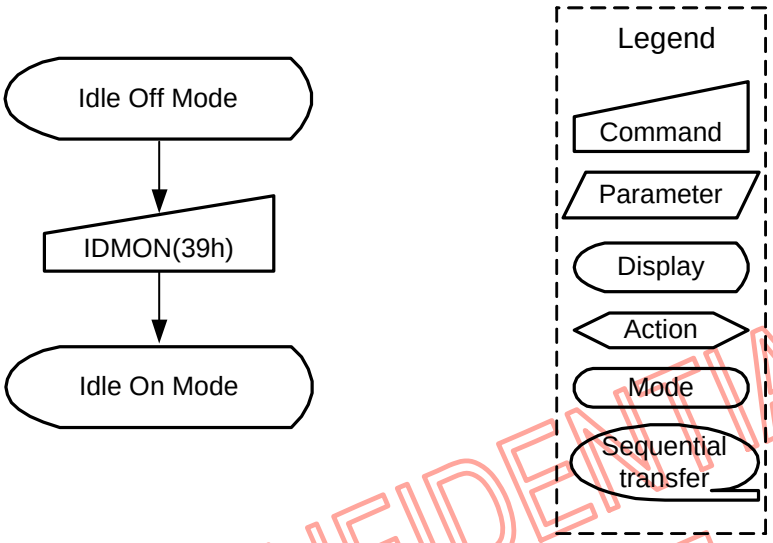
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart



COLMOD: Interface Pixel Format (3A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
COLMOD	Write	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is to be transferred via the RGB interface. The formats are shown in the table:

Bit	NAME	DESCRIPTION
VIPF3	Pixel Format for RGB Interface	"0101" = 16-bit/pixel "0110" = 18-bit/pixel "0111" = 24-bit/pixel The others = not defined
VIPF2		
VIPF1		
VIPF0		
IFPF3	Pixel Format for Control Interface	"0101" = 16-bit/pixel "0110" = 18-bit/pixel "0111" = 24-bit/pixel The others = not defined
IFPF2		
IFPF1		
IFPF0		

Restriction

There is no visible effect until the Frame Memory is written to.

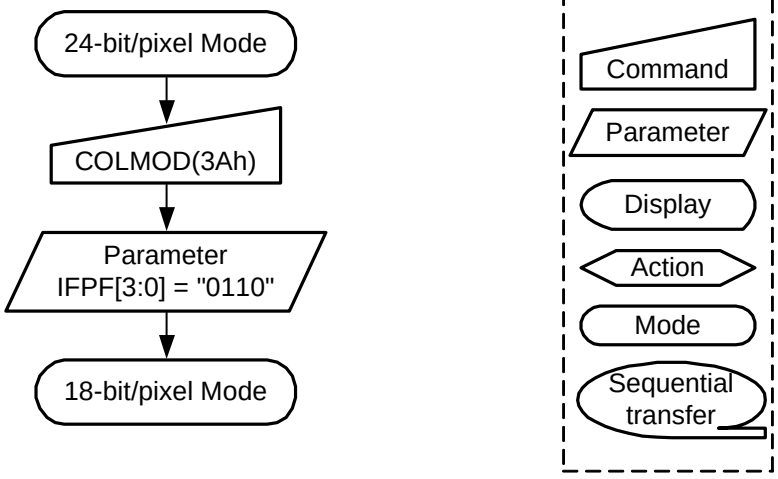
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	77h
S/W Reset	77h
H/W Reset	77h

Flow Chart



RAMWRC: Memory Write Continue (3C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWRC	Write	3Ch	3C00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

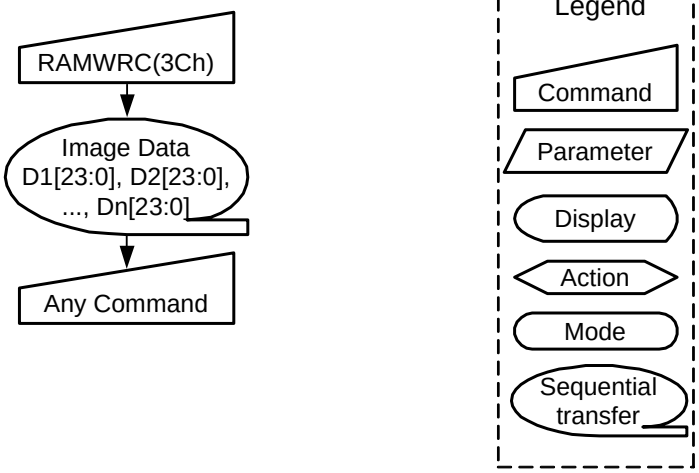
Description	This command is used to transfer data from MPU interface to frame memory, if there is wanted to continue memory write after "RAMWR Memory Write (2Ch)" command. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTL setting Then D[23:0] is stored in frame memory and the column register and the row register incremented. Sending any other command can stop Frame Write.
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



RAMRDC: Memory Read Continue (3E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRDC	Read	3Eh	3E00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command is used to transfer data from frame memory to MPU interface, if there is wanted to continue memory write after "RAMRD Memory Read (2Eh)" command.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting.
Then D[23:0] is read back from the frame memory and the column register and the row register incremented
Frame Read can be canceled by sending any other command.

Restriction

There is no restriction on length of parameters. No access in the frame memory in Sleep In mode

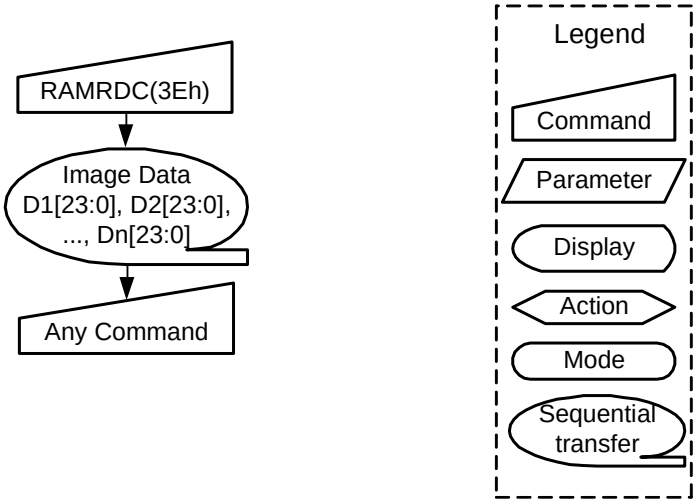
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



STESL: Set Tearing Effect Scan Line (4400h~4401h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
STESL	Write	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8
			4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0

NOTE: "-" Don't care

Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.

Note that STESL with N[15:0]="000h" is equivalent to TEON with M="0"
The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.
This command takes affect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.

Restriction

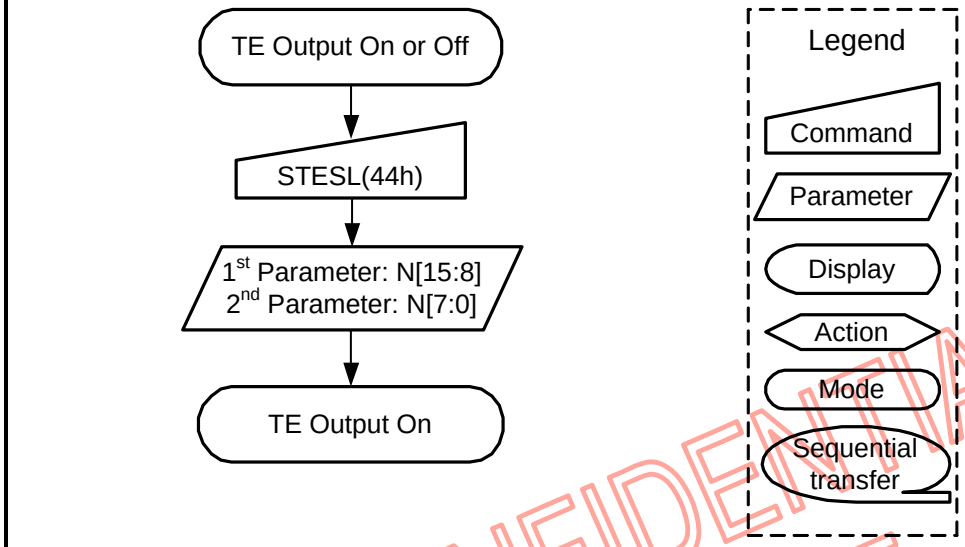
When N[15:0] is greater than maximum scanning line like below, data of out of range will be ignored.
For CGM[7:0] = "70h" (480 x 864 resolution)
Parameter range 0 ≦ N[15:0] ≦ 864 (0360h)
For CGM[7:0] = "6Bh" (480 x 854 resolution)
Parameter range 0 ≦ N[15:0] ≦ 854 (0356h)
For CGM[7:0] = "50h" (480 x 800 resolution)
Parameter range 0 ≦ N[15:0] ≦ 800 (0320h)
For CGM[7:0] = "28h" (480 x 720 resolution)
Parameter range 0 ≦ N[15:0] ≦ 720 (02D0h)
For CGM[7:0] = "00h" (480 x 640 resolution)
Parameter range 0 ≦ N[15:0] ≦ 640 (0280h)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

GSL: Get Scan Line (4500h~4501h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GSL	Read	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8
			4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0

NOTE: "-" Don't care

Description

This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC + VBP + VADR + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0.
When in Sleep in mode, the returned value is undefined.

Restriction

-

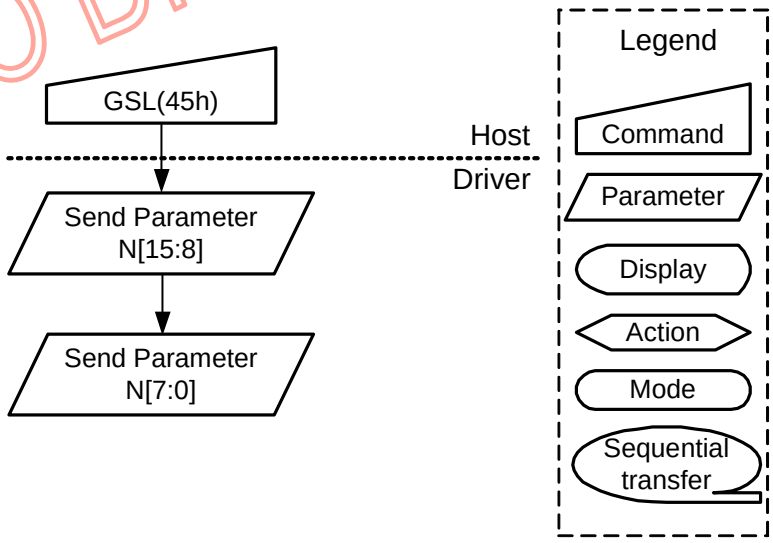
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	XXXXh
S/W Reset	XXXXh
H/W Reset	XXXXh

Flow Chart



DPCKRGB: Display Clock in RGB Interface (4A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPCKRGB	Write	X	4A00h	00h	0	0	0	0	0	0	0	ICM

NOTE: "-" Don't care

Description

This command is used to select SRAM data input path and display clock in RGB interface.

ICM	Data Write to SRAM		SRAM Data Read to Display
	SRAM Write Clock	SRAM Data Input Path	Internal Display Clock
0	PCLK	D[23:0]	VS, HS and PCLK
1	SCL	SDI	Internal Oscillator

Restriction

-

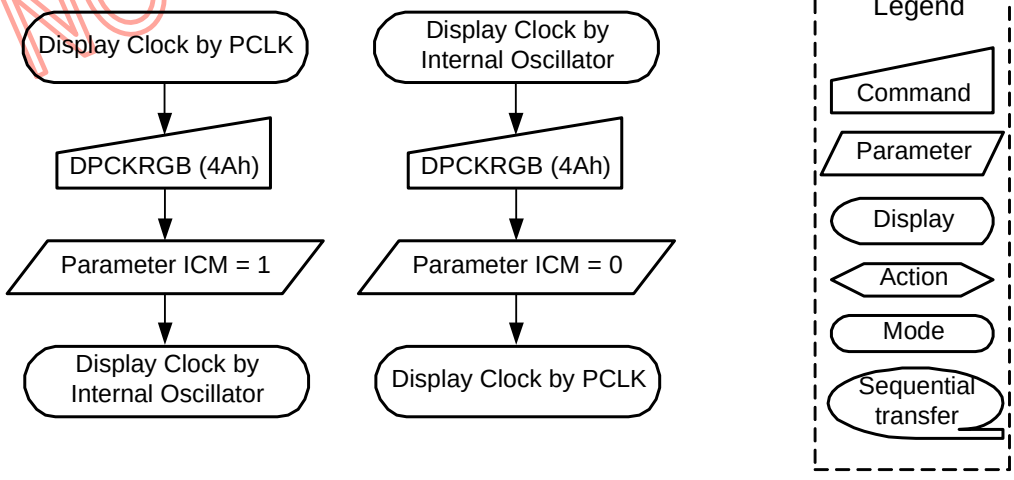
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ICM = "0"
S/W Reset	ICM = "0"
H/W Reset	ICM = "0"

Flow Chart



DSTBON: Deep Standby Mode On (4F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DSTBON	Write	X	4F00h	00h	0	0	0	0	0	0	0	DSTB

NOTE: "-" Don't care

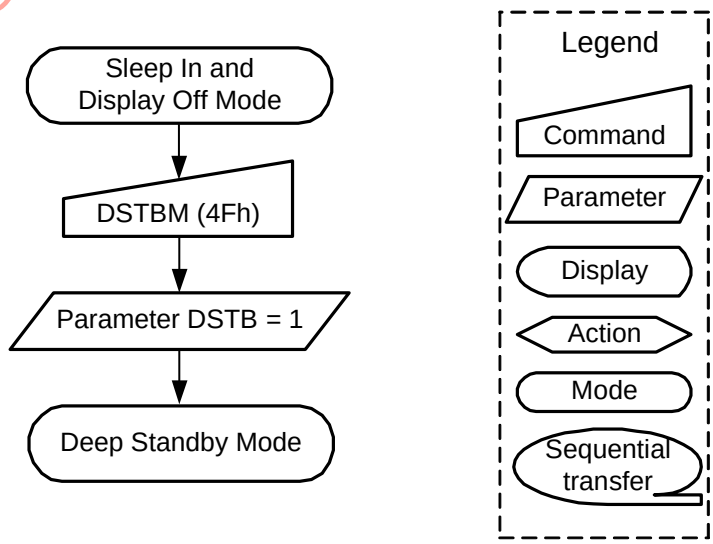
Description	This command is used to enter deep standby mode. DSTB="1", enter deep standby mode. Notes: 1. Before setting this command, enter Sleep In Mode (1000h) and Display Off (2800h) first. User can not write this register in Sleep-Out and Display-On mode. 2. It can not exit Deep Standby Mode while setting bit DSTB from "1" to "0". 3. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DSTB = "0"
S/W Reset	DSTB = "0"
H/W Reset	DSTB = "0"

Flow Chart



WRPFD: Write Profile Value for Display (5000h~500Fh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRPFD	Write	50h	5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010
			5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020
			5002h	00h	V037	V036	V035	V034	V033	V032	V031	V030
			:	00h	:	:	:	:	:	:	:	:
			500Dh	00h	V147	V146	V145	V144	V143	V142	V141	V140
			500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150
			500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160

NOTE: "-" Don't care

Description	This command is used to define profile values for display.
Restriction	-

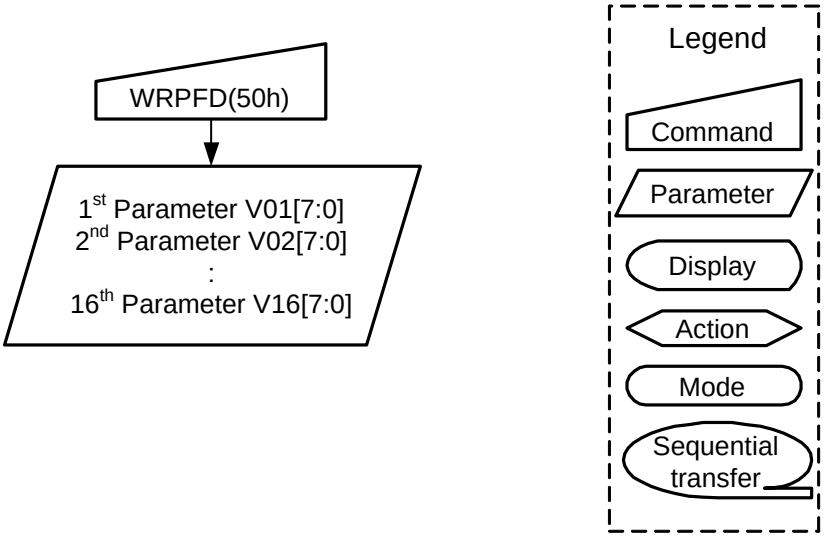
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



WRDISBV: Write Display Brightness (5100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	Write	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

NOTE: "-" Don't care

Description

This command is used to adjust brightness value.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0%
01h	2/256	0.78125%
:	:	:
FEh	255/256	99.609375%
FFh	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

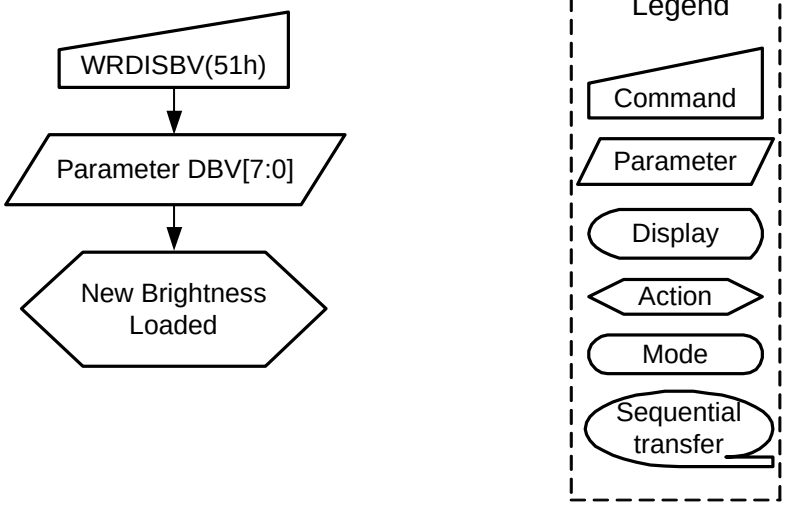
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDISBV: Read Display Brightness (5200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDISBV	Read	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

NOTE: "-" Don't care

Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
Restriction	-

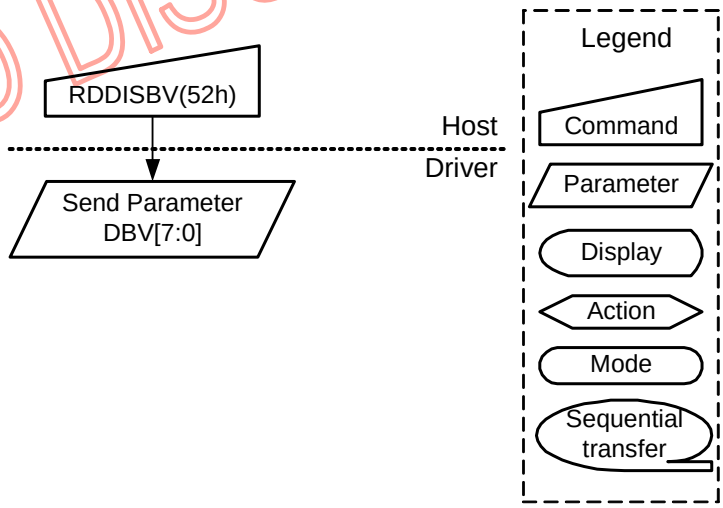
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCTRLD: Write CTRL Display (5300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	Write	53h	5300h	00h	0	0	BCTRL	A	DD	BL	DB	G

NOTE: "-" Don't care

Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

A	DESCRIPTION	PWM duty for LEDPWM Pin
0	Off	By DBV[7:0] of command "WRDISBV (5100h)"
1	On	By LABC block

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

DB: Display Brightness Manual/Automatic

DB	DESCRIPTION
0	Manual, the user has to use this setting for manual adjustment of the brightness to have an effect.
1	Automatic, information about the used brightness is included in the active profile.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

G: Gamma Curve Manual/Automatic

G	DESCRIPTION
0	Manual, by GAMSET-command
1	Automatic, information about the used gamma is included in the active profile.

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

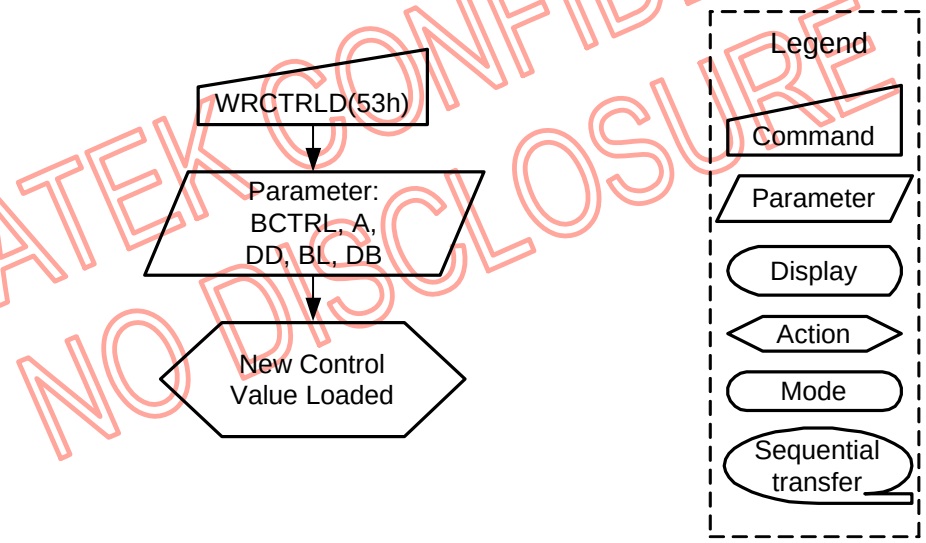
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCTRLD: Read CTRL Display Value (5400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCTRLD	Read	54h	5400h	00h	0	0	BCTRL	A	DD	BL	DB	G

NOTE: "-" Don't care

Description

This command returns ambient light, brightness control and gamma setting value.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

A	DESCRIPTION	PWM duty for LEDPWM Pin
0	Off	By DBV[7:0] of command "WRDISBV (5100h)"
1	On	By LABC block

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

DB: Display Brightness Manual/Automatic

DB	DESCRIPTION
0	Manual, the user has to use this setting for manual adjustment of the brightness to have an effect.
1	Automatic, information about the used brightness is included in the active profile.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

G: Gamma Curve Manual/Automatic

G	DESCRIPTION
0	Manual, by GAMSET-command
1	Automatic, information about the used gamma is included in the active profile.

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

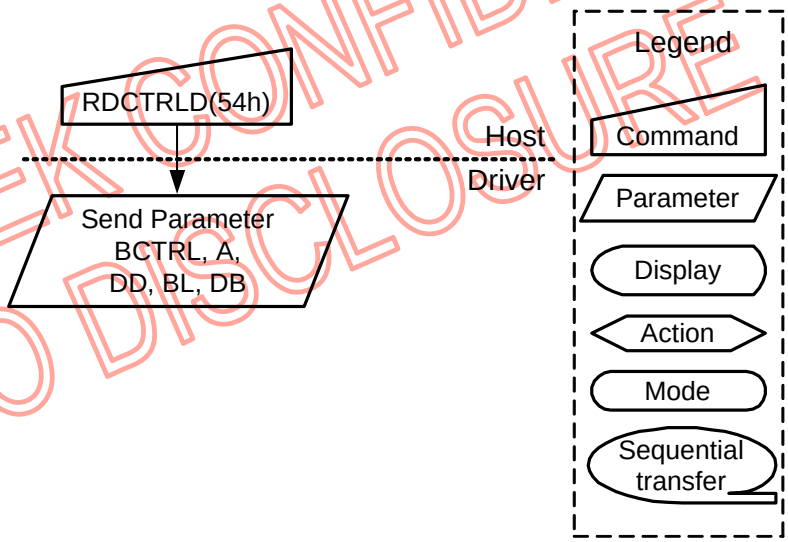
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCABC: Write Content Adaptive Brightness Control (5500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABC	Write	55h	5500h	00h	0	0	0	0	0	0	C1	C0

NOTE: "-" Don't care

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Picture Image (Moving-Mode)

Restriction

This register is synchronized with V-sync by internal circuit.

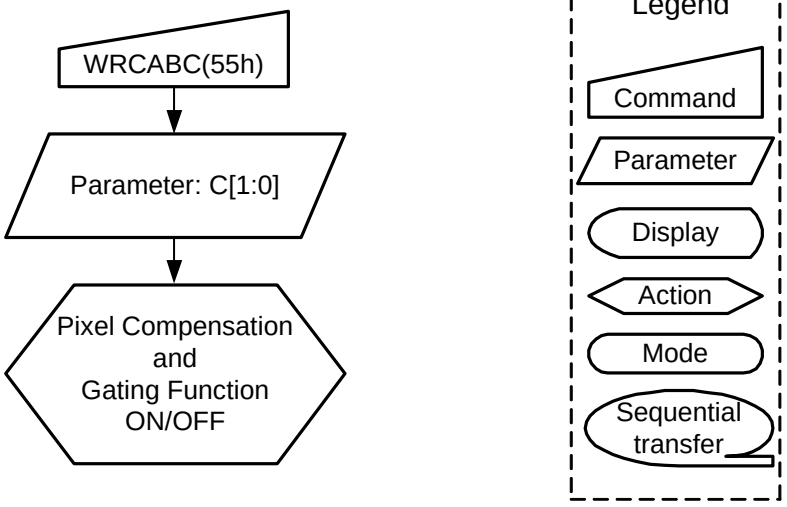
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCABC: Read Content Adaptive Brightness Control (5600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABC	Read	56h	5600h	00h	0	0	0	0	0	0	C1	C0

NOTE: "-" Don't care

Description

This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Picture Image (Moving-Mode)

Restriction

-

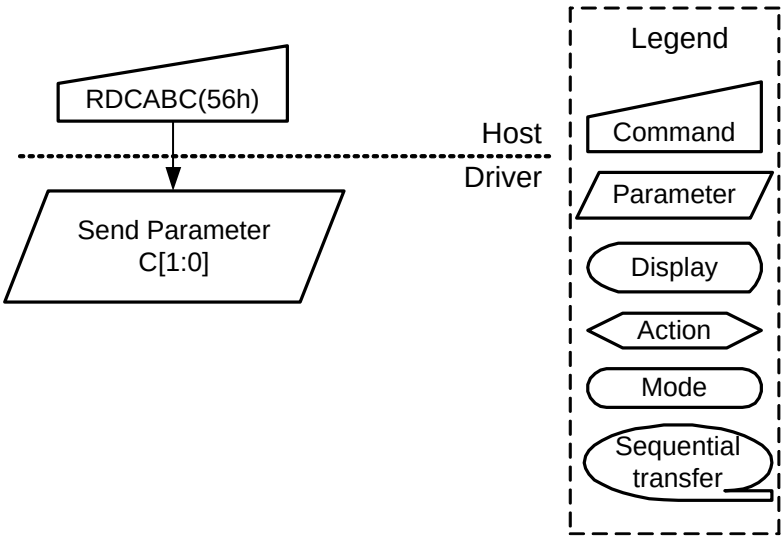
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRHYSTE: Write Hysteresis (5700h~573Fh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRHYSTE	Write	57h	5700h	00h	I0115	I0114	I0113	I0112	I0111	I0110	I019	I018
			5701h	00h	I017	I016	I015	I014	I013	I012	I011	I010
			5702h	00h	I0215	I0214	I0213	I0212	I0211	I0210	I029	I028
			5703h	00h	I027	I026	I025	I024	I023	I022	I021	I020
			:	00h	In15	In14	In13	In12	In11	In10	In9	In8
			:	00h	In7	In6	In5	In4	In3	In2	In1	In0
			571Ch	00h	I1515	I1514	I1513	I1512	I1511	I1510	I159	I158
			571Dh	00h	I157	I156	I155	I154	I153	I152	I151	I150
			571Eh	00h	I1615	I1614	I1613	I1612	I1611	I1610	I169	I168
			571Fh	00h	I167	I166	I165	I164	I163	I162	I161	I160
			5720h	00h	D0115	D0114	D0113	D0112	D0111	D0110	D019	D018
			5721h	00h	D017	D016	D015	D014	D013	D012	D011	D010
			5722h	00h	D0215	D0214	D0213	D0212	D0211	D0210	D029	D028
			5723h	00h	D027	D026	D025	D024	D023	D022	D021	D020
			:	00h	Dn15	Dn14	Dn13	Dn12	Dn11	Dn10	Dn9	Dn8
			:	00h	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0
			573Ch	00h	D1515	D1514	D1513	D1512	D1511	D1510	D159	D158
			573Dh	00h	D157	D156	D155	D154	D153	D152	D151	D010
			573Eh	00h	D1615	D1614	D1613	D1612	D1611	D1610	D169	D168
			573Fh	00h	D167	D166	D165	D164	D163	D162	D161	D160

NOTE: "-" Don't care

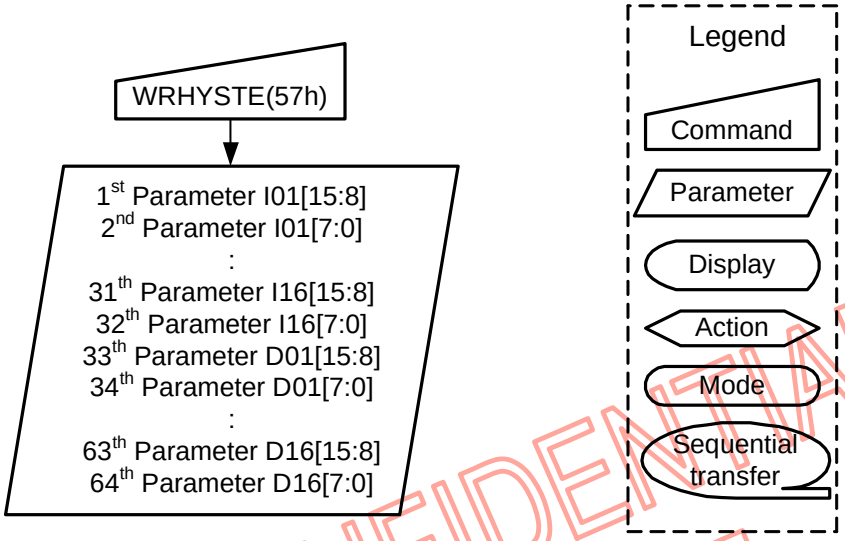
Description	This command is used to define Hysteresis filter function. In[15:0] defines increment values and Dn[15:0] defines decrement values. Don't care about the parameter values after "65535 (FFFFh)". I16[15 : 0] bits and D16[15 : 0] bits are always set to "65535 (FFFFh)" internally, if I15[15 : 0] bits and D15[15 : 0] bit are still valid and less than "65535 (FFFFh)".
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



WRGAMMSET: Write Gamma Setting (5800h~5807h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRGAMMSET	Write	58h	5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010
			5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030
			5802h	00h	G063	G062	G061	G060	G053	G052	G051	G050
			5803h	00h	G083	G082	G081	G080	G073	G072	G071	G070
			5804h	00h	G103	G102	G101	G100	G093	G092	G091	G090
			5805h	00h	G123	G122	G121	G120	G113	G112	G111	G110
			5806h	00h	G143	G142	G141	G140	G133	G132	G131	G130
			5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150

NOTE: "-" Don't care

Description

This command is used to define gamma setting values for each luminance level.
Gamma value is defined on command "Gamma Set (2600h)".

Gn[3:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G=2.2)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Restriction

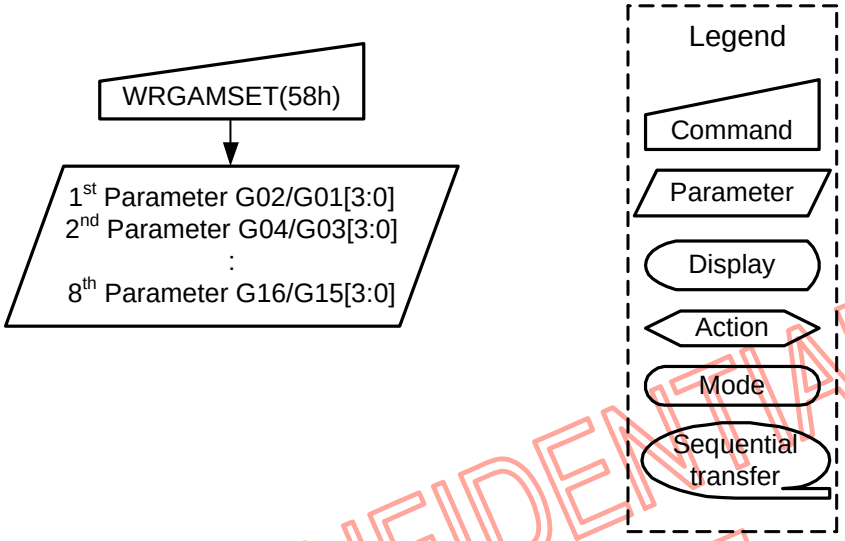
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart	

RDFSVM: Read FS Value MSBs (5A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFSVM	Read	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8

NOTE: "-" Don't care

Description

This command returns MSBs (FSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading.
Another command for LSBs (FSV[7:0]). See the command "Read FS Value LSBs (5B00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

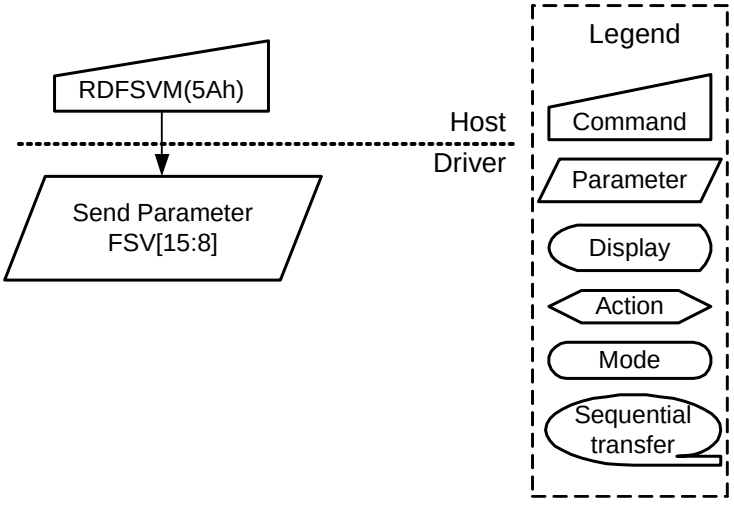
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDFSVL: Read FS Value LSBs (5B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFSVL	Read	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0

NOTE: "-" Don't care

Description

This command returns LSBs (FSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading.
Another command for MSBs (FSV[15:8]). See the command "Read FS Value MSBs (5A00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

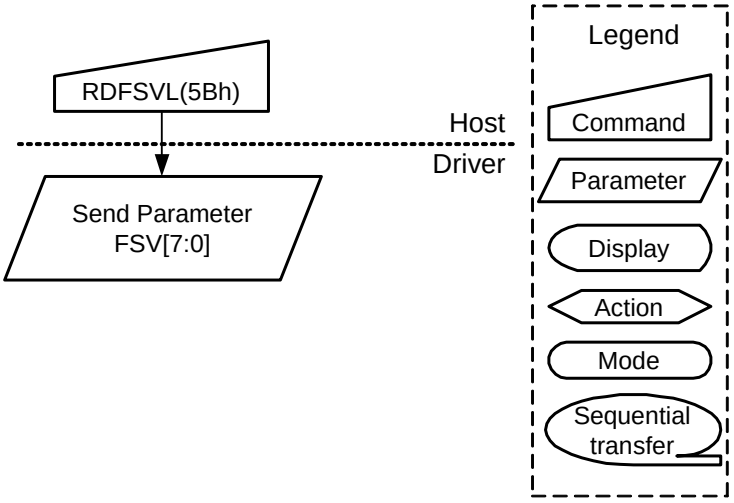
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDMFFSVM: Read Median Filter FS Value MSBs (5C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDMFFSVM	Read	5Ch	5C00h	00h	FFSV15	FFSV14	FFSV13	FFSV12	FFSV11	FFSV10	FFSV9	FFSV8

NOTE: "-" Don't care

Description

This command returns MSBs (FFSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the median filter.
Another command for LSBs (FFSV[7:0]). See the command "Read Median Filter FS Value LSBs (5D00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FFSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FFSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

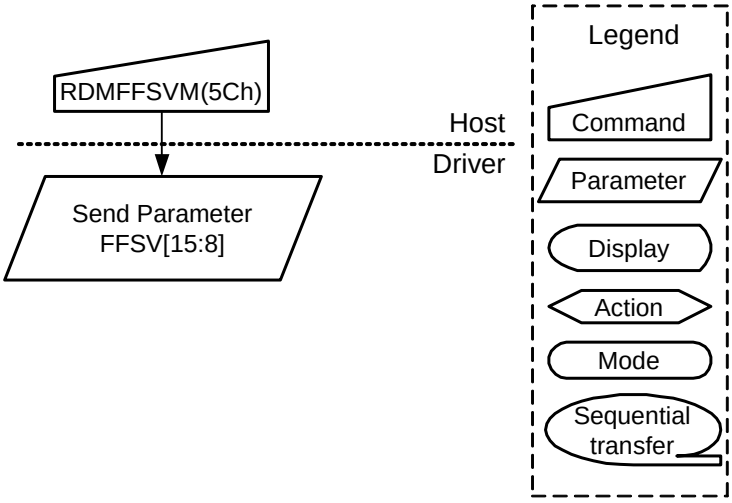
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDMFFSVL: Read Median Filter FS Value LSBs (5D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDMFFSVL	Read	5Dh	5D00h	00h	FFSV7	FFSV6	FFSV5	FFSV4	FFSV3	FFSV2	FFSV1	FFSV0

NOTE: "-" Don't care

Description

This command returns LSBs (FDSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the median filter.
Another command for MSBs (FFSV[15:8]). See the command "Read Median Filter FS Value MSBs (5C00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FFSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

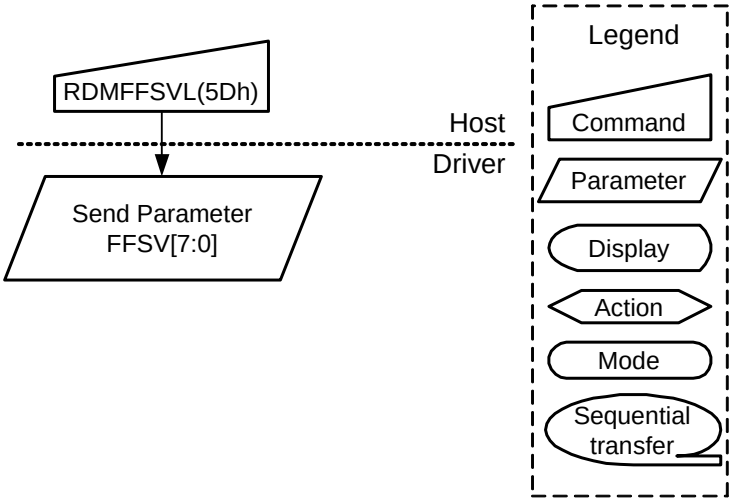
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCABCMB: Write CABC minimum brightness (5E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABCMB	Write	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

NOTE: "-" Don't care

Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-

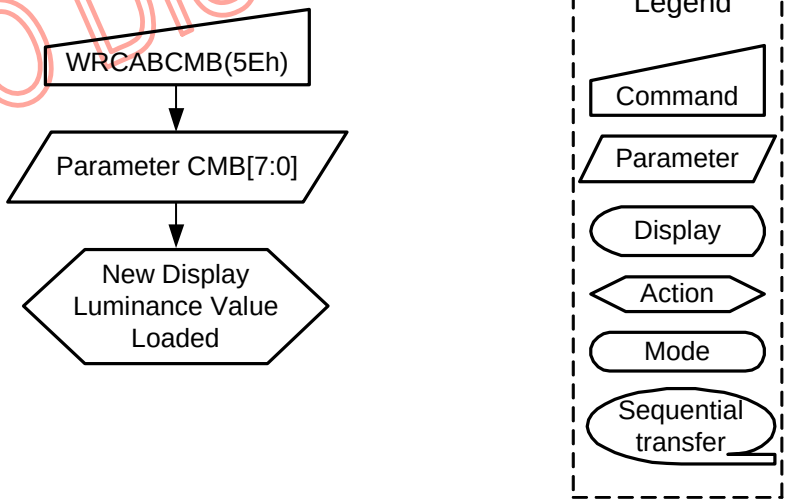
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCABCMB: Read CABC minimum brightness (5F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABCMB	Read	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

NOTE: "-" Don't care

Description

This command return the minimum brightness value of CABC function
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
CMB[7:0] is minimum brightness forCABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.

Restriction

-

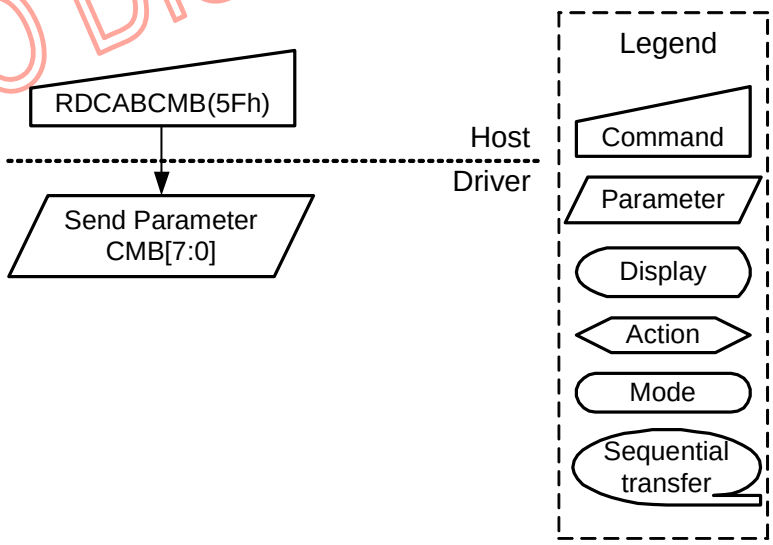
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRLSCC: Write Light Sensor Compensation Coefficient Value (6500h~6501h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRLSCC	Write	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
			6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

NOTE: "-" Don't care

Description	This command is used to send the compensation coefficient value (CC[15 : 0]). Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary).
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

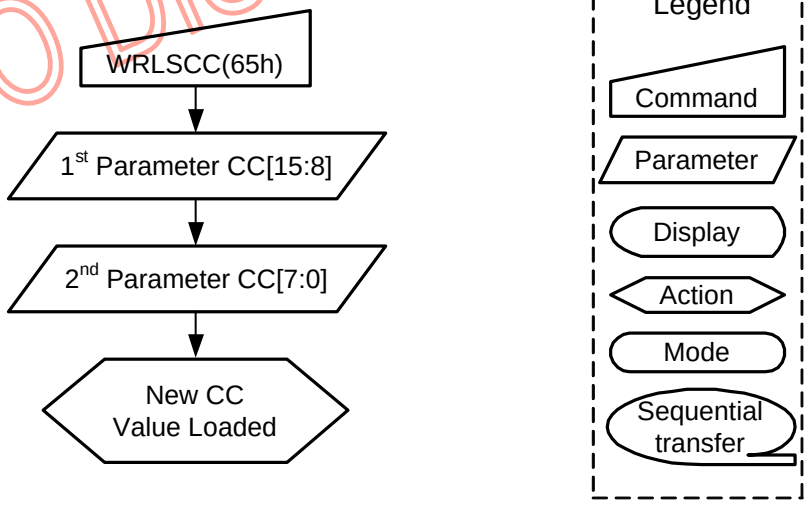
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8000h
S/W Reset	8000h
H/W Reset	8000h

Flow Chart



RDLSCCM: Read Light Sensor Compensation Coefficient Value MSBs (6600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDLSCCM	Write	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

NOTE: "-" Don't care

Description

This command returns MSBs of the compensation coefficient value (CC[15:8]) which is stored by "Write Light Sensor Compensation Coefficient Value (6500h)" command.
It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order.
Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "1000 000".

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

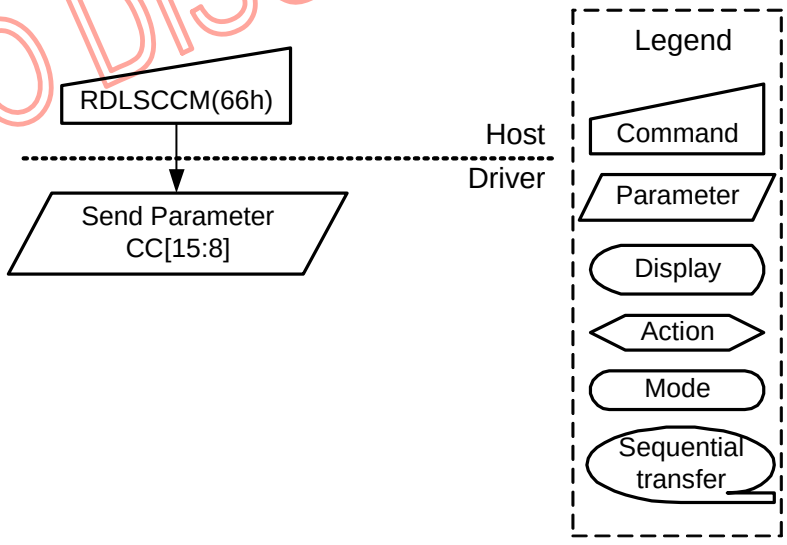
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



RDLSCCL: Read Light Sensor Compensation Coefficient Value LSBs (6700h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDLSCCL	Write	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

NOTE: "-" Don't care

Description	This command returns LSBs of the compensation coefficient value (CC[7:0]) which is stored by "Write Light Sensor Compensation Coefficient Value (6501h)" command. It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order. Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "0000 000".
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

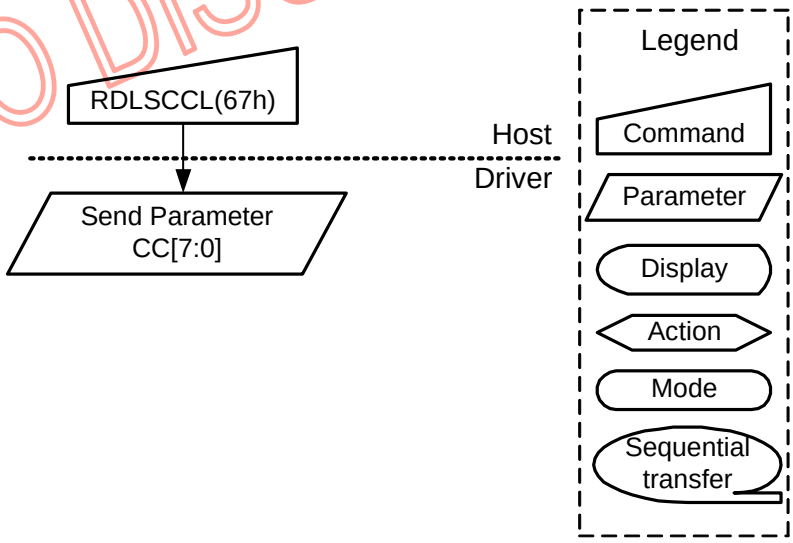
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDBWLB: Read Black/White Low Bits (7000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBWLB	Read	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0

NOTE: "-" Don't care

Description	This command returns the lowest bits of black and white color characteristic. Black: Bkx and Bky White: Wx and Wy
Restriction	-

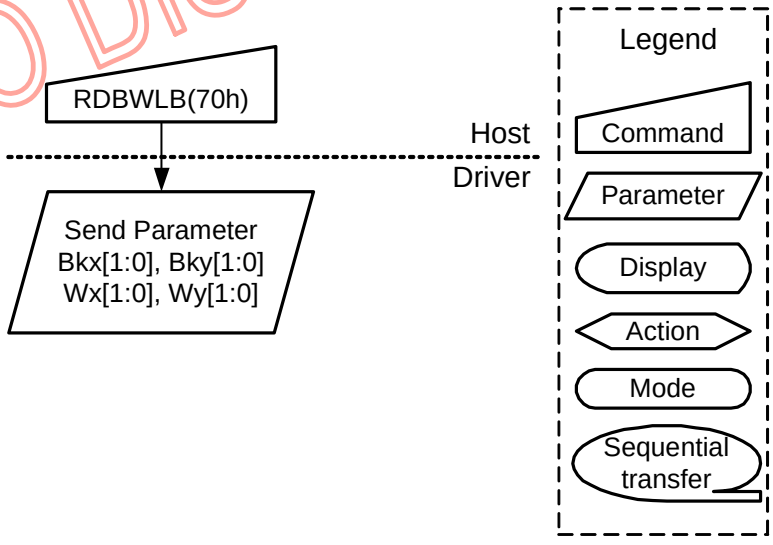
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBkx: Read Bkx (7100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBkx	Read	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2

NOTE: "-" Don't care

Description	This command returns the Bkx bit (Bkx[9:2]) of black color characteristic.
Restriction	-

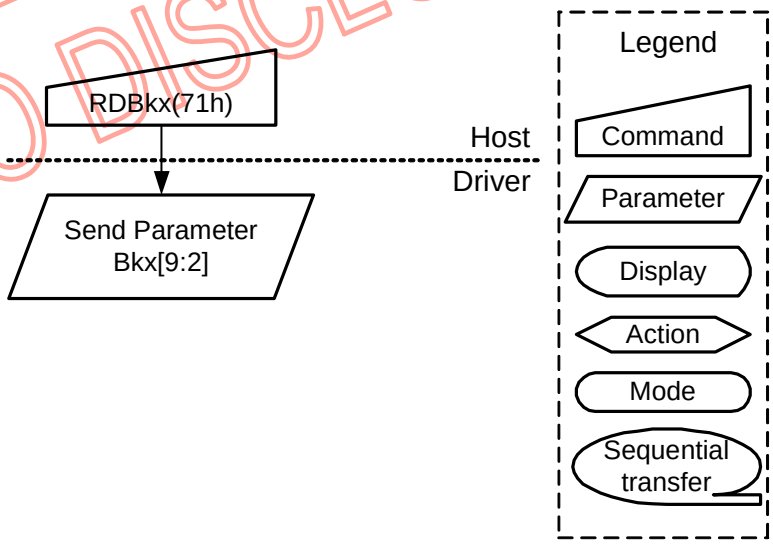
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBky: Read Bky (7200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBky	Read	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2

NOTE: "-" Don't care

Description	This command returns the Bky bit (Bky[9:2]) of black color characteristic.
Restriction	-

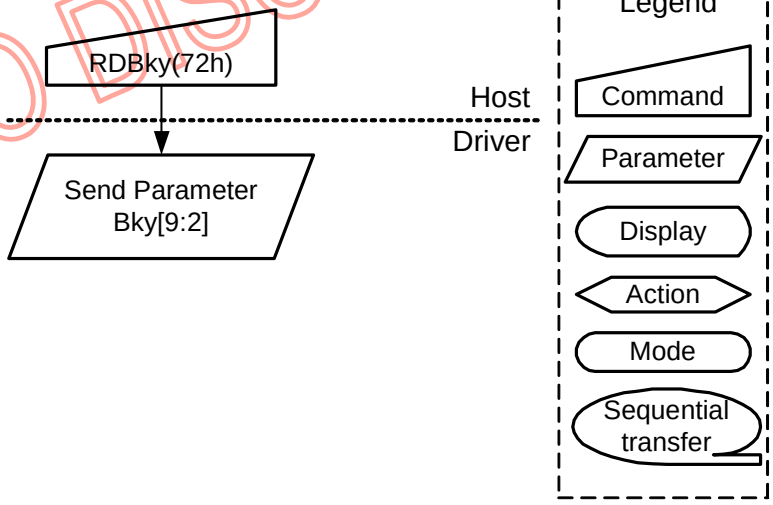
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDWx: Read Wx (7300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWx	Read	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2

NOTE: "-" Don't care

Description	This command returns the Wx bit (Wx[9:2]) of white color characteristic.
Restriction	-

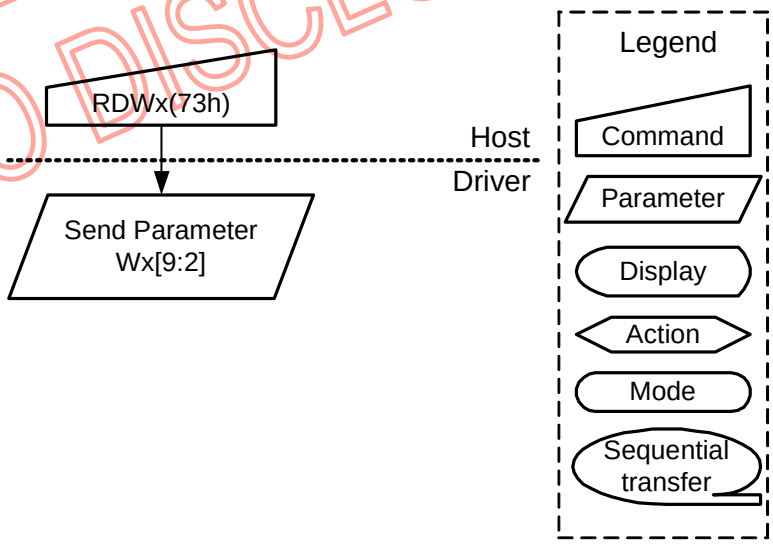
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDWy: Read Wy (7400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWy	Read	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2

NOTE: "-" Don't care

Description	This command returns the Wy bit (Wy[9:2]) of white color characteristic.
Restriction	-

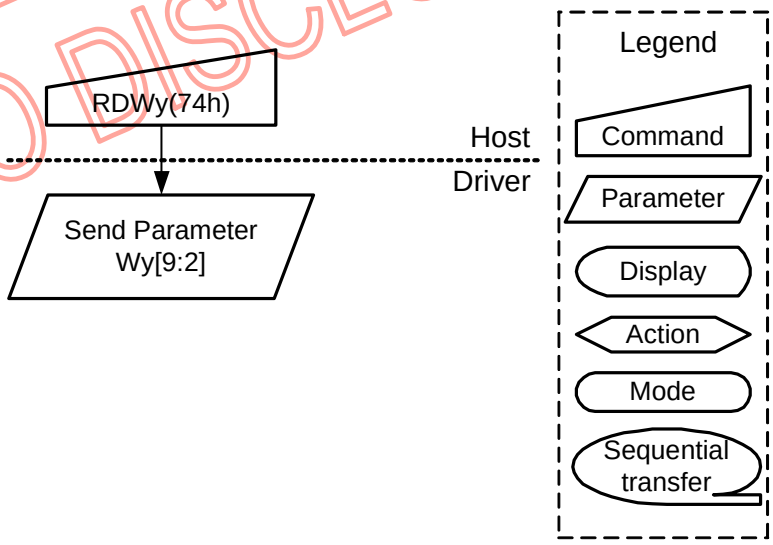
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRGLB: Read Red/Green Low Bits (7500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRGLB	Read	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0

NOTE: "-" Don't care

Description	This command returns the lowest bits of red and green color characteristic. Red: Rx and Ry Green: Gx and Gy
Restriction	-

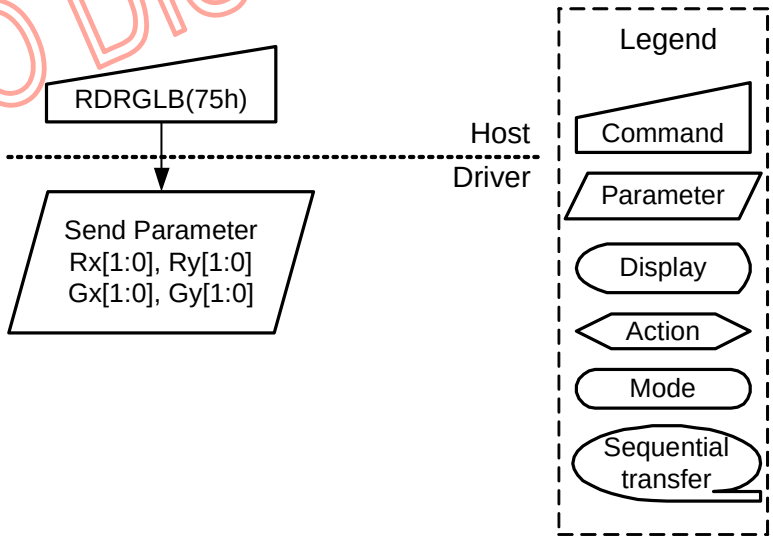
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRx: Read Rx (7600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRx	Read	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2

NOTE: "-" Don't care

Description	This command returns the Rx bit (Rx[9:2]) of red color characteristic.
Restriction	-

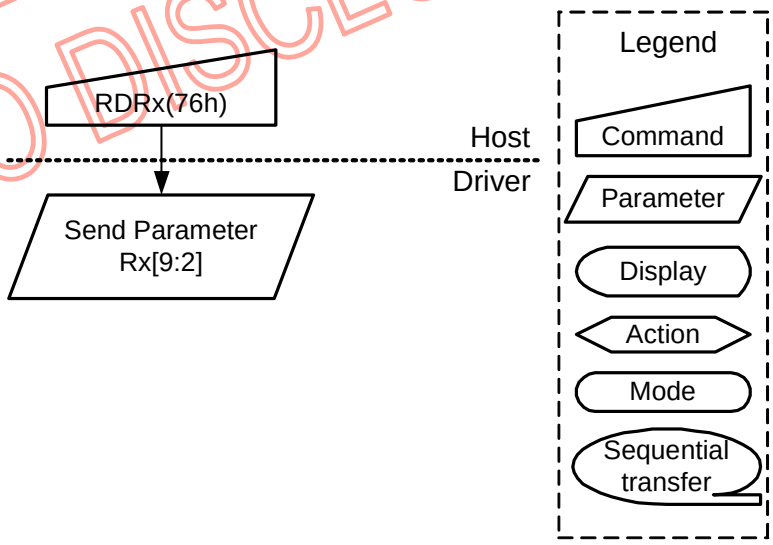
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRy: Read Ry (7700h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRy	Read	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2

NOTE: "-" Don't care

Description	This command returns the Ry bit (Ry[9:2]) of red color characteristic.
Restriction	-

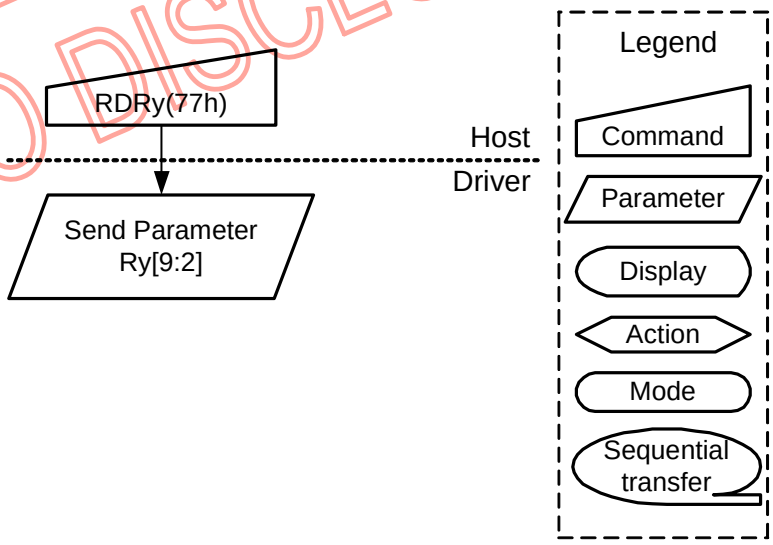
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDGx: Read Gx (7800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGx	Read	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2

NOTE: "-" Don't care

Description	This command returns the Gx bit (Gx[9:2]) of green color characteristic.
Restriction	-

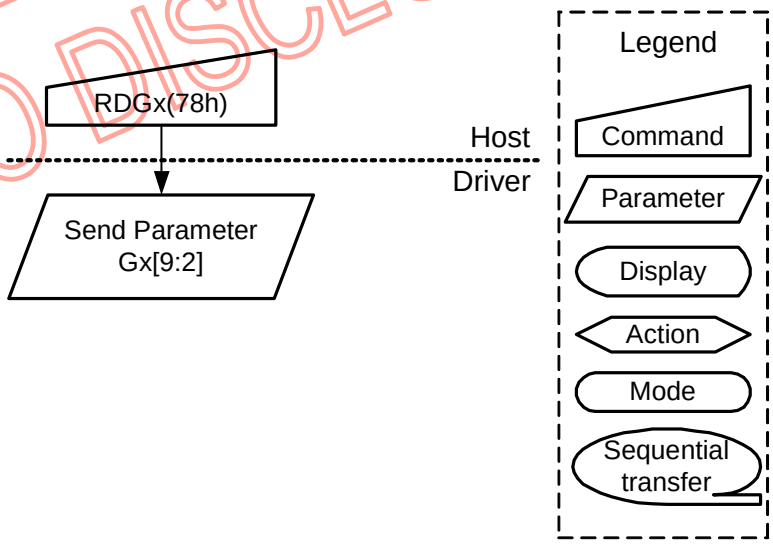
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDGy: Read Gy (7900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGy	Read	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2

NOTE: "-" Don't care

Description	This command returns the Gy bit (Gy[9:2]) of green color characteristic.
Restriction	-

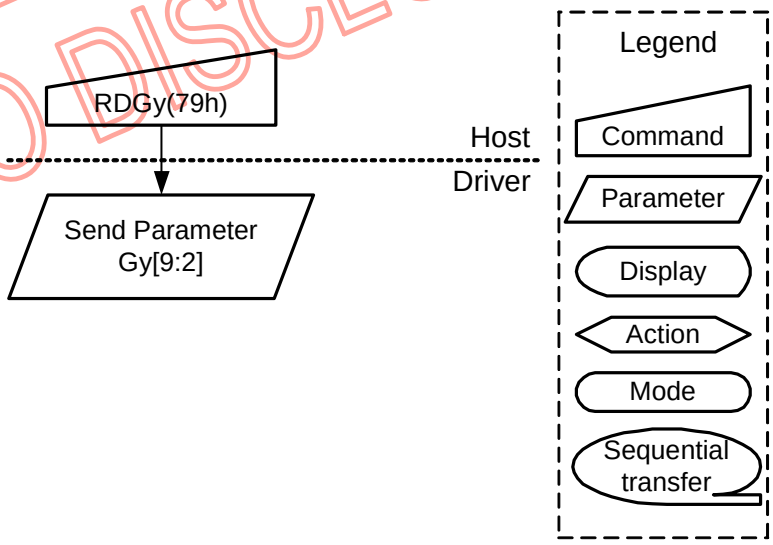
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBALB: Read Blue/AColor Low Bits (7A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBALB	Read	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0

NOTE: "-" Don't care

Description	This command returns the lowest bits of blue and A color characteristic. Blue: Bx and By A: Ax and Ay
Restriction	-

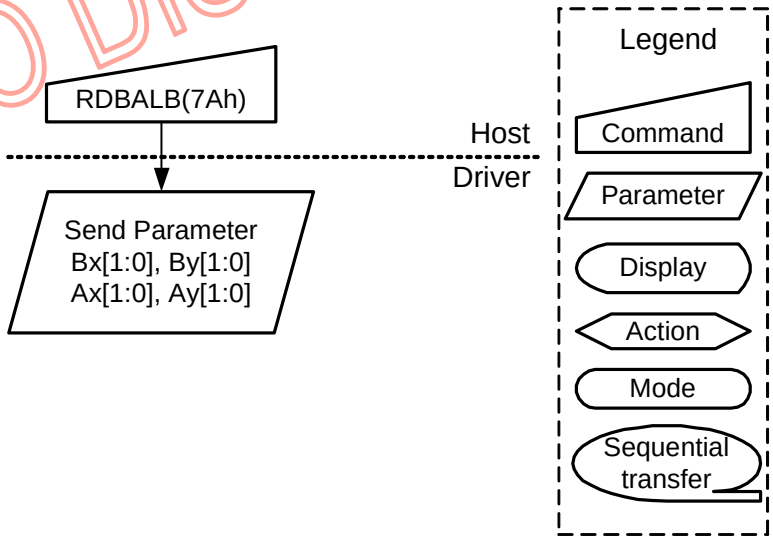
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBx: Read Bx (7B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBx	Read	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2

NOTE: "-" Don't care

Description	This command returns the Bx bit (Bx[9:2]) of blue color characteristic.
Restriction	-

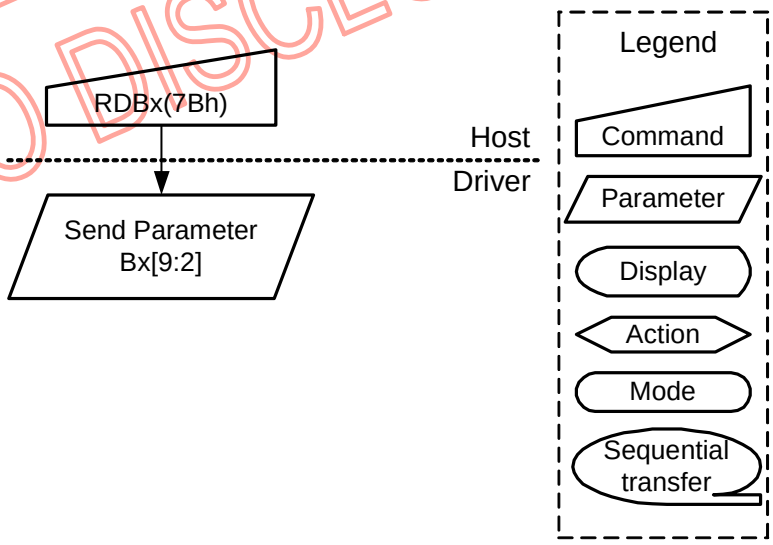
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBy: Read By (7C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBy	Read	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2

NOTE: "-" Don't care

Description	This command returns the By bit (By[9:2]) of blue color characteristic.
Restriction	-

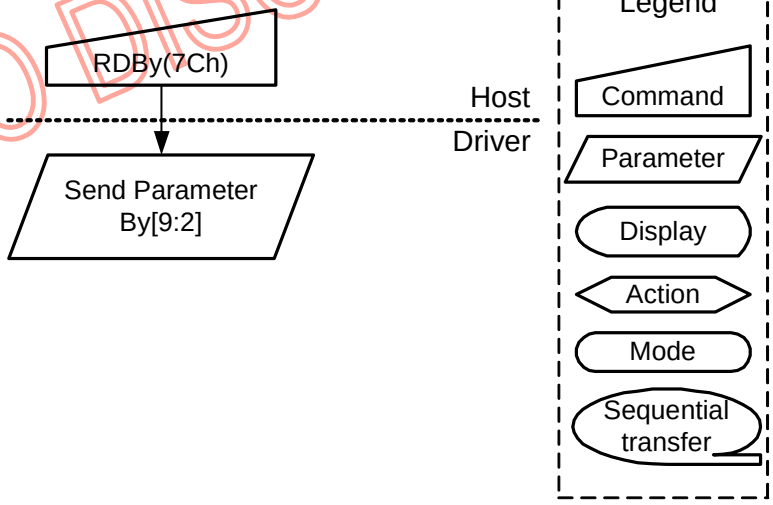
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDAx: Read Ax (7D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAx	Read	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2

NOTE: "-" Don't care

Description	This command returns the Ax bit (Ax[9:2]) of A color characteristic.
Restriction	-

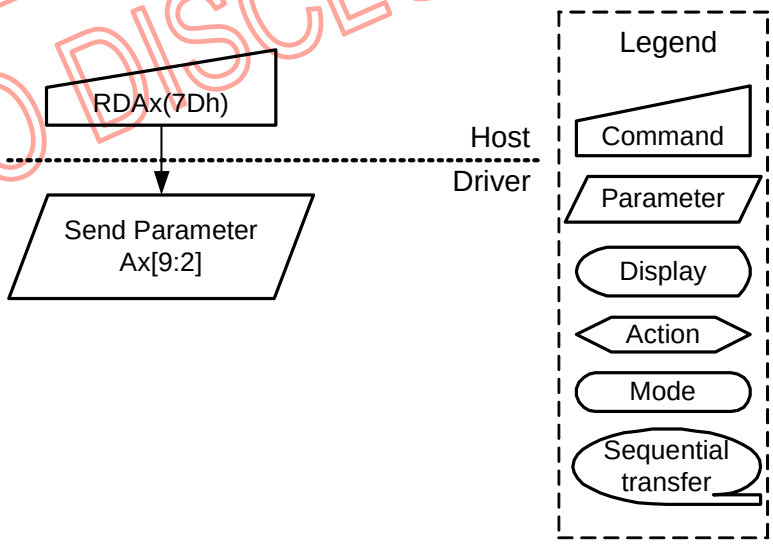
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDAy: Read Ay (7E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAy	Read	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2

NOTE: "-" Don't care

Description	This command returns the Ay bit (Ay[9:2]) of A color characteristic.
Restriction	-

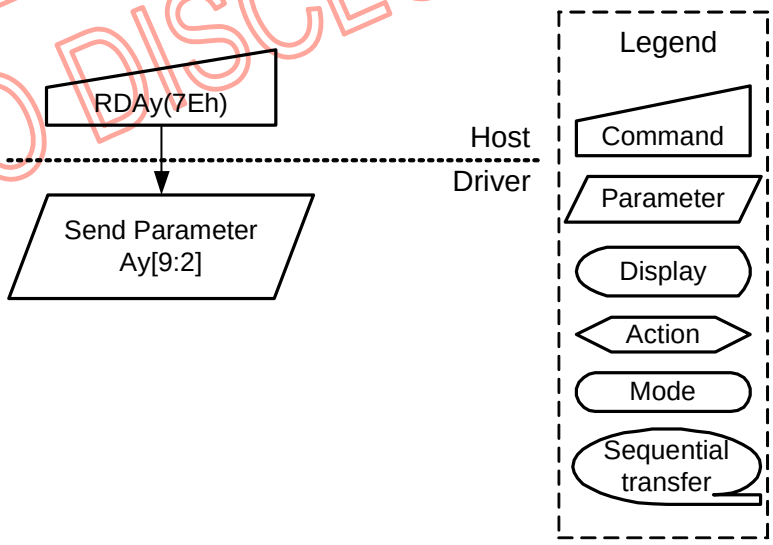
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDDDBS: Read DDB Start (A100h~A104h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDDBS	Read	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
			A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A104h	00h	1	1	1	1	1	1	1	1

NOTE: "-" Don't care

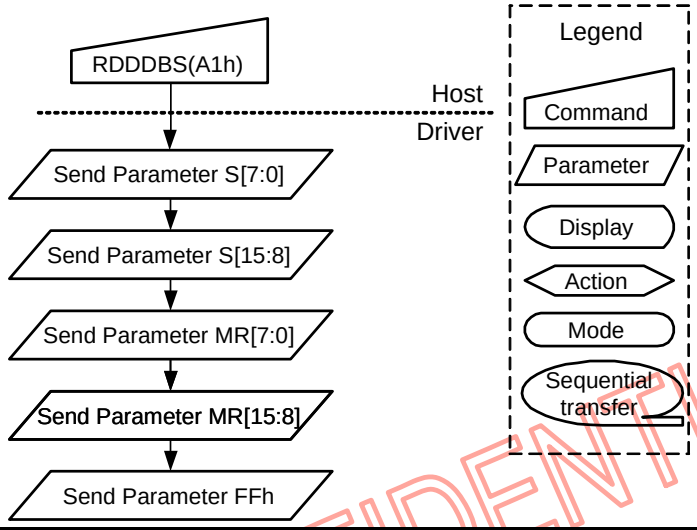
Description	This command returns the supplier identification and display module mode/revision information. *Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning.* *Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.* This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent. SID[15:0]: Supplier identification MID[15:0]: Module ID
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDDDBC: Read DDB Continue (A800h~A804h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDDBC	Read	A8h	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
			A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A804h	00h	1	1	1	1	1	1	1	1

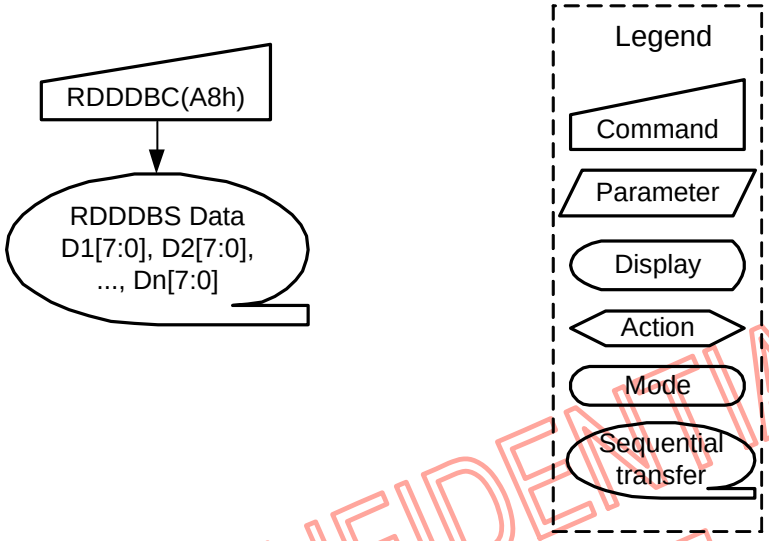
NOTE: "-" Don't care

Description	This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command. *Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.* *Note: For use example,* *1. Set maximum return packet size=3* *2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]* *3. Read 0xA8, return 2 bytes MID[15:8] and 0xFF*
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart	

RDFCS: Read First Checksum (AA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFCS	Read	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0

NOTE: "-" Don't care

Description	This command returns the first checksum what has been calculated from "User Command Set" area registers (not include "Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 150ms after there is the last write access on "User Command Set" area registers before there can read this checksum value.

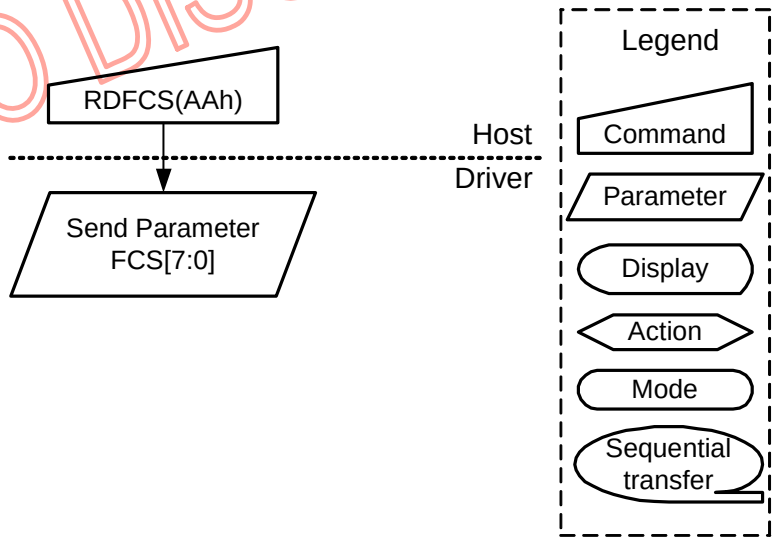
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCCS: Read Continue Checksum (AF00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCCS	Read	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0

NOTE: "-" Don't care

Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from "User Command Set" area registers and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 300ms after there is the last write access on "User Command Set" area registers before there can read this checksum value in the first time.

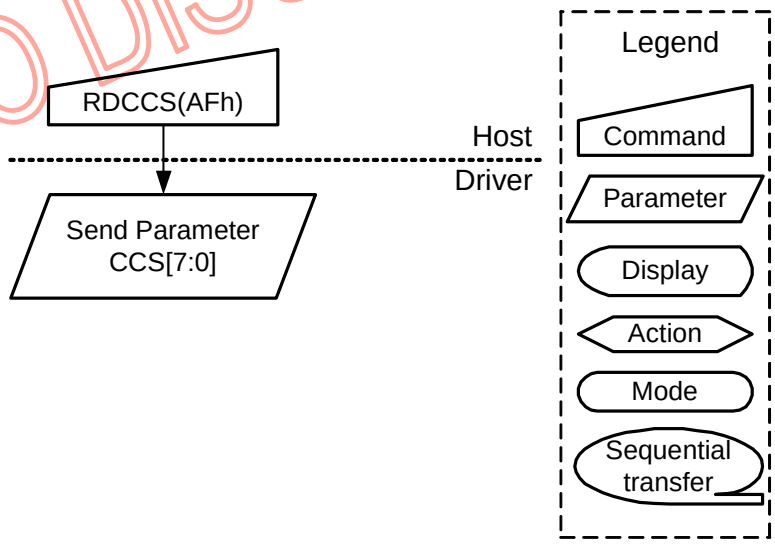
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDID1: Read ID1 Value (DA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

NOTE: "-" Don't care

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-

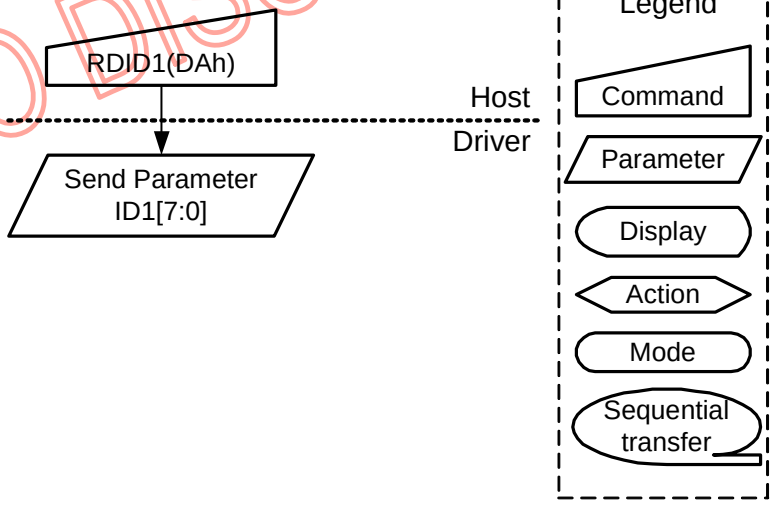
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDID2: Read ID2 Value (DB00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

NOTE: "-" Don't care

Description	This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 80h to FFh
Restriction	-

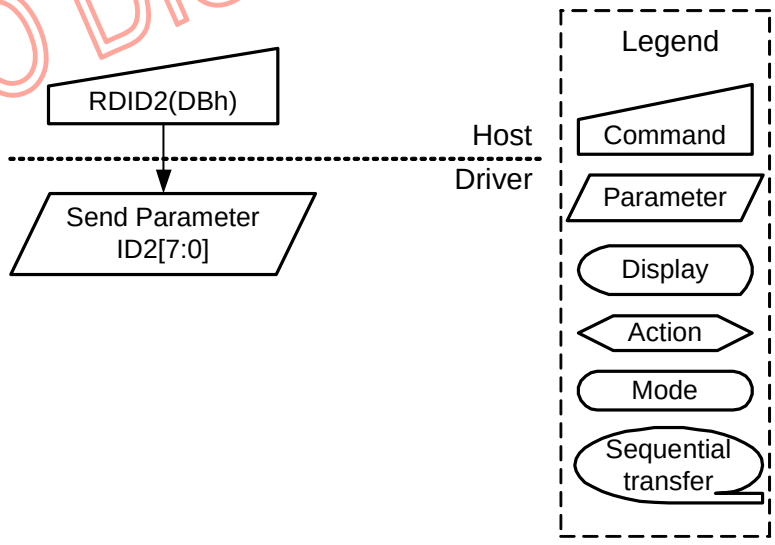
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	80h
S/W Reset	MTP Value	80h
H/W Reset	MTP Value	80h

Flow Chart



RDID3: Read ID3 Value (DC00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

Description	This parameter read byte identifies the TFT LCD module/driver.
Restriction	-

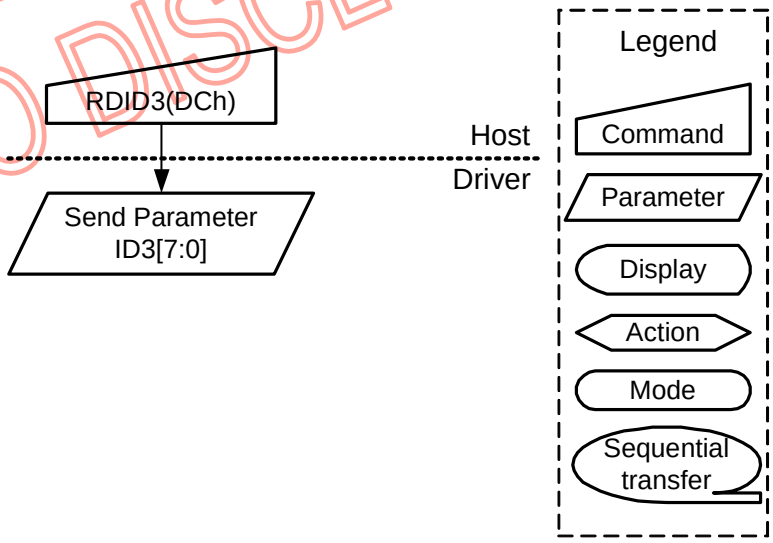
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VDDA, VDDB, VDDR,VDDAM	-0.3 ~ +5.5	V
Supply voltage (Logic)	VDDI	- 0.3 ~ +5.5	V
Supply voltage (Digital)	DVDD,DIOPWR	-0.3 ~ +2.0	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ +6.6	V
	AVEE-AVSS	+0.3 ~ -6.6	V
Supply voltage (HV)	VGH-VGLX (VGHO-VGLO)	-0.3 ~ +33	V
Logic Input voltage range	VIN	- 0.3 ~ VDDI + 0.3	V
Logic Output voltage range	VO	- 0.3 ~ VDDI + 0.3	V
Differential Input Voltage	HSSI_CLK_P/N, HSSI_DATA0_P/N, HSSI_DATA1_P/N	-0.3 ~ +1.8	V
Operating temperature range	TOPR	-40 ~ +85	ºC
Storage Temperature range	TSTG	-55 ~ +125	ºC

NOTE:
If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 ESD Protection Level

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 2500	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 250	V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

7.4 Light Sensitivity

The operation of the IC will not be materially altered by incident light.

7.5 DC Characteristics

7.5.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.3	3.7	4.8	V	Note 1, 2
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1, 2
	VDDIL	I/O supply voltage	1.1	1.2	1.3	V	
Input / Output							
Logic High level input voltage	VIH	VDDI=1.65~3.3V	0.7 VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL	VDDI=1.65~3.3V	VSSI	-	0.3 VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	VDDI=1.65~3.3V IOH = -1.0mA	0.8 VDDI	-	VDDI	V	Note 1, 2, 5
Logic Low level output voltage	VOL	VDDI=1.65~3.3V IOL = +1.0mA	VSSI	-	0.2 VDDI	V	Note 1, 2, 5
Logic High level leakage (Except MIPI/MDDI)	ILIH	Vin=0~VDDI	-	-	1	µA	Note 1, 2, 3
Logic Low level leakage (Except MIPI/MDDI)	ILIL	Vin=0~VDDI	-1	-	-	µA	Note 1, 2, 3
Logic High level leakage (MIPI/MDDI)	ILIH	Vin=0~VDDAM	-	-	1	µA	Note 2, 8
Logic Low level leakage (MIPI/MDDI)	ILIL	Vin=0~VDDAM	-1	-	-	µA	Note 2, 8
DC/DC Converter Operation							
AVDD booster voltage	AVDD	-	4.5	-	6.5	V	Note 2, 7
AVEE booster voltage	AVEE	-	-6.5	-	-4.5	V	Note 2, 7
VCL booster voltage	VCL	-	-2.5	-	-4.0	V	Note 2, 7
VGH booster voltage	VGH	-	AVDD +VDDB	-	2AVDD -AVEE	V	Note 2, 6
VGLX booster voltage	VGLX	-	AVEE +VCL	-	2AVEE -AVDD	V	Note 2, 6
Voltage difference between VGH and VGLX	VGHL	|VGH-VGLX|	-	-	30	V	Note 2
Oscillator tolerance	ΔOSC	25 ºC	-5	-	5	%	
Source Driver							
Gamma reference voltage	VGMP	-	3.0	-	6.3	V	Note 2
	VGSP	-	0.0	-	3.7	V	Note 2
	VGMN	-	-6.3	-	-3.0	V	Note 2
	VGSN	-	-3.7	-	0.0	V	Note 2
Output offset voltage	VOFSET	-	-	-	45	mV	Note 4
Output deviation voltage	Vdev	Sout≥4.0V, Sout≥1.0V	-	-	20	mV	Note 4
		1.0V<Sout<4.0V	-	-	10	mV	Fig.7.5.2

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSSI=VSS=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB, VDDIM, VDDAM and VSS means VSSA, VSSR, VSSB, AVSS, VSSIM, VSSAM.
VDDB, VDDA and VDDR should be the same input voltage level.
Note 2) When the measurements are performed with module, measurement points are like below.
Note 3) WRX, RDX, CSX, D[23:0], D/CX, PCLK, VS, HS, DE, SDI, NBWSEL, DSWAP, PSWAP, LANSEL, EXB1T, VGSW[3:0] I2C_SA0,RGBBP,, IM[3:0], DSTB_SEL and Test pins.
Note 4) Channel loading= 40pF / channel, Ta=25 ºC.
Note 5) SDO, ERR, GPO[3:0] and Test pins
Note 6) VDDB=2.8V, Ta=25 ºC, no load on panel and Iload=2mA, \|Output Voltage – Target Voltage\| < 100mV.
Note 7) VDDB=2.8V, Ta=25 ºC, no load on panel and Iload=?mA, power pad serial resistor is smaller than maximum value.
Note 8) Vin = 0 to VDDAM, VDD=2.3 to 4.8V, VDDI=1.65 to 3.3V, VSSAM=VSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).

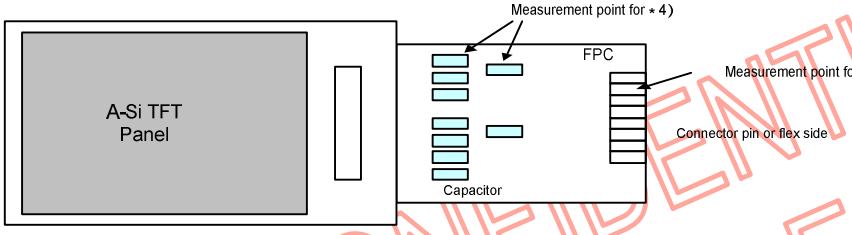


Fig. 7.5.1 Measurement Points for All Characteristics.

-When Sout >=4.0V, Sout<=1.0V
|(S0, S1, S2, …. , S1440) – Average (S0, S1, S2, …. , S1440)| <= 20mV
-When 4.0V>Sout>1.0V
|(S0, S1, S2, …. , S1440) – Average (S0, S1, S2, …. , S1440)| <= 10mV
-Sout=V0~V255
$|S_{Target}$ – Average (S0, S1, S2, …. , S1440)| <= 45mV

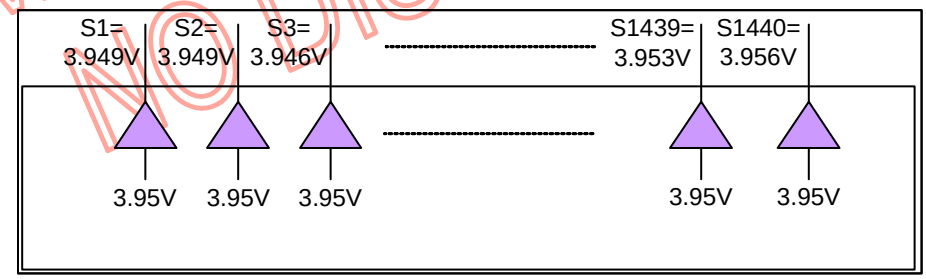


Fig. 7.5.2 Source output deviation

7.5.2 MIPI Characteristics

7.5.2.1 DC CHARACTERISTICS FOR DSI LP MODE

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.65~3.3V, VDD=2.3 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VDD means VDDAM, VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

Note 2) DSI high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

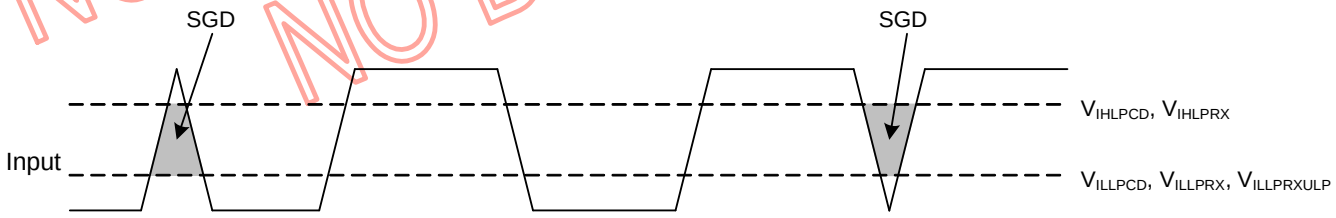


Fig. 7.5.3 Spike/Glitch rejection-DSI

7.5.2.2 DC CHARACTERISTICS FOR DSI HS MODE

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-D0+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-D0+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-D0+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-D0+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-D0+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-D0+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-D0+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-D0+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-D0+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-D0+/-	-	-	14	pF

Note 1) VDDI=1.65~3.3V, VDD=2.3 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VDD means VDDAM, VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.

Note 4) Without 50mV (-50mV to 50mV) ground difference.

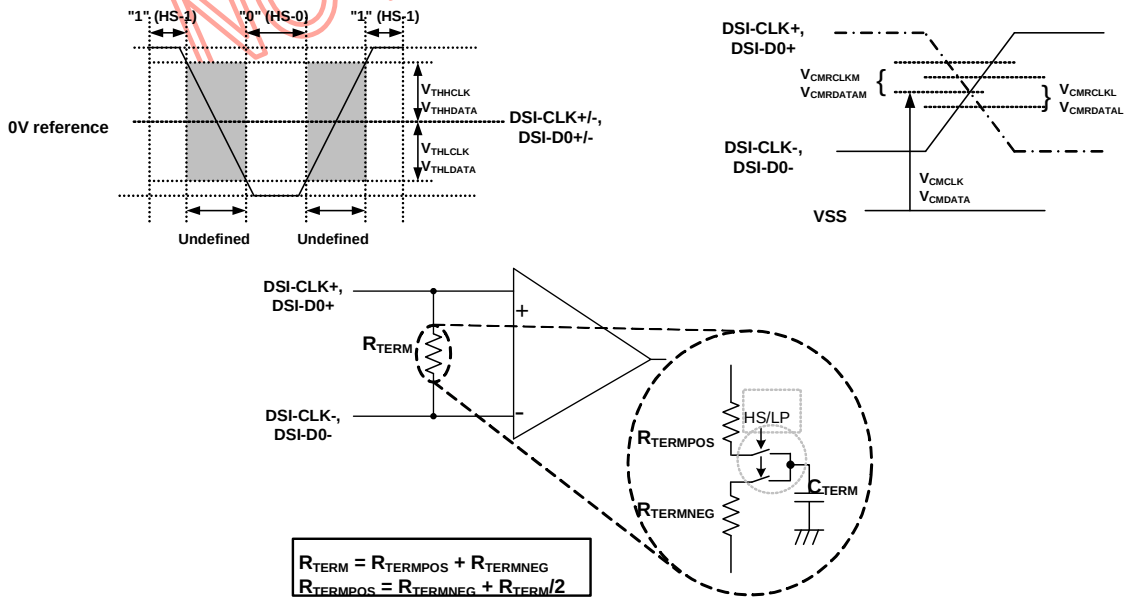


Fig. 7.5.4 Differential voltage range, termination resistor and Common mode voltage

7.5.3 MDDI Characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Differential input “High” level voltage (hibernation wake-up)	$V_{IT+offset}$	VT=125mV (MDDI_DATA_P/M)	-	100	125	mV
Differential input “Low” level voltage (hibernation wake-up)	$V_{IT-offset}$	VT=125mV (MDDI_DATA_P/M)	75	100	-	mV
Differential input “High” level voltage	V_{IT+}	VT=0mV (MDDI_STB_P/M, MDDI_DATA_P/M)	-	0	50	mV
Differential input “Low” level voltage	V_{IT-}	VT=0mV (MDDI_STB_P/M, MDDI_DATA_P/M)	-50	0	-	mV
Current consumption in Hibernation	I_{HIB}	VDDI=1.8V, VDDAM=2.85V, 1/Tbit=384Mbps, Ta=25ºC	-	TBD	TBD	µA
Current consumption in Data Transfer	I_{Trans}	VDDI=1.8V, VDDAM=2.85V, 1/Tbit=384Mbps, Ta=25ºC, In Video Stream Packet Transfer	-	TBD	TBD	mA
Terminal impedance	Zt	-	80	-	125	ohm

Note 1) VDDI= 1.65~3.3V, VDD=2.3 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VDD means VDDAM, VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

7.6 AC Characteristics

7.6.1 Parallel Interface Characteristics (80-Series MCU)

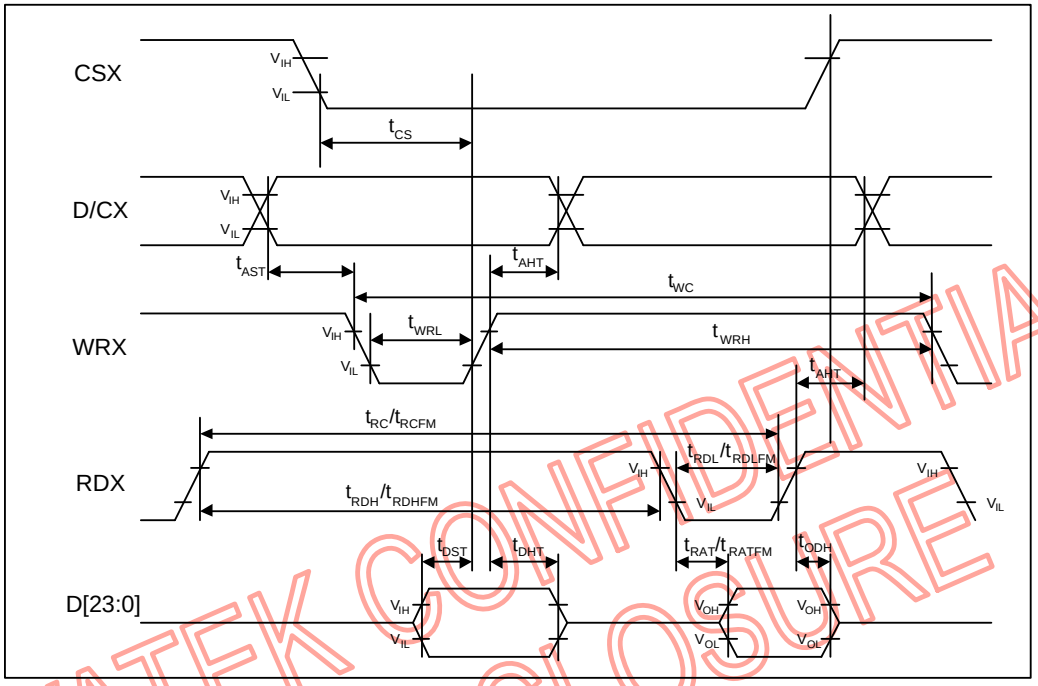


Fig. 7.6.1 Parallel interface characteristics (80-Series)

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
WRX	tWC	Write cycle	33	-	ns	
	tWRH	Control pulse "H" duration	15	-	ns	
	tWRL	Control pulse "L" duration	15	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90	-	ns	
	tRDL	Control pulse "L" duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	400	-	ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	250	-	ns	
	tRDLFM	Control pulse "L" duration (FM)	150	-	ns	
D/CX	tAST	Address setup time (Write)	0	-	ns	
		Address setup time (Read)	10	-	ns	
	tAHT	Address hole time	2	-	ns	
D[17:0]	tDST	Data setup time	15	-	ns	
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	150	ns	
	tODH	Output disable time	5	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB

Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.6.2 Serial Interface Characteristics

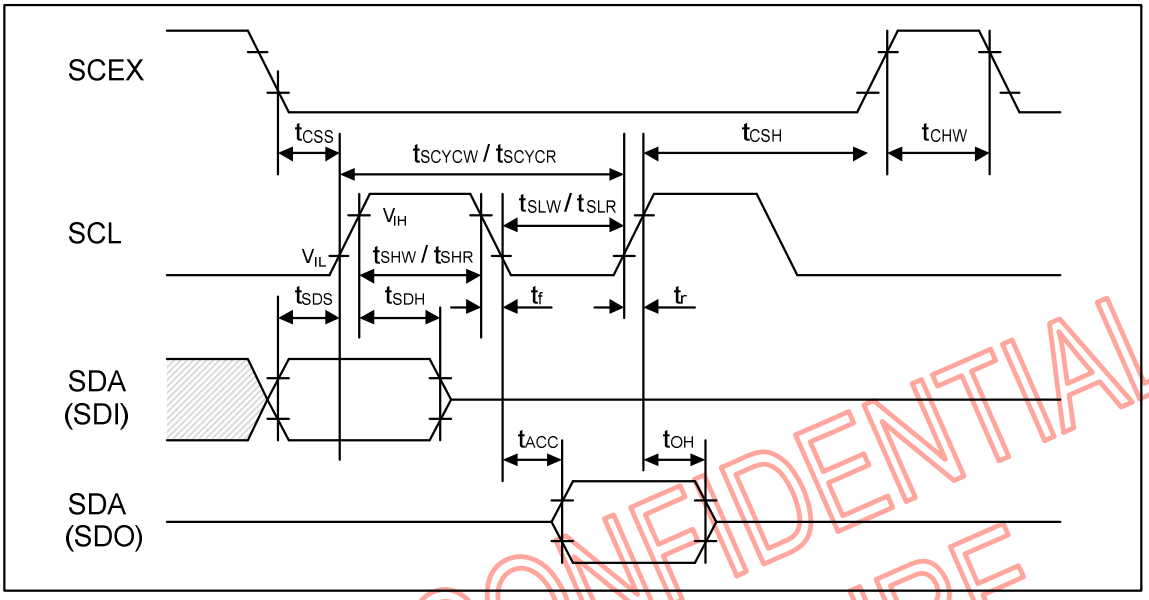


Fig. 7.6.2 3-pin serial interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70˚C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	40	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
	t_{SCYCR}	Serial clock cycle (Read GRAM)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read GRAM)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read GRAM)	140	-	ns	
	t_{SCYCR}	Serial clock cycle (Read ID)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read ID)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read ID)	140	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSX	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

7.6.3 I2C Bus Timing Characteristics

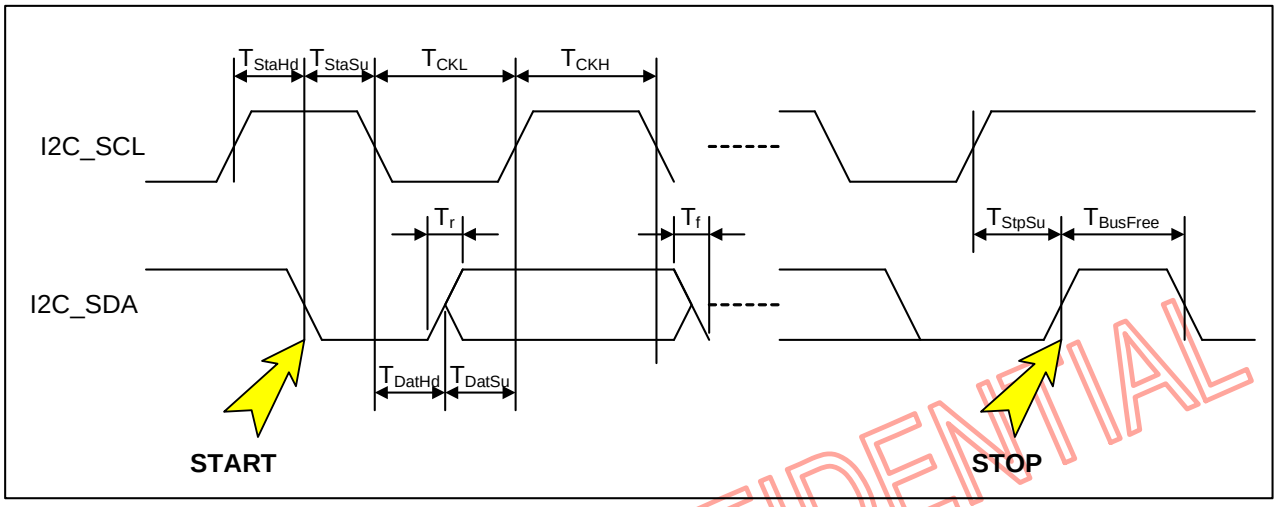


Fig. 7.6.3 I2C Bus Operation

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
I2C_SCL	$T_{CKL}+T_{CKL}$	Working frequency	-	400	KHz	
	T_{CKL}	I2C clock low	1300	-	ns	
	T_{CKH}	I2C clock high	600	-	ns	
I2C_SDA	T_r	I2C data rising time	-	300	ns	
	T_f	I2C data falling time	-	300	ns	
	T_{DatHd}	I2C data hold time	0	900	ns	
	T_{DatSu}	I2C data setup time	100	-	ns	
	T_{StaHd}	I2C start condition hold time	600	-	ns	
	T_{StaSu}	I2C start condition setup time	600	-	ns	
	T_{StpSu}	I2C stop condition setup time	600	-	ns	
	$T_{BusFree}$	I2C bus free time	1300	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB

7.6.4 RGB Interface Characteristics

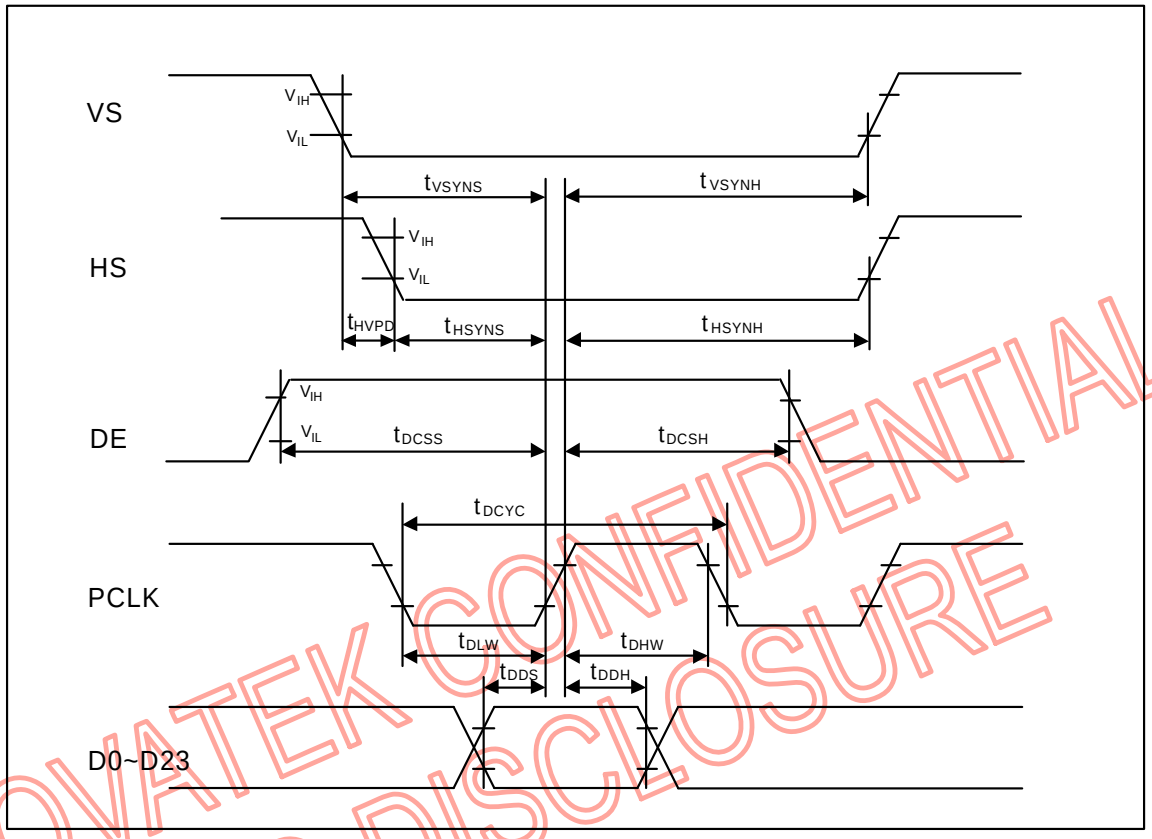


Fig. 7.6.4 RGB interface characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
VS	t_{VSYNS}	VSYNC setup time	10	-	-	ns	
	t_{VSYNH}	VSYNC hold time	10	-	-	ns	
HS	t_{HSYNS}	HSYNC setup time	10	-	-	ns	
	t_{SCYCR}	HSYNC hold time	10	-	-	ns	
	t_{HVPD}	HSYNC to VSYNC falling edge	400	-	-	ns	
PCLK	t_{DCYC}	PCLK cycle time	33	-	125	ns	
	t_{DLW}	PCLK "L" pulse width	11	-	-	ns	
	t_{DHW}	PCLK "H" pulse width	11	-	-	ns	
	f_{DFREQ}	PCLK frequency	8	-	30	MHz	
DE	t_{DCSS}	DE setup time	10	-	-	ns	
	t_{DCSH}	DE hold Time	10	-	-	ns	
D0~D23	t_{DDS}	RGB Data setup time	10	-	-	ns	
	t_{DDH}	RGB Data hold time	10	-	-	ns	

Note 1) VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSS=VSSI=DVSS=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
VDD means VDDA, VDDR, VDDB and VSS means VSSA, VSSR, VSSB
Note 2) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

7.6.5 MIPI DSI Timing Characteristics

7.6.5.1 HIGH SPEED MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	-	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note) Dn = D0 and D1.

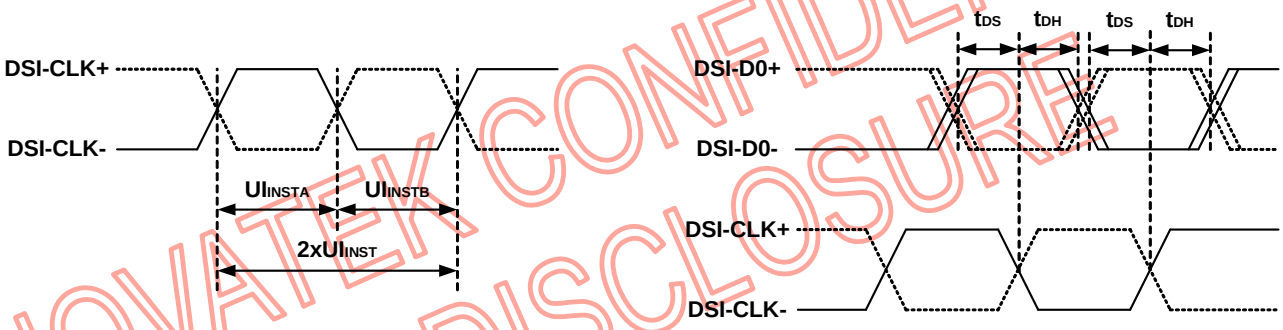


Fig. 7.6.4 DSI clock channel timing

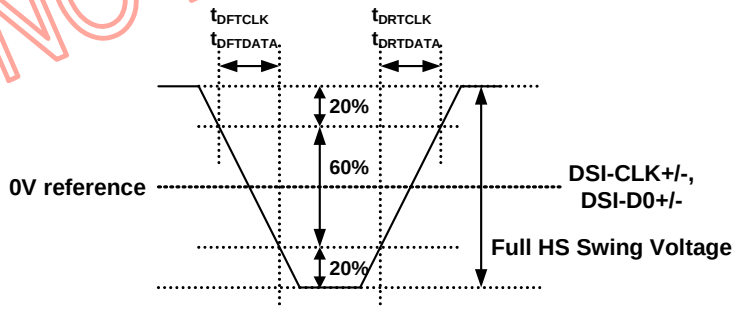


Fig. 7.6.5 Rising and fall time on clock and data channel

7.6.5.2 LOW POWER MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output

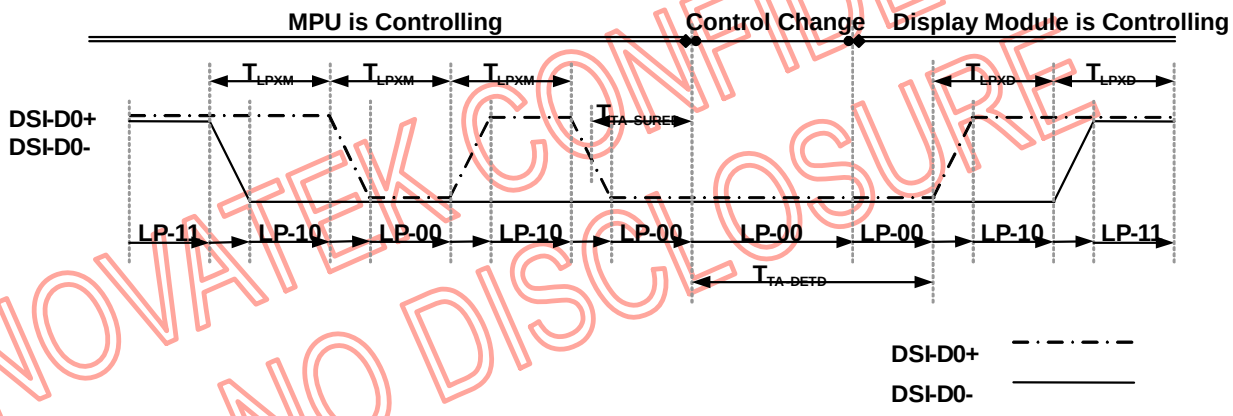


Fig. 7.6.6 Bus Turnaround (BAT) from MPU to display module Timing

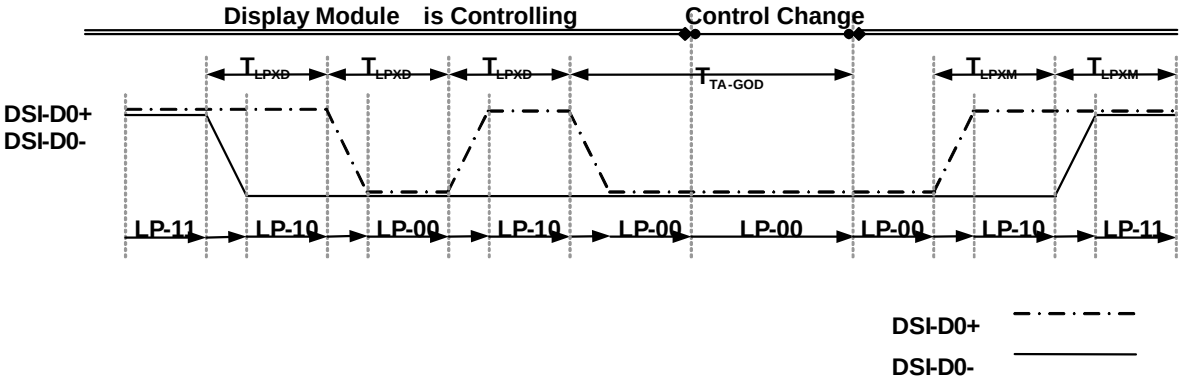


Fig. 7.6.7 Bus Turnaround (BAT) from display module to MPU Timing

7.6.5.3 DSI BURSTS

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note) Dn = D0 and D1.

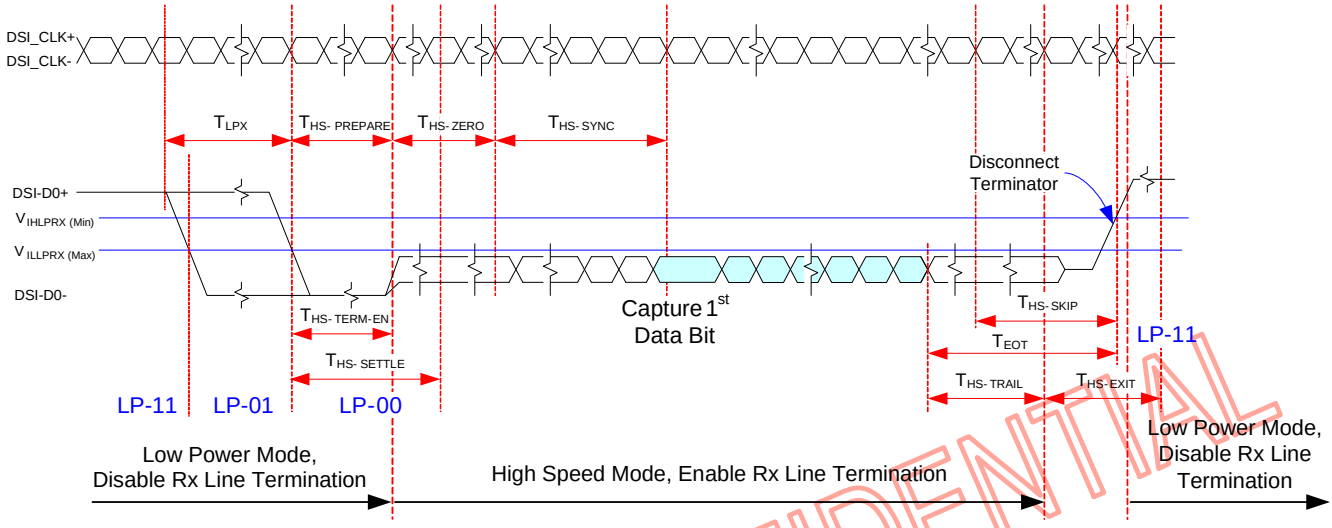


Fig. 7.6.8 Data lanes-Low Power Mode to/from High Speed Mode Timing

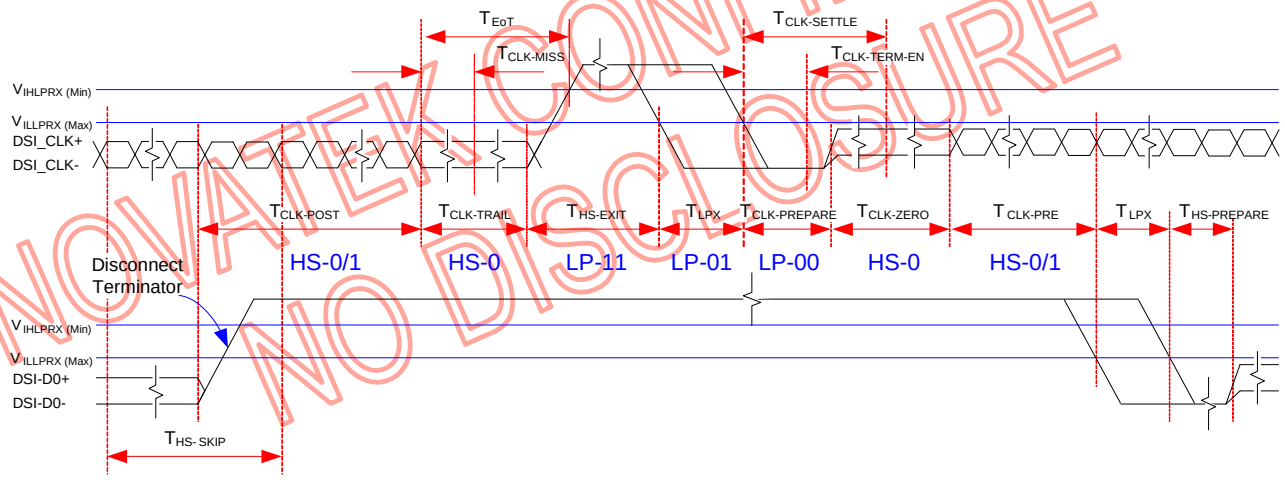


Fig. 7.6.9 Clock lanes- High Speed Mode to/from Low Power Mode Timing

7.6.6 MDDI Timing Characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
MDDI_STB_P/M MDDI_DATA_P/M	1/Tbit	Data transfer rate	-	384	450	Mbps	
MDDI_STB_P/M MDDI_DATA_P/M	|Tskew-pair|	Differential transfer input skew	-	-	0.05	ns	
MDDI_STB_P/M MDDI_DATA_P/M	|Tskew-data|	Data/Strobe input skew	-	-	0.3	ns	

Note) MDDI_DATA_P/M = MDDI_DATA0_P/M and MDDI_DATA1_P/M.

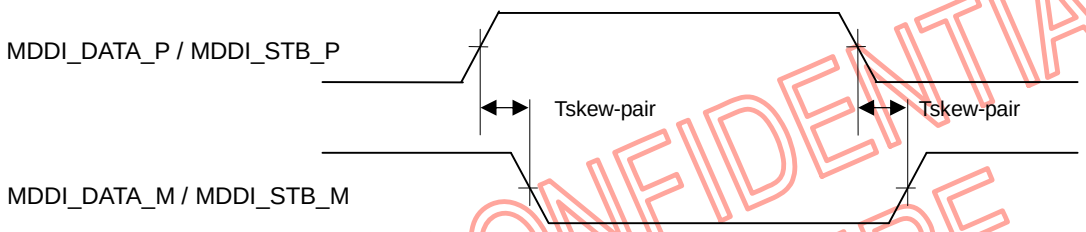


Fig. 7.6.10 Skew between MDDI positive and negative signal pair

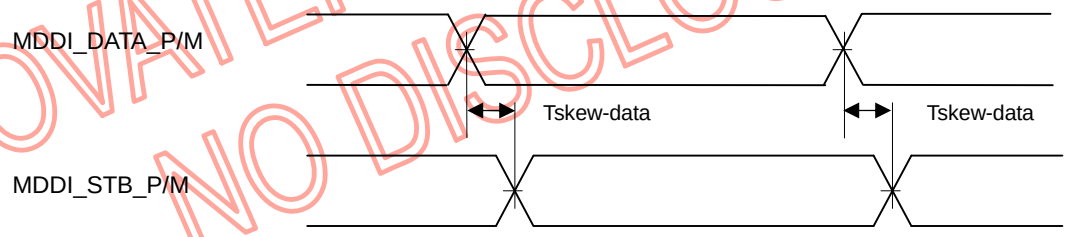


Fig. 7.6.11 Skew between MDDI_DATA_P/M and MDDI_STB_P/M

7.6.7 Reset Input Timing

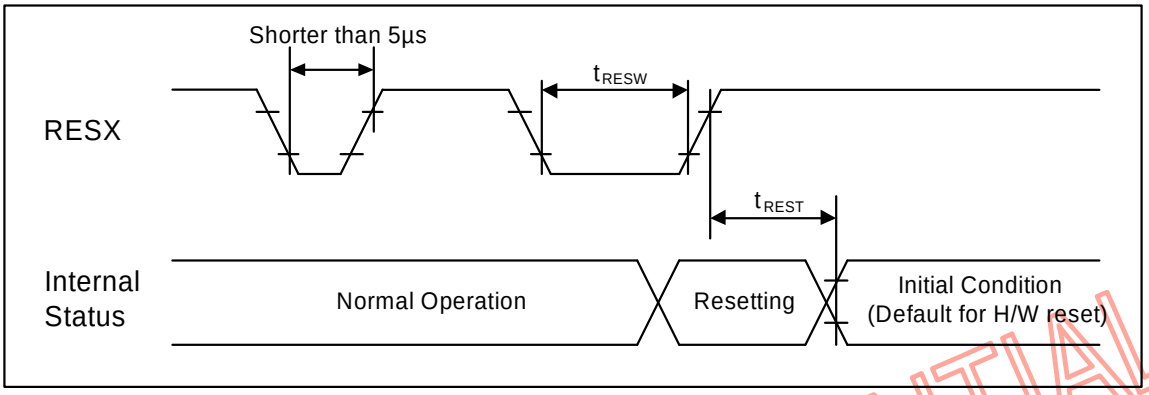


Fig. 7.6.12 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

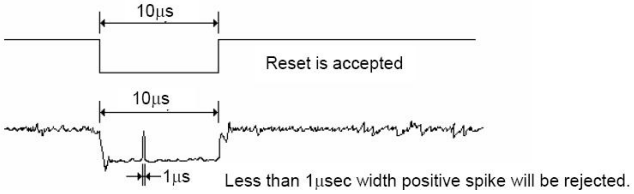
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

8 REFERENCE APPLICATIONS

8.1 Microprocessor Interface

The display, which is using 80-series MPU interface, is connected to the MPU as it is illustrated below.

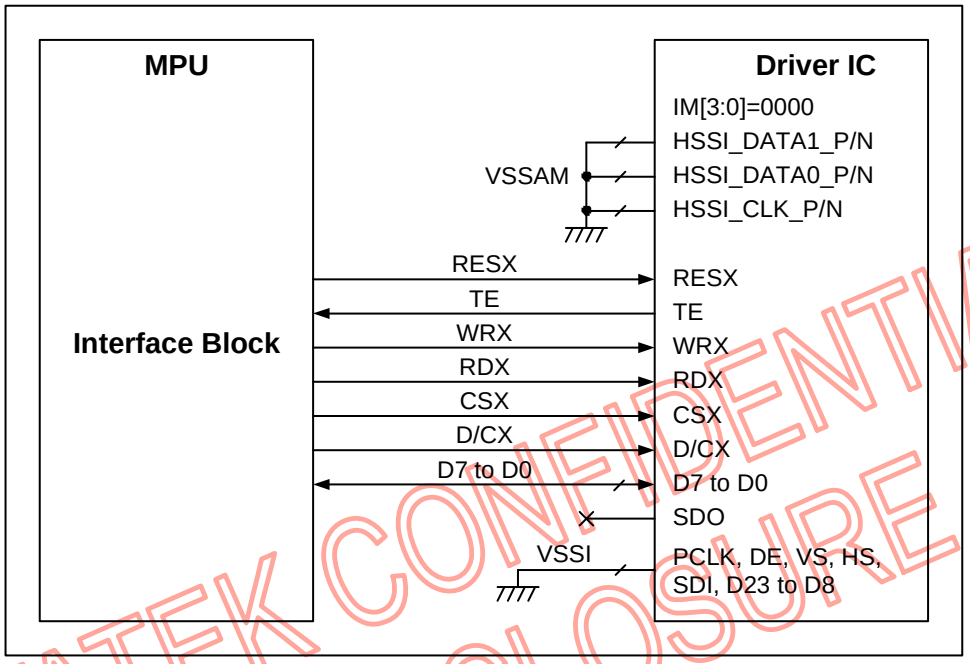


Fig. 8.1.1 Interfacing for 80-series 8-bit MPU by Connecting IM[3:0]="0000"

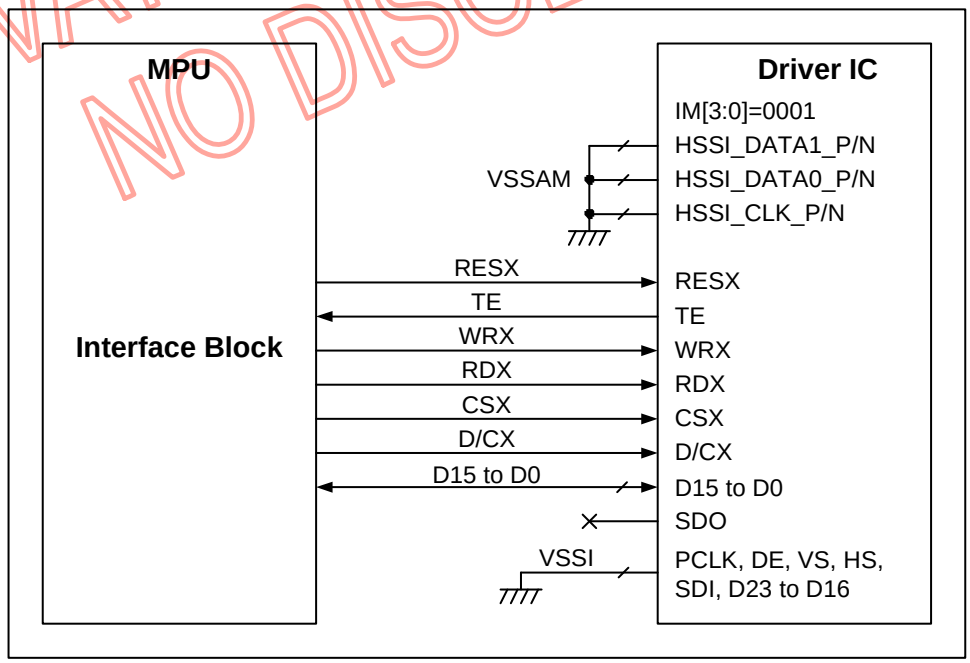


Fig. 8.1.2 Interfacing for 80-series 16-bit MPU by Connecting IM[3:0]="0001"

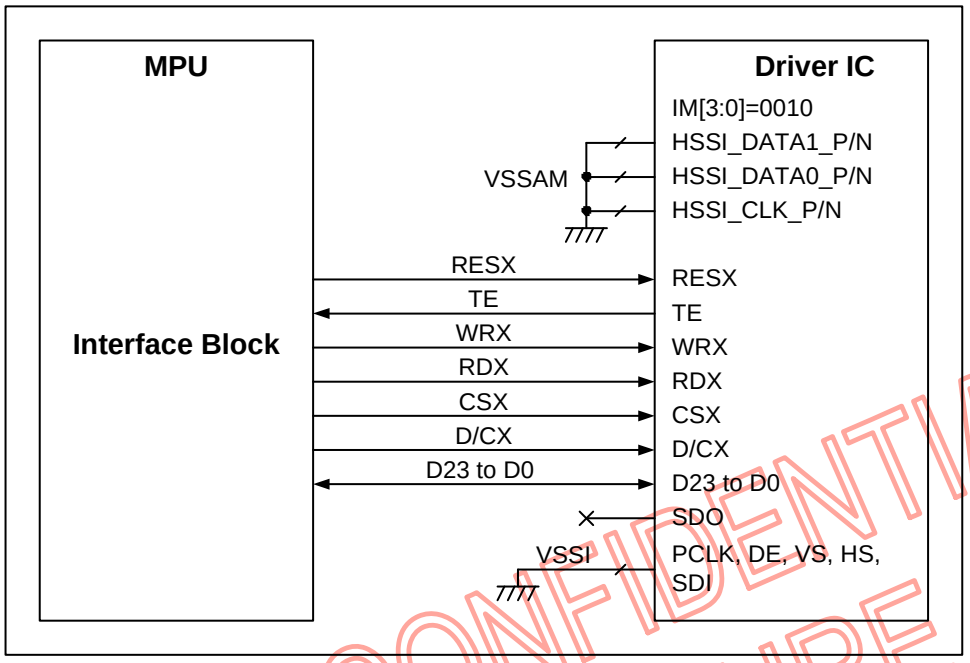


Fig. 8.1.3 Interfacing for 80-series 24-bit MPU by Connecting IM[3:0]="0010"

Note: Left MVDDL and MVDDA open (not used) when using 80-series MPU interface.

The display, which is using RGB with 16-bit SPI interface, is connected to the MPU as it is illustrated below.

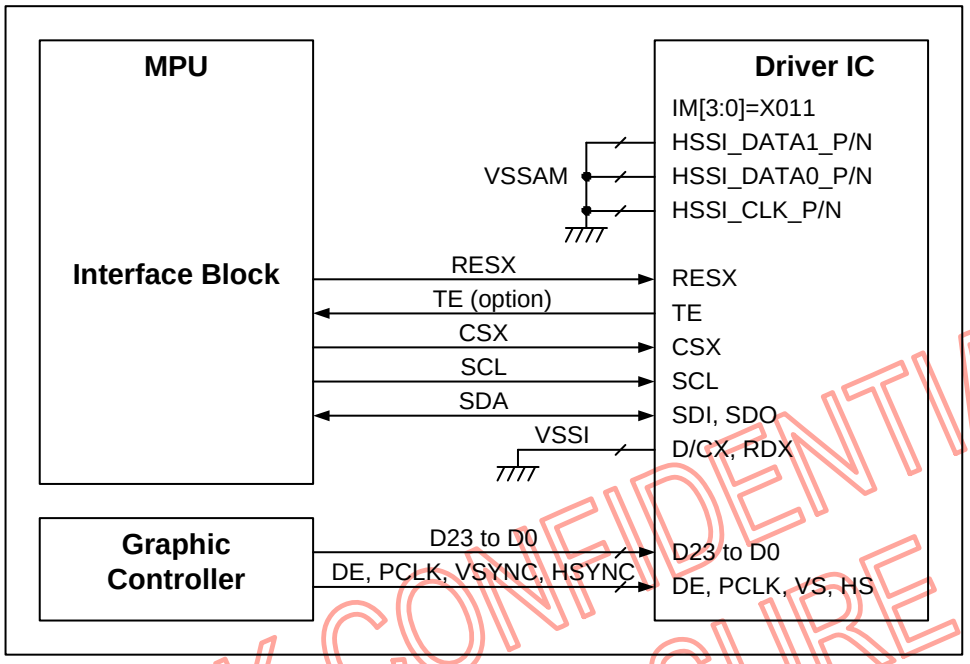


Fig. 8.1.4 Interfacing for RGB with SPI by Connecting IM[3:0]="X011"

The display, which is using RGB with I2C interface, is connected to the MPU as it is illustrated below.

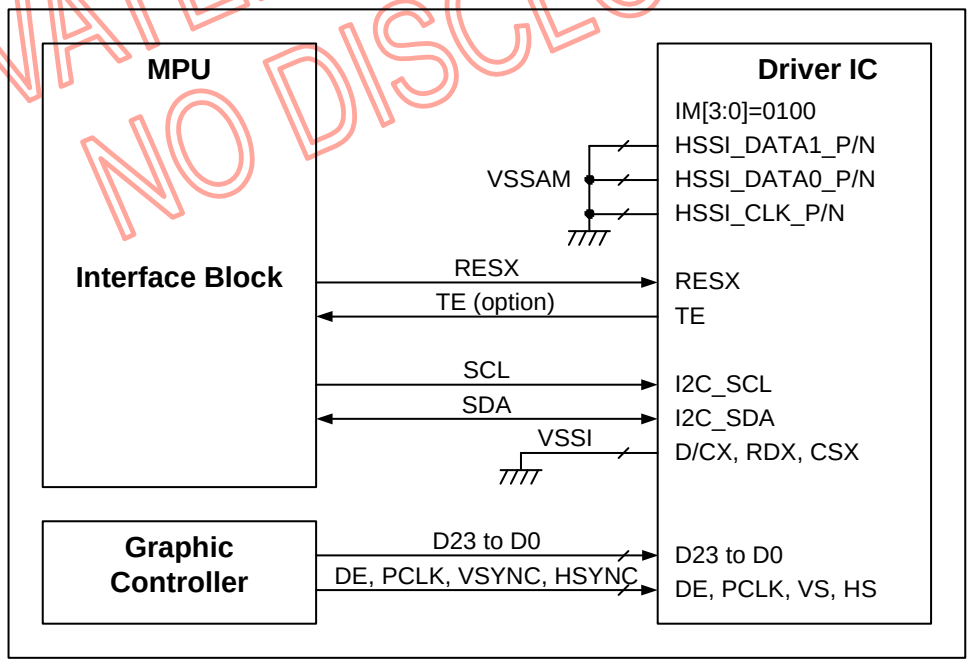


Fig. 8.1.5 Interfacing for RGB with I2C by Connecting IM[3:0]="0100"

Note 1. Connecting D23, D22, D15, D14, D7 and D6 to VSSI when using 18-bit/pixel (VIPF[3:0]="0110").
Connecting D23~D21, D15, D14 and D7~ D5 to VSSI when using 16-bit/pixel (VIPF[3:0]="0101").
Note 2. Left MVDDL and MVDDA open (not used) when using RGB with SPI interface.
Note 3. IM3 is used to select SCL rising or falling edge trigger for 16-bit SPI interface.

The display, which is using MIPI DSI and the TE line, is connected to the MPU as it is illustrated below.

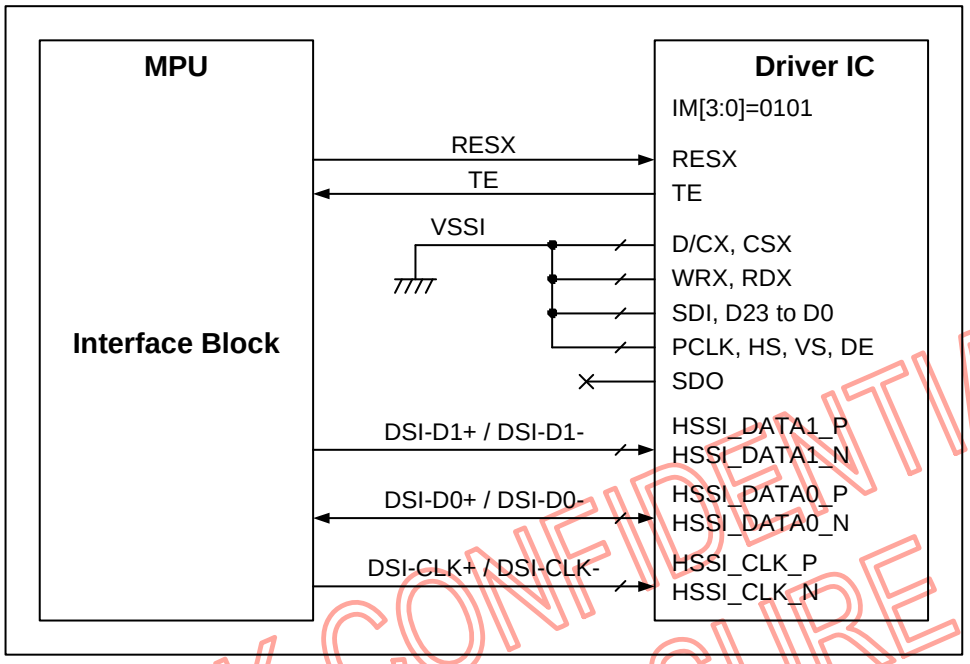


Fig. 8.1.6 Interfacing for MIPI DSI with TE Line by Connecting IM[3:0]="0101"

The display, which is using MIPI DSI without the TE line, is connected to the MPU as it is illustrated below.

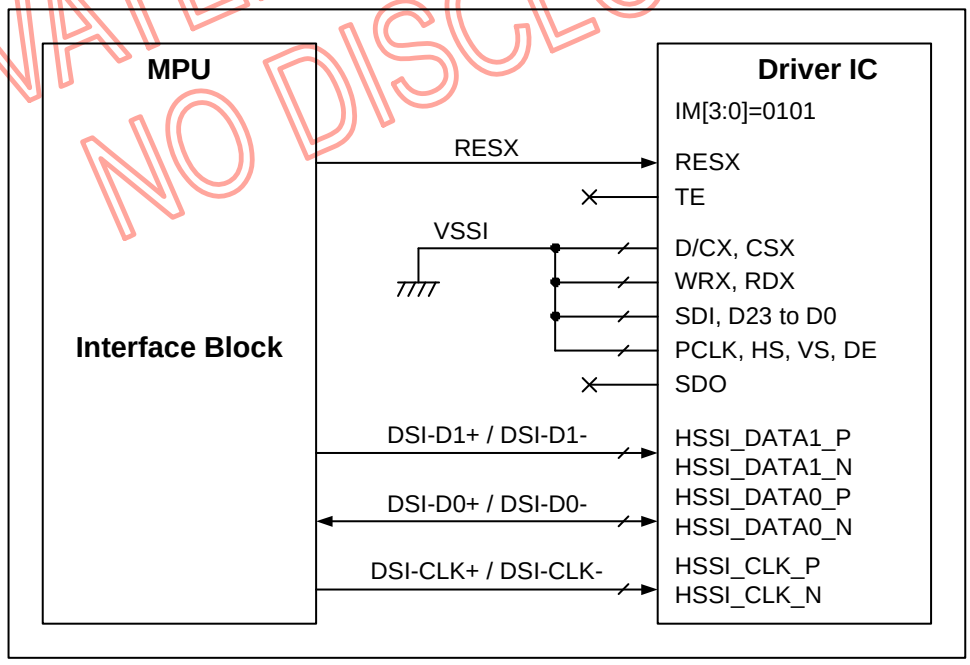


Fig. 8.1.7 Interfacing for MIPI DSI without TE Line by Connecting IM[3:0]="0101"

Note1. Bit DSITE should be "1", the TE line is enabled, when using MIPI with TE line.
Note2. Bit DSITE should be "0", the TE line is disabled, when using MIPI without TE line. The command 35h TEON cannot active the separated TE line.
Note3. Connecting HSSI_DATA1_P/N to VSSAM when using 1 data lane application.

The display, which is using MDDI with 16-bit SPI interface, is connected to the MPU as it is illustrated below.

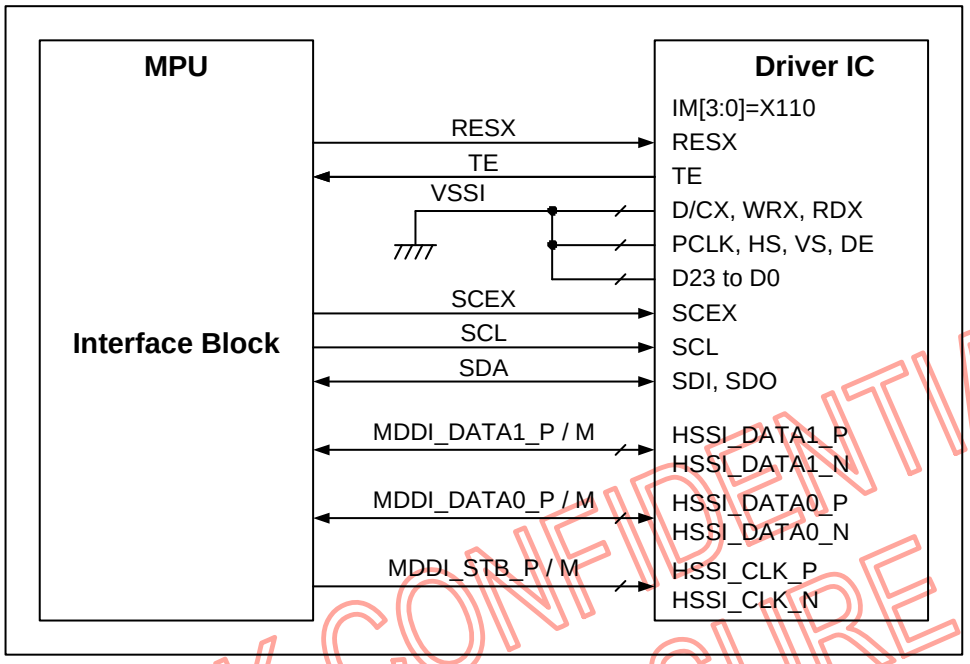


Fig. 8.1.8 Interfacing for MDDI with 16-bit SPI by Connecting IM[3:0]="X110"

The display, which is using MDDI with I2C interface, is connected to the MPU as it is illustrated below.

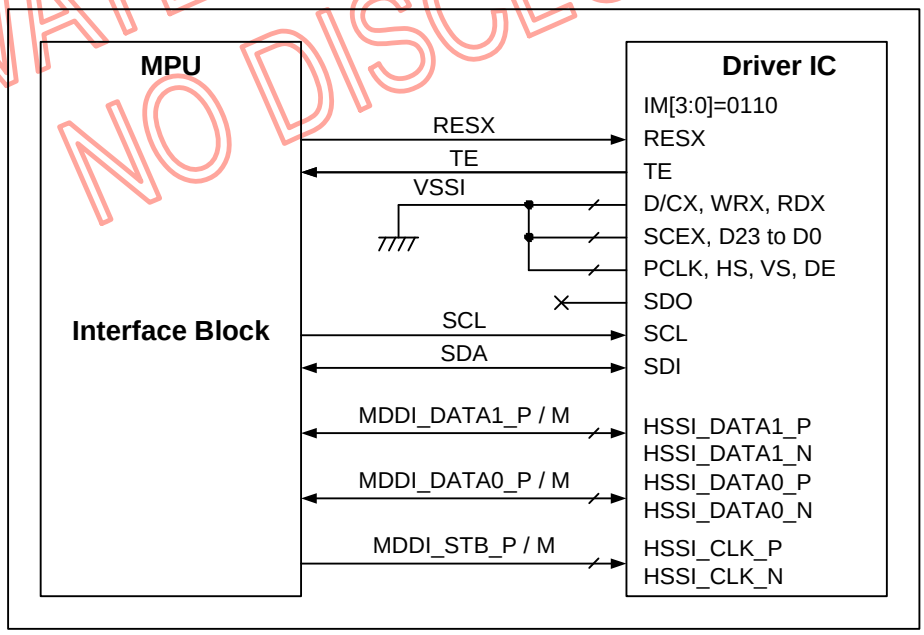


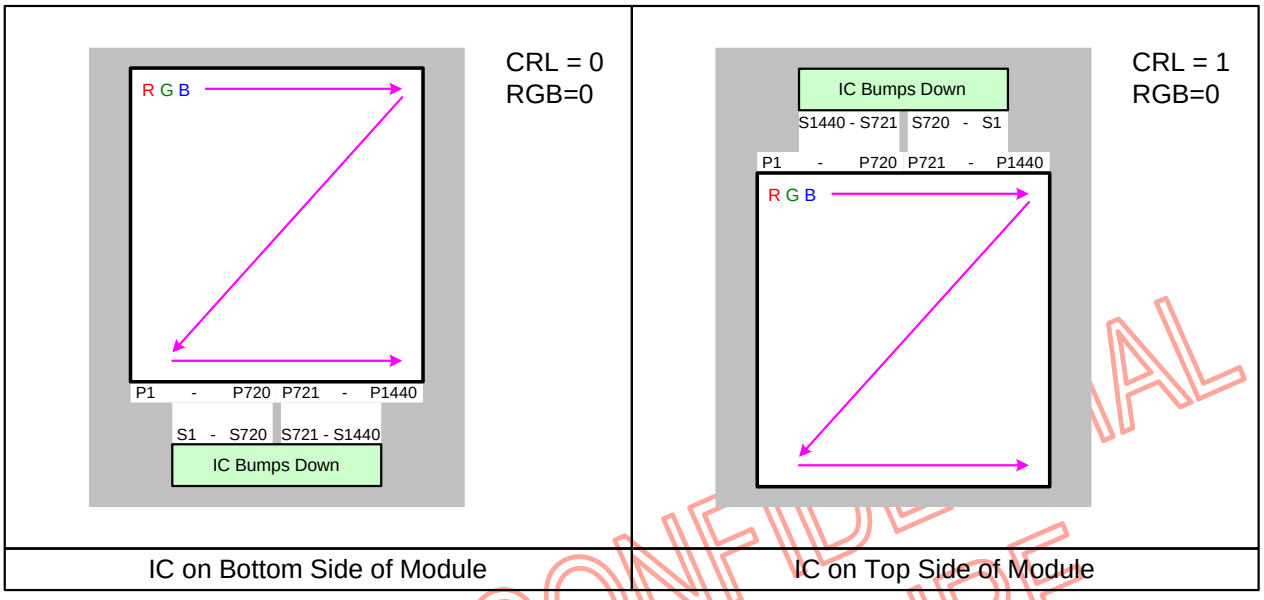
Fig. 8.1.9 Interfacing for MDDI with I2CI by Connecting IM[3:0]="0111"

Notes:

1. Connecting HSSI_DATA1_P/N to VSSAM when using MDDI Type-I (1 data lane).

2. IM3 is used to select SCL rising or falling edge trigger when using 16-bit SPI interface.

8.2 Connections with Panel



IC on Bottom Side of Module | IC on Top Side of Module

NOTES:

1. The scan direction from top to bottom indicated in above figure means (CTB XOR ML = "0").

2. The relationship between Sn output sequence and CRL/CGM[7:0] is shown below.

CGM[7:0]	Display Resolution	Sn Output Sequence	Note
C0h	480RGB x 1024	CRL="0": $S1_{(R)}$→$S2_{(G)}$→$S3_{(B)}$→…→$S1438_{(R)}$→$S1439_{(G)}$→$S1440_{(B)}$ CRL="1": $S1440_{(R)}$→$S1439_{(G)}$→$S1438_{(B)}$→…→$S3_{(R)}$→$S2_{(G)}$→$S1_{(B)}$	All S1 to S1440 are used
70h	480RGB x 864		
6Bh	480RGB x 854		
50h	480RGB x 800		
28h	480RGB x 720		
00h	480RGB x 640		