



Data Sheet

NT35310

**One-chip Driver IC with internal GRAM for 262K colors
320RGB x 480 a-Si TFT LCD with CPU / RGB / MDDI / MIPI
Interface**

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INDEX

REVERSION HISTORY	7
1. GENERAL DESCRIPTION	8
1.1 PURPOSE OF THIS DOCUMENT	8
1.2 GENERAL DESCRIPTION.....	8
2. FEATURES	9
3. BLOCK DIAGRAM	12
4. PIN DESCRIPTIONS	13
4.1 POWER INPUTS	13
4.2 MCU SYSTEM INTERFACE	13
4.3 SPI INTERFACE.....	14
4.4 RGB INTERFACE	14
4.5 MDDI / MIPI INTERFACE.....	15
4.6 CABG CONTROL PINS	15
4.7 INTERFACE LOGIC PINS	16
4.8 DISPLAY DRIVER ANALOG OUTPUTS	17
4.9 POWER SUPPLY	18
4.10 TEST PINS (TEST AND DUMMY PINS)	18
5. FUNCTION DESCRIPTIONS	19
5.1 MPU INTERFACE	19
5.1.1 General Protocol.....	20
5.1.2 80-System Interface.....	20
5.1.2.1 Write cycle sequence.....	21
5.1.2.2 Read Cycle Sequence.....	22
5.2 SPI INTERFACE	23
5.2.1 General Description for LoSSI.....	23
5.2.2 Command Write for LoSSI.....	23
5.2.3 Read Functions for LoSSI.....	23
5.2.4 Display Module Data Transfer Recovery for LoSSI.....	24
5.2.5 Display Module Data Transfer Pause for LoSSI.....	26
5.2.6 Display Module Data Transfer Modes for LoSSI	27
5.2.6.1 Method 1.....	27
5.2.6.2 Method 2.....	27
5.3 DISPLAY DATA RAM (DDRAM)	28
5.3.1 Serial Interface for DATA RAM write	29
5.3.2 8-Bits Parallel Interface for RAM Data Write.....	30
5.3.3 9-Bits Parallel Interface (80-system) for RAM Data Write	32
5.3.4 16-Bits Parallel Interface for RAM Data Write.....	33
5.3.5 18-Bits Parallel Interface for RAM Data Write.....	35
5.3.6 Serial Interface Signals for RAM Data Read	36
5.3.7 80-8-bits Parallel Interface Signals for RAM Data Read	37
5.3.8 80-9-bits Parallel Interface Signals for RAM Data Read	38
5.3.9 80-16-bits Parallel Interface Signals for RAM Data Read	39
5.3.10 80-18-bits Parallel Interface Signals for RAM Data Read.....	40
5.4 RGB INTERFACE	41
5.4.1 General Description.....	41
5.4.2 General Timing Diagram	42
5.4.3 RGB Interface Bus Width Set.....	43
5.4.4 RGB Interface Mode Set.....	44
5.4.5 RGB Interface Mode 1 & Mode 2 Timing Chart	45
5.5 FRAME TEARING EFFECT INTERFACE	48
5.5.1 Tearing Effect Line Modes.....	48
5.5.2 Example 1: MPU write is faster than panel read	51
5.5.3 Example 2: MPU write is slower than panel read	52
5.6 MDDI INTERFACE (MOBILE DISPLAY DIGITAL INTERFACE)	56

5.6.1 MDDI Link Protocol	57
5.6.2 MDDI Link Packet descriptions	57
5.6.3 Writing Video Data to Memory Sequence	67
5.6.4 Writing Register Sequence	67
5.6.5 Reading Video Data from Memory Sequence	68
5.6.6 Reading Register Sequence	68
5.6.7 Hibernation Setting	69
5.6.8 Deep Standby Mode Setting by MDDI	70
5.6.9 Vsync Based Link Wakeup	72
5.7 MIPI INTERFACE (MOBILE INDUSTRY PROCESSING INTERFACE)	73
5.7.1 Display Module Pin Configuration for DSI	74
5.7.2 Display Serial Interface (DSI)	75
5.7.2.1 General Description	75
5.7.2.2 Interface Level Communication	75
5.7.2.2.1 General	75
5.7.2.2.2 DSI-CLOCK Lane	76
5.7.2.2.3 DSI-DATA Lanes	82
5.7.2.3 Packet Level Communication	93
5.7.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structures	93
5.7.2.3.2 Packer Transmission	112
5.7.2.3.3 Communication Sequence	143
5.7.2.4 Video Mode Communication	155
5.7.2.4.1 Transmission Packet Sequences	155
5.7.2.4.2 Non-Burst Mode with Sync Pulses	156
5.7.2.4.3 Non-Burst Mode with Sync Events	157
5.7.2.4.4 Burst Mode	158
5.7.2.4.5 Parameters	158
5.7.2.4.6 Video mode ON/OFF sequence	159
5.7.3 Memory access for DSI	161
5.8 WINDOW ADDRESS FUNCTION	169
5.9 REDUCED POWER CONSUMPTION DRIVE SETTINGS	170
5.10 FRAME-FREQUENCY ADJUSTMENT FUNCTION	170
5.11 GAMMA FUNCTION	171
5.12 RESET FUNCTION	172
5.13 BASIC OPERATION MODE	174
5.14 POWER ON/OFF SEQUENCE	175
5.15 INSTRUCTION SETTING SEQUENCE	176
5.15.1 Sleep SET/EXIT Sequences	176
5.15.2 Deep Standby Mode ENTER/EXIT Sequences	177
5.16 MTP WRITE SEQUENCE	178
5.16.1 First Time MTP Programming Sequence (for all MTP)	179
5.16.2 Second Time MTP Programming Sequence	180
5.16.3 Third Time MTP Programming Sequence (Only for VCOM, ID and WRDDB)	181
5.16.4 Fourth Time MTP Programming Sequence (Only for VCOM, ID and WRDDB)	182
5.17 INSTRUCTION SETUP FLOW	183
5.17.1 Initializing with the Build-in Power Supply Circuit	183
5.17.2 Power Off Sequence	184
5.18 SLEEP OUT-COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE	185
6. COMMAND DESCRIPTIONS	187
6.1 USER COMMAND SET (COMMAND 1)	189
NOP (00h): No Operation	191
SOFT_RESET (01h): Software Reset	192
RDID (04h): Read Display ID	193
RDNUMED (05h): Read Number of the Errors on DSI	194
GET_POWER_MODE (0Ah): Read Display Power Mode	195
GET_ADDRESS_MODE (0Bh): Get the Frame Memory to the Display Panel Read Order	196
GET_PIXEL_MODE (0Ch): Read Input Pixel Format	197
GET_DISPLAY_MODE (0Dh): Read the Current Display Mode	198
GET_SIGNAL_MODE (0Eh): Get Display Module Signaling Mode	199
RDDSDR (0Fh): Read Display Self-Diagnostic Result	200
ENTER_SLEEP_MODE (10h): Enter the Sleep-In Mode	201

<i>EXIT_SLEEP_MODE (11h): Exit the Sleep-In Mode</i>	202
<i>ENTER_PARTIAL_MODE (12h): Partial Display Mode On</i>	203
<i>ENTER_NORMAL_MODE (13h): Normal Display Mode On</i>	204
<i>EXIT_INVERT_MODE (20h): Display Inversion Off</i>	205
<i>ENTER_INVERT_MODE (21h): Display Inversion On</i>	206
<i>ALLPOFF (22h): All Pixel Off</i>	207
<i>ALLPON (23h): All Pixel On</i>	208
<i>GMASET (26h): Gamma Curves Selection</i>	209
<i>SET_DISPLAY_OFF (28h): Display Off</i>	210
<i>SET_DISPLAY_ON (29h): Display On</i>	211
<i>SET_HORIZONTAL_ADDRESS (2Ah): Set the Column Address</i>	212
<i>SET_VERTICAL_ADDRESS (2Bh): Set Page Address</i>	214
<i>WRITE_MEMORY_START (2Ch): Memory Write Start Command</i>	216
<i>SET_MDDI_RAM_READ_ADDRESS (2Dh): Set the RAM Horizontal and Vertical Address</i>	217
<i>READ_MEMORY_START (2Eh): Memory Read Start Command</i>	218
<i>SET_PARTIAL_AREA (30h): Defines the Partial Display Area</i>	220
<i>SCRLAR (33h): Set Scroll Area</i>	222
<i>SET_TEAR_ON (35h): Tearing Effect Line ON</i>	226
<i>SET_ADDRESS_MODE (36h): Memory Data Access Control</i>	228
<i>VSCSAD (37h): Vertical Scroll Start Address of RAM</i>	231
<i>EXIT_IDLE_MODE (38h): Idle Mode Off</i>	233
<i>ENTER_IDLE_MODE (39h): Idle Mode On</i>	234
<i>SET_PIXEL_FORMAT (3Ah): Set the Interface Pixel Format</i>	236
<i>RGBCTRL (3Bh): RGB Interface Signal Control</i>	237
<i>RAMWRC (3Ch): Memory Write Continuously</i>	240
<i>RAMRDC (3Eh) : RAM Read Continuously</i>	241
<i>SET_TEAR_SCANLINE (44h): Set Tear Line</i>	242
<i>RDSCL (45h) : Read Scan Line</i>	244
<i>ENTER_DSTB_MODE (4Fh): Enter the Deep Standby Mode</i>	245
<i>WRDISBV (51h): Write Display Brightness</i>	246
<i>RDDISBV (52h): Read Display Brightness</i>	247
<i>WRCTRLD (53h): Write CTRL Display</i>	248
<i>RDCTRLD (54h): Read CTRL Display</i>	250
<i>WRCTRLD (55h): Write CTRL Display</i>	251
<i>RDCABC (56h): Read Content Adaptive Brightness Control (CABC) Mode</i>	252
<i>RDCABCMB (5Fh): Read CABC Minimum Brightness</i>	254
<i>RDDSDR (68h): Read Display Self-Diagnostic Result</i>	255
<i>SET_MDDI (8Fh)</i>	256
<i>RDDDBS (A1h): Read DDB Start</i>	257
<i>RDDDBC (A8h): Read DDB Continue</i>	258
<i>RDFCS (AAh): Read First Checksum</i>	259
<i>MDDI_WAKE_TOGGLE (ADh): MDDI VSYNC BASED LINK WAKE-UP</i>	260
<i>STB_EDGE_POSITION (AEh)</i>	261
<i>RDCCS (AFh): Read Continue Checksum</i>	263
<i>RDID1 (DAh): Read ID1</i>	264
<i>RDID2 (DBh): Read ID2</i>	265
<i>RDID3 (DCh): Read ID3</i>	266
<i>IDLEMODE_BL_Control (E1h): Write IDLEMODE_BL_Control</i>	267
<i>IDLEMODE_BL_Control (E2h): Read IDLEMODE_BL_Control</i>	269
<i>PAGE_CTRL (EDh) : Unlock CMD2</i>	270
<i>PAGE_STATUS (FFh) : PAGE unlock status</i>	272
6.2 CMD2_P0 REGISTER LIST	273
<i>RDREGEXT1</i>	274
<i>DISPLAY_CTRL (B0h)</i>	275
<i>PORCH_CTRL: Front & Back Porch Setting (B1h)</i>	277
<i>FRAMERATE_CTRL (B2h)</i>	279
<i>SPI&RGB IF SETTING (B3h): SPI&RGB INTERFACE SETTING</i>	282
<i>INVCTRL (B4h): Inversion Control</i>	283
<i>PMTCTL (B5h) : Partial and Idle Mode Timing Control</i>	284
<i>DISPLAY_CTRL_NORM (B6h)</i>	286

<i>DISPLAY_CTRL2: Set the States for LED Control (B7h)</i>	288
<i>MTP Selection (B8h)</i>	289
<i>PWR_CTRL1 (C0h)</i>	290
<i>PWR_CTRL2 (C1h)</i>	297
<i>PWR_CTRL3 (C2h)</i>	299
<i>PWR_CTRL5 (C3h)</i>	300
<i>PWR_CTRL6 (C4h)</i>	301
<i>PWR_CTRL7 (C5h)</i>	303
<i>PWR_CTRL8 (C6h)</i>	305
<i>WID_CTRL1 (D1h): WID1</i>	307
<i>WID_CTRL2 (D2h): WID2</i>	308
<i>WID_CTRL3 (D3h): WID3</i>	309
<i>READID4 (D4h): Read ID4</i>	310
<i>DDB_CTRL (D5h) : Write DDB Info</i>	311
<i>RDVNT (DDh): Read NV Memory Flag Status</i>	312
<i>EPWRITE (DEh): NV Memory Write Command</i>	313
<i>MTPPW (DFh): MTP Write function enable</i>	314
<i>RDREGEXT1 (EBh) : Register read command in SPI interface</i>	315
<i>RDREGEXT2 (ECh) : Register read command in SPI interface</i>	316
<i>PAGE_LOCK (EFh) : Set the Register to command1</i>	317
<i>PAGE_LOCK (BFh) : Set the Register to command2 Page 1</i>	318
6.3 CMD2_P1 REGISTER LIST	319
<i>3GAMMAR_CTRL_RED_P (E0h)</i>	326
<i>3GAMMAR_CTRL_RED_N (E1h)</i>	328
<i>3GAMMAR_CTRL_GREEN_P (E2h)</i>	330
<i>3GAMMAR_CTRL_GREEN_N (E3h)</i>	332
<i>3GAMMAR_CTRL_BLUE_P (E4h)</i>	334
<i>3GAMMAR_CTRL_BLUE_N (E5h)</i>	336
<i>CABC GAMMA offset (E6h)</i>	338
<i>CABC GAMMA offset (E7h)</i>	340
<i>CABC GAMMA offset (E8h)</i>	342
<i>PAGE_LOCK (00h) : Set the Register to command2 Page 0</i>	344
7. ELECTRICAL CHARACTERISTICS	345
7.1 ABSOLUTE MAXIMUM RATINGS	345
7.2 DC CHARACTERISTICS	346
7.2.1 Basic Characteristics.....	346
7.2.2 Current Consumption.....	347
7.2.3 MDDI DC Characteristics.....	347
7.2.4 MIPI DC Characteristics.....	348
7.3 AC CHARACTERISTICS	349
7.3.1 80-System Bus Interface Timing Characteristics (16-/8-bits Transfer Mode).....	349
7.3.2 80-System Bus Interface Timing Characteristics (1 transfer per pixel).....	350
7.3.3 80-System Bus Interface Timing Characteristics (2 or 3 transfer per pixel).....	350
7.3.4 MDDI Interface Characteristics.....	353
7.3.5 MIPI Interface Characteristics.....	354
7.3.6 RGB Interface Characteristics.....	358
7.3.7 Reset Timing Characteristics.....	359
7.3.15 Liquid Crystal Driver Output Characteristics.....	360
8.1 CONNECT EXAMPLE WITH EXTERNAL COMPONENTS	363
8.2 POWER SCHEME	365
8.3 MAXIMUM SERIES RESISTANCE	366
9. CHIP INFORMATION	367
9.1 CHIP INFORMATION	367
9.1.1 CHIP OVERVIEW.....	367
9.1.2 APPLICATION CIRCUIT.....	368
9.2 BUMP INFORMATION	370
9.2.1 Input PAD Format.....	370

9.2.2 Output PAD Fotmat.....	371
9.2.3 Alignment Mark Information.....	372
9.3 PAD COORDINATES	373
9.3.1 For Panel Resolution: 320(RGB)*480	373

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Reversion History

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	- Initial Version	Connie	Charley Max		2011/11/04
0.01	<ul style="list-style-type: none"> - Modified MTP 1time(page 10, 182 ,184) - Modified DCX Pad type (page16) - Modified TE1/IDLE_ON description(page 18) - Modified VGL description (page 20) - Modified MIPI command table (page 108) - Modified RTN description(page 174) - Add SRE in 55h&56h (page 255-257) - SET_MIPI_MDDI change address to 8Fh (page192, 277) - Add STB EDGE TIMING CTRL(AEh) (page 192,284) - Add IDLEMODE_BL Control(E1,E2h) (page 192,290,291) - Add WRALS(E3h)(page 194, 292) - Add RDALS(E4h)(page 194, 293) - Change switch page flow, add command2_P0,commandP1(page 294~296) - Add command2_P0 table (page297) - Modified B2h default value, min RTN=123 (page 304,305) - Add LPM_HZ &TE1_ON of B3h (page 307) - Modified interval scan for B5h (page 309) - Add SDT & EQI of B6h (page 311) - Add VGSP & VGSN of C0h (page321-327) - Modified C2h VGL pump setting (page 329) - Change sunlight Hystersis Curve to command2_P0 of E0h (page 346) - Add command2_P0 table (page351) - Add setting gamma command (page 359-376) - Modified DC Characteristics follow nokia spec (page 378) - Remove 70~7Eh - Add CVSS - Remove B8h's SMX,SMY - Modified 36h note description. (page 233) - Add VGH&VGL clamp command of C6h(page 320) - Modified 3Bh default value. - Add gamma default value. 	Connie	Charley		2011/12/12
0.02	<ul style="list-style-type: none"> - Add 8-8-8 format for MIPI interface (page133,162~165) - Modified B1h default value.(page273,277) - Modified Command2_P0 register table(page273~274) - Modified Command2_P1 register table(page.319~325) - Add MDDI IF 8-8-8 format(page65,66) - Modify SPI IF SDA pin description(page14) - Modify MTP Flow(page178~182) - Modify components table(page 361~ 364) - Modify application circuit(pag 368,369) - Modify 7.2.4MIPI DC characteristics voltage(page 348) - Add Differential input voltage in 7.1Absolute Maximum Ratings(page 345) - Add TESTM,OSC test pin in 4.10 Test Pins description (page 18) -Modify A1h parameter and description(page190, 257) -Modify A8h parameter and description(page 190,258) -Remove SRE in 55h and 56h(page251,252) -Modify D5h parameter(page274, 311) -Modify case1&case2 components table(page361,362) 	Connie	Charley		2012/02/09

1. General Description

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35310. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

NT35310 is a single chip low power LCD controller/driver for 262K color a-Si TFT-LCD -LCD displays of 480 gates and 320xRGB columns. It has a 345600 bytes display RAM and a full set of control functions.

The NT35310 supports Mobile Display Digital Interface (MDDI), MIPI Interface, RGB interface, 8/9/16/18-bits 80 system interfaces and serial peripheral interfaces (SPI) interface. The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The NT35310 is also able to make gamma correction settings separately for RGB dots to allow adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 320-RGB x 480-dot 262K-color images, as well as internal boosters that generate the LCD driving voltage, breeder resistance and voltage follower circuit for the LCD driver. A deep standby mode is also supported for lower power consumption.

The NT35310 also supports CABC function for the backlight control. It's able to reduce the total power consumption of display module significantly.

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2. Features

- Single chip a-Si TFT LCD driver-TFT-LCD Controller/ driver with Display RAM.
- **Display Resolutions**
 - 320RGB x 480 (HVGA)
- **Display Data Memory: 345600 bytes.**
- **Display Modes**
 - Full color: 262K-colors
 - Reduced color: 65K-colors
 - Idle mode: 8-colors
- **Interfaces**
 - 8-bits, 9-bits, 16-bits or 18-bits interfaces with 80-series MPU
 - Serial Peripheral Interface (SPI)
 - 16-bits, 18-bits RGB interface
 - Mobile Display Digital Interface (MDDI 1.2 Type-1)
 - MIPI DSI Interface (D-PHY: V1.00.00 , DSI:1.01.00 R11, DCS:1.01.00, 1 data lane)
- **Display Features**
 - High-speed RAM write function
 - Window address functions for specifying a rectangular area on the internal RAM to write data
 - Individual gamma correction setting for RGB dots
 - Deep standby function.

- **On chip**
 - DC/DC converter
 - VCOM voltage generator (Dot inversion)
 - Provide MTP (1 times) to store related Power and gamma setting related registers
 - Provide MTP (4 times) to store VCOM, ID1, ID2 and ID3.
 - Oscillator for display clock generation
 - On module checksums checking
 - Image Enhancement Technology

- **Content Adaptive Backlight Control (CABC) Function**
 - Histogram analysis & data process
 - Moving picture auto-detect mode.
 - Dimming control.
 - Supported in full display mode.

- **Driving Algorithm**
 - Support 1 dot inversion, 2 dot inversion, 4 dot inversion, column inversion driving.

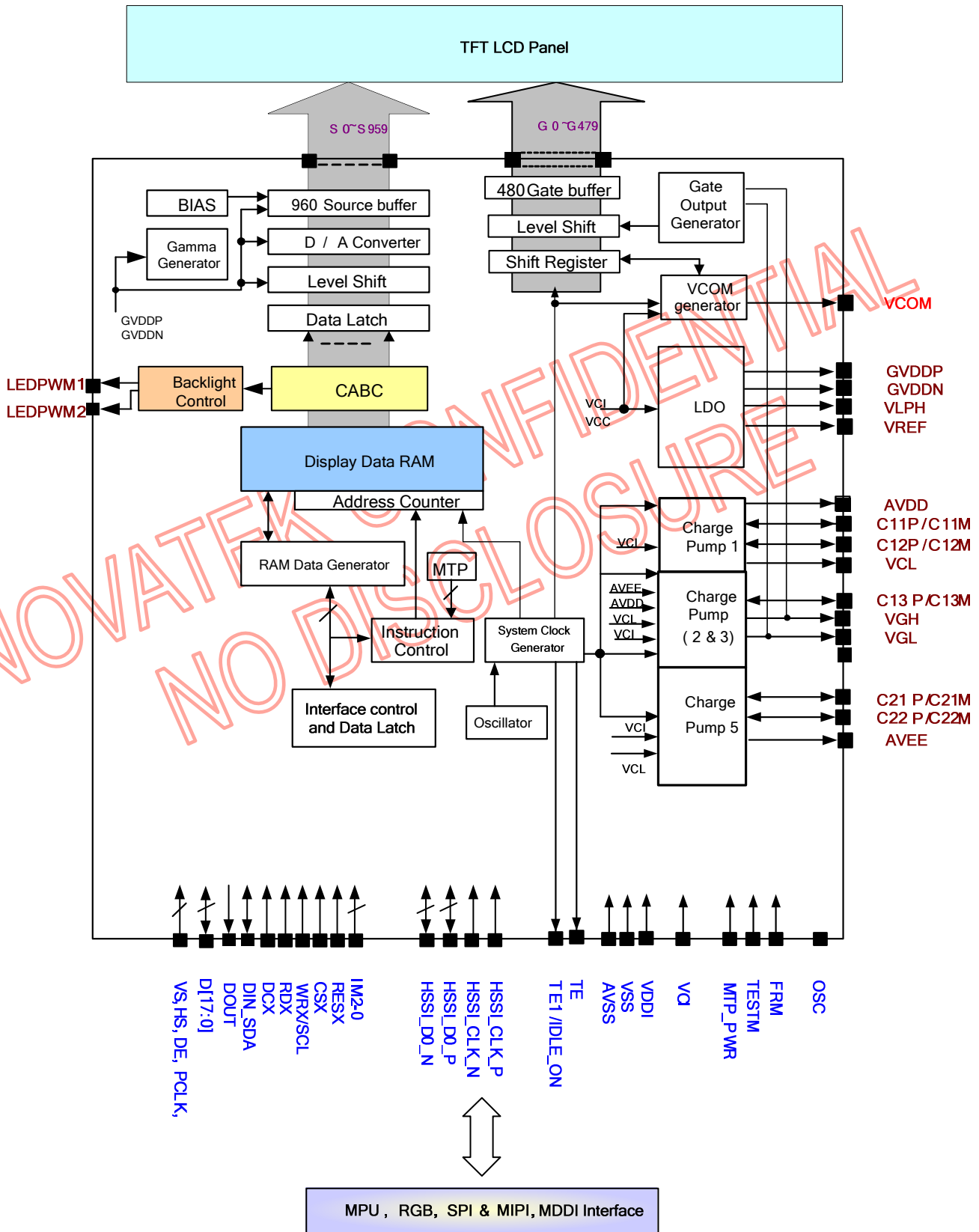
- **Supply Voltage Range**
 - I/O supply voltage range for VDDI to VSS: 1.65V to 3.3 V
 - Analog supply voltage range VCI to AVSS: 2.3V to 3.3 V

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- **Output Voltage Level**

- Positive Power supply for driver circuit range(AVDD): $AVDD-AVSS = 2 \times VCI, 3 \times VCI$
- Negative Power supply for driver circuit range(AVEE): $AVEE-AVSS = -AVDD$
- Positive polarity Source output high voltage level: $GVDDP = 3V \text{ to } 5.5V$ (12.5mV/step , $AVDD-GVDDP > 0.25V$)
- Negative polarity Source output high voltage level: $GVDDN = -3V \text{ to } -5.5V$ (12.5mV/step , $AVEE-GVDDN < -0.25V$)
- Common electrode output voltage level: $VCOM = 0V, -0.2V \text{ to } -3V$ (12.5mV/step , $AVEE-VCOMDC < -0.25V$)
- Positive gate driver output voltage level: $VGH-AVSS = 11V \text{ to } 18V$ ($VCI \times 4, \times 5, \times 6$)
- Negative gate driver output voltage level: $VGL-AVSS = -18V \text{ to } -7.5V$ ($-VCI \times 3, \times 4, \times 5, \times 6$)

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3. Block Diagram

Figure 3.1 Block Diagram

4. Pin Descriptions

4.1 Power Inputs

Symbol	Pad Type	Description
VCI	Power Supply	Power supply to the liquid crystal power supply analog circuit. Connect VCI to an external power supply (VCI = 2.3V to 3.3).
VDDI	Power Supply	Power supply to the I/O. VDDI = 1.65V to 3.3V.
VLPH	LDO Output	LDO output for MIPI TX use (LPDT). Connect a capacitor to stabilize output voltage. Leave it open if MIPI interface is not used.
VSS	Power Ground	Ground for the digital logic. VSS = 0V
AVSS	Power Ground	Ground for the analog unit (regulator, liquid crystal power supply circuit). AVSS = 0V. In case of COG, connect AVSS to VSS on the FPC to prevent noise.
CVSS	Power Ground	Ground for Charge pump. Please connect to VSS.
MTP_PWR	Power input	-Input power for NV memory programming. -Input power range: 7.5V -When not under programming, MTP_PWR pin can be floating or tied to ground.

4.2 MCU System Interface

Symbol	Pad Type	Description
DCX	Digital Input (VDDI)	Data or Command selection pin in MCU parallel interface Low: Index register High: Control register If not used, please pull it to VDDI.
WRX/ SCL	Digital Input (VDDI)	-Writes strobe signal to write data when WRX is Low in CPU system bus interface operation . -Read or write operation in CPU system bus interface. -If not used, please pull it to VDDI.
RDX	Digital Input (VDDI)	-Reads strobe signal to read out data when RDX is Low in 80-system bus interface operation. -Read or write operation in CPU system bus interface. -If not used, please pull it to VDDI.
CSX	Digital Input (VDDI)	Chip select input pin of NT35310. Low: Selected (accessible) High: Unselected (not accessible) If not used, please pull it to VDDI.
D0 to D17	Digital I/O (VDDI)	-18-bits bi-directional data bus for CPU system interface. -8-bits interface: D7-0 are used (Un-used pin should connect to VSS level.) -9-bits interface: D8-0 are used (Un-used pin should connect to VSS level.) -16-bits interface: D15-0 are used (Un-used pin should connect to VSS level.)

4.3 SPI Interface

Symbol	Pad Type	Description
CSX	Digital Input (VDDI)	Chip select input pin of NT35310. Low: Selected (accessible) High: Unselected (not accessible) If not used, please pull it to VDDI.
WRX/SCL	Digital Input (VDDI)	-WRX: Write enable in the 8080-MCU parallel interface operation. -SCL: A synchronous clock signal in serial interface operation.
DIN_SDA	Digital I/O (VDDI)	Serial input signal in serial I/F mode. Note 1 : If not in use, please fix this pin at VSS level.
DOUT	Digital Output (VDDI)	Serial data output. If SDA_EN=0, DOUT is not use. If SDA_EN=1, DOUT is serial data output. Let it to open in MPU interface mode.
DCX	Digital Input (VDDI)	Used in 8-bits SPI for Data / Command Selection pin If not used, please fix this pin at VDDI level.

4.4 RGB Interface

Symbol	Pad Type	Description
DE	Digital Input (VDDI)	Data enable signal in RGB I/F mode. If not used, please fix this pin at VSS level.
PCLK	Digital Input (VDDI)	Pixel clock signal in RGB I/F mode If not used, please fix this pin at VSS level.
HS	Digital Input (VDDI)	Horizontal sync. signal in RGB I/F mode If not used, please fix this pin at VDDI level.
VS	Digital Output (VDDI)	Vertical sync. signal in RGB I/F mode. If not used, please fix this pin at VDDI level.
D0~ D17	Digital Output (VDDI)	18-bits data bus for RGB I/F mode. Data bus is share with 80 -system interface. If not used, please fix this pin at VSS level.

4.5 MDDI / MIPI Interface

Symbol	Pad Type	Description
HSSI_CLK_P/N	MDDI / MIPI Input	-STB+/- signal line in MDDI I/F or DSI_CLK+/- in MIPI I/F. -HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -Please pull it to VSS level if NOT used.
HSSI_D0_P/N	MDDI / MIPI Input/Output	-MDDI / MIPI positive and negative data signal line. -HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -Please pull it to VSS level if NOT used.

4.6 CAB Control Pins

Symbol	Pad Type	Description
LEDPWM1 LEDPWM 2	Digital Output (VDDI –VSS or Hi-Z)	This pin is connected to the external LED driver - PWM type control signal for brightness of the LED backlight - The width of this LEDPWM signal is set from 256 values between 0% (LOW) and 100% (HIGH) - This pin can be set to Hi-impedance output by LEDPWM_OEB bits. -If not used, please open this pin

4.7 Interface Logic Pins

Symbol	Pad Type	Description																																																						
IM2-0	Digital Input (VDDI)	Selects the interface to MPU (VDDI-VSS amplitude signal).																																																						
		<table border="1"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>Interface Selection</th> <th>Data Pins</th> <th>Available Colors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>80-system, 18-bits interface</td> <td>D17-0</td> <td>262k</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>80-system, 9-bits interface</td> <td>D8-0</td> <td>262k</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>80-system, 16-bits interface</td> <td>D15-0</td> <td>65k, 262k</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>80-system, 8-bits interface</td> <td>D7-0</td> <td>65k, 262k</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>MDDI+ 9bits serial interface</td> <td>HSSI_D0_P/N</td> <td>65k, 262k</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>9bits serial interface+ RGB interface</td> <td>DIN_SDA,DOUT</td> <td>65k, 262k</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>MIPI</td> <td>HSSI_D0_P/N</td> <td>65k, 262k</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8bits serial interface+ RGB interface</td> <td>DIN_SDA, DOUT,DCX</td> <td>65k, 262k</td> </tr> </tbody> </table>	IM2	IM1	IM0	Interface Selection	Data Pins	Available Colors	0	0	0	80-system, 18-bits interface	D17-0	262k	0	0	1	80-system, 9-bits interface	D8-0	262k	0	1	0	80-system, 16-bits interface	D15-0	65k, 262k	0	1	1	80-system, 8-bits interface	D7-0	65k, 262k	1	0	0	MDDI+ 9bits serial interface	HSSI_D0_P/N	65k, 262k	1	0	1	9bits serial interface+ RGB interface	DIN_SDA,DOUT	65k, 262k	1	1	0	MIPI	HSSI_D0_P/N	65k, 262k	1	1	1	8bits serial interface+ RGB interface	DIN_SDA, DOUT,DCX	65k, 262k
		IM2	IM1	IM0	Interface Selection	Data Pins	Available Colors																																																	
		0	0	0	80-system, 18-bits interface	D17-0	262k																																																	
		0	0	1	80-system, 9-bits interface	D8-0	262k																																																	
		0	1	0	80-system, 16-bits interface	D15-0	65k, 262k																																																	
		0	1	1	80-system, 8-bits interface	D7-0	65k, 262k																																																	
		1	0	0	MDDI+ 9bits serial interface	HSSI_D0_P/N	65k, 262k																																																	
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1	1	0	MIPI	HSSI_D0_P/N	65k, 262k																																																			
1	1	1	8bits serial interface+ RGB interface	DIN_SDA, DOUT,DCX	65k, 262k																																																			
TE	Digital Output (VDDI -VSS)	-Frame head pulse signal. Utilize this signal when synchronizing RAM data write operations.																																																						
		- VDDI is the Power supply for FTE pin output buffer. please connect VDDI to suitable level. -If not used, please open this pin																																																						
TE1/IDLE_ON	Digital Output (VDDI -VSS)	-TE1 is used for noise sensing of touch panel (Generating a pulse output per scan line from NT35310).																																																						
		- IDLE_ON is used for IDLE mode BL control. -Please used command LPM_HZ &TE1_ON to select the pin function.																																																						
RESX	Digital Input (VDDI)	-This signal will reset the device and must be applied to properly initialize the chip. Signal is active Low. -There is no internal pull high resistor for this pin.																																																						

4.8 Display Driver Analog Outputs

Symbol	Pad Type	Description
VCOM	LCD Output	VCOM output voltage for DC VCOM mode.
AVDD	Power output	Positive Power supply to the source and VCOM drive.
AVEE	Power output	Negative Power supply to the source and VCOM drive.
VGLO	Analog Output	VGLO output from charge pump (please connect to VGL on panel)
S0 to S959	Source Output	Liquid crystal application voltage output lines.
G0 to G479	Gate Output	Gate driver output pins.

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4.9 Power Supply

Symbol	Pad Type	Description
VDD	Power Supply	Power supply to the internal logic regulator circuit. VDD = 1.5V (Typical).
VGH	Charge Pump Output	Output voltage from the step-up circuit, generated from AVDD.
VGL	IC substrate input	Please connect to VGLO pad.
VCL	Charge Pump Output	Output voltage from the step-up circuit, generated from VCI. VCL = - VCI1
C11P/C11M C12P/C12M	Analog Output	Capacitor connection pins for the step-up circuit 1 which generate AVDD and VCL.
C21P/C21M C22P/C22M	Analog Output	Capacitor connection pins for the step-up 5 circuit which generate AVEE.
C13P/C13M	Analog Output	Capacitor connection pins for the step-up 2,3 circuit which generate VGH and VGL.
GVDDP	LDO Output	Positive voltage level generated from AVDD. LDO output for positive gray scale voltage generator.
GVDDN	LDO Output	Negative voltage level generated from AVEE. LDO output for negative gray scale voltage generator.
VREF	LDO Output	Reference voltage output from the internal reference voltage generating circuit.

4.10 Test Pins (Test and Dummy Pins)

Symbol	Pad Type	Description
TESTM	Digital Input	Test pin not accessible to user. Please connect to VSS or let it open.
OSC	Digital Input	Test pin not accessible to user. Please connect to VSS or let it open.
VSS_DUM	-	Please let this pin Hiz or connect to VSS.
Dummy	-	These pins are dummy (possess no function inside) Dummy pin not accessible to user; must be let it open.
FRM	Digital Input (VDDI)	This pin can select the free running mode for burn-in test. The display data alternates between full black and full white independent of input data in free running mode. - FRM = '0', Normal operation mode - FRM = '1', Free running mode If it is not in use, keep it at VSS level.

5. Function Descriptions

5.1 MPU Interface

The NT35310 provides several types of MPU interfaces at high speed. However, if the interface cycle time is faster than the limit, the external MPU needs to have dummy wait(s) to meet the limit of the interface cycle time. User can read / write the registers or RAM via these MPU interfaces. Interface type can be selected by setting the IM2 / IM1 / IM0 pins.

IM2	IM1	IM0	System Interface	Data Pins	Available Colors
0	0	0	80-System 18-bits Interface	D[17 : 0]	262k
0	0	1	80-System 9-bits Interface	D[8 : 0]	262k
0	1	0	80-System 16-bits Interface	D[15 : 0]	65k, 262k
0	1	1	80-System 8-bits Interface	D[7 : 0]	65k, 262k
1	0	0	MDDI+9bits serial interface	HSSI_D0_P/N for MDDI I/F	65k, 262k
1	0	1	9bits serial interface + RGB	DIN_SDA,DOUT	65k, 262k
1	1	0	MIPI Interface	HSSI_D0_P/N	65k, 262k
1	1	1	8bits serial interface	DIN_SDA,DOUT and DCX	65k, 262k

Table 5.1.1 Interfaces of NT35310

5.1.1 General Protocol

For programming of the LCD driver, the general supported protocol is shown in Fig. 5.1.1

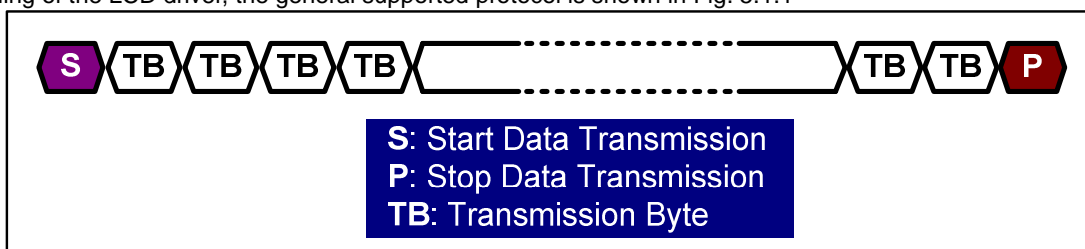


Figure 5.1.1 Programming Protocol

5.1.2 80-System Interface

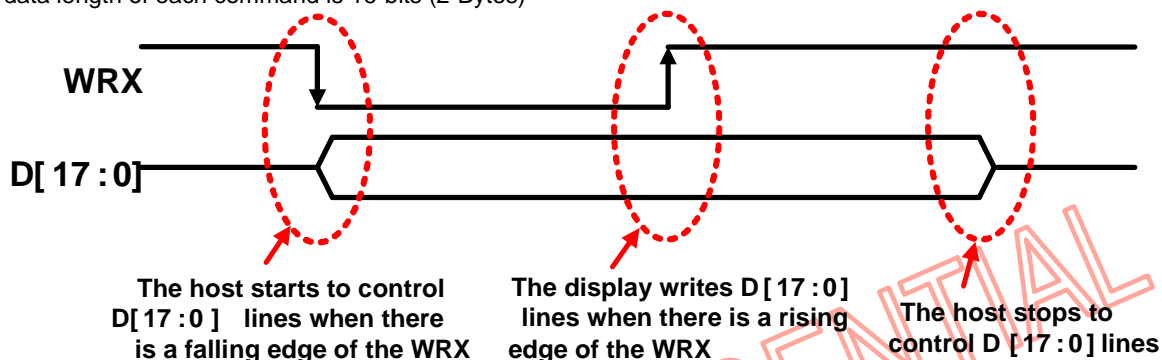
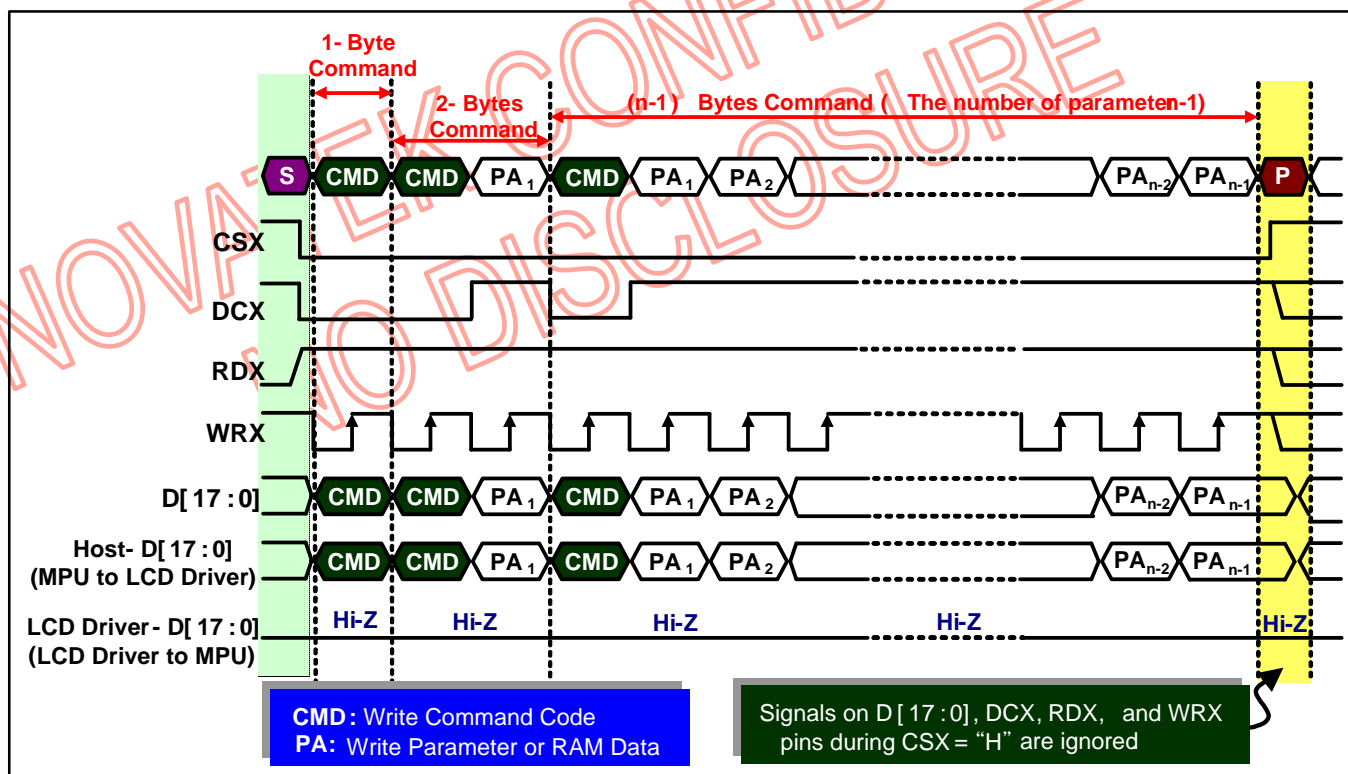
The MCU uses 11-wires 8-bits-data, 12-wires 9-bits-data, 19-wires 16-bits-data and 21-wires 18-bits-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[17 : 0] is parallel data. The Graphics Controller Chip reads the data at the rising edge of WRX signal. The DCX is the data/command flag. When DCX = '1', D[17 : 0] bits are display RAM or command parameters. When DCX = '0', D[17 : 0] bits are commands. The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected by setting IM2, IM1 and IM0 as following table.

IM2	IM1	IM0	Interface	DCX	RDX	WRX	Function Description
0	1	1	8-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
				1	1	↑	Write 16/18-bits display data or 8-bits parameter (D7 to D0)
				1	↑	1	Read 16/18-bits Display data (D7 to D0)
				1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	0	1	9-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
				1	1	↑	Write 18-bits display data (D8 to D0) Write 8-bits parameter (D7 to D0)
				1	↑	1	Read 18-bits Display data (D8 to D0)
				1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	1	0	16-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
				1	1	↑	Write 16/18-bits display data (D15 to D0) Write 8-bits parameter (D7 to D0)
				1	↑	1	Read 16/18-bits Display data (D15 to D0)
				1	↑	1	Read 8-bits parameter or status (D7 to D0)
0	0	0	18-bits Parallel	0	1	↑	Write 8-bits command (D7 to D0)
				1	1	↑	Write 18-bits display data (D17 to D0) Write 8-bits parameter (D7 to D0)
				1	↑	1	Read 18-bits Display data (D17 to D0)
				1	↑	1	Read 8-bits parameter or status (D7 to D0)

Table 5.1.2 The Function of 80-Series System Interface

5.1.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control lines (DCX, RDX, WRX) and data signals (D[17 : 0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (= '0') and vice versa it is data (= '1'). The data length of each command is 16-bits (2-Bytes)


Figure 5.1.2 80-Series WRX Protocol

Figure 5.1.3 80-Series Parallel Bus Protocol for Register or RAM Write

5.1.2.2 Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17 : 0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

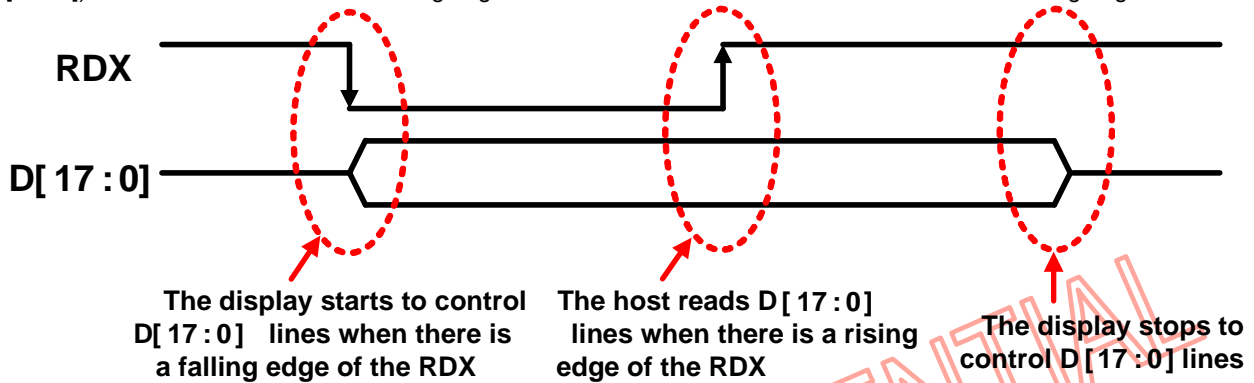


Figure 5.1.6 80-Series RDX Protocol

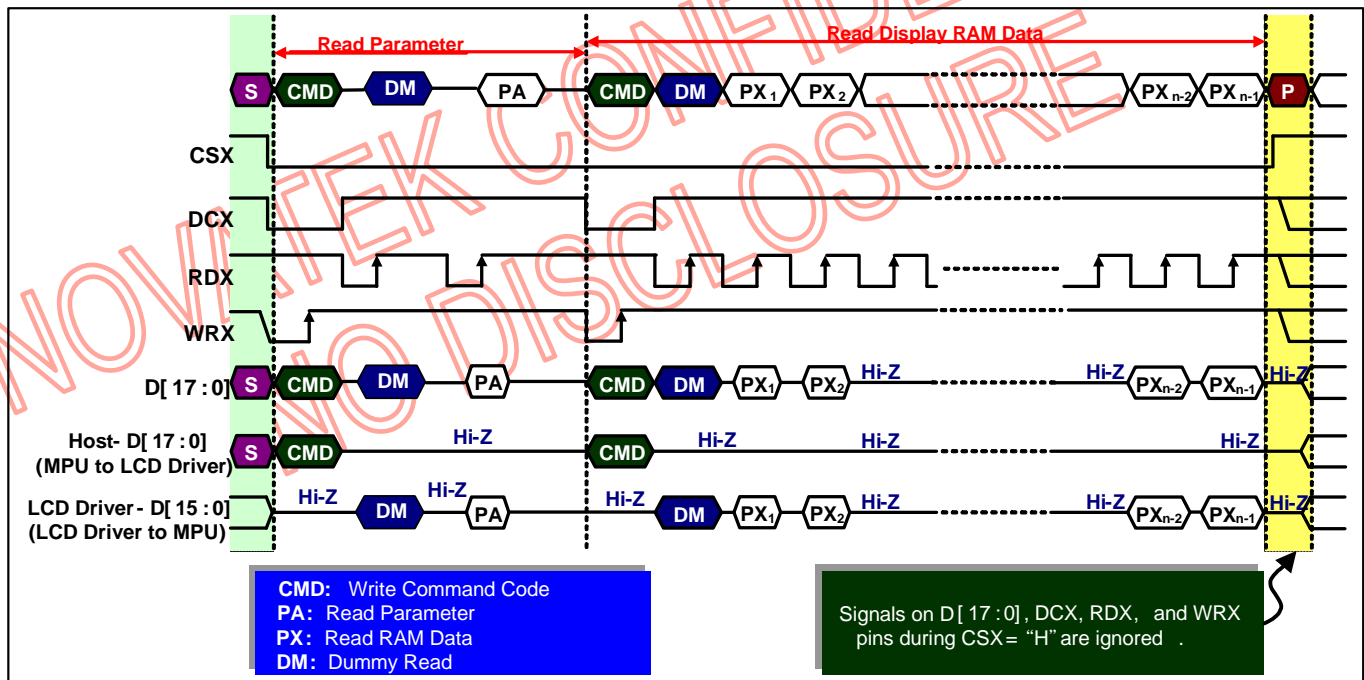


Figure 5.1.7 80-Series Parallel Bus Protocol for Register or RAM Read

Note:
One dummy read is required in read register and display RAM data.

5.2 SPI Interface

5.2.1 General Description for LoSSI

The Module uses a 9-bits serial interface (LoSSI). The chip-select CSX (active low) enables and disables the serial interface. RESX (active low) is an external reset signal. SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D/CX, D7 to D0. The Graphics Controller Chip reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bit are display RAM data or command parameters. When D/CX = "0" D7 to D0 bit are commands.

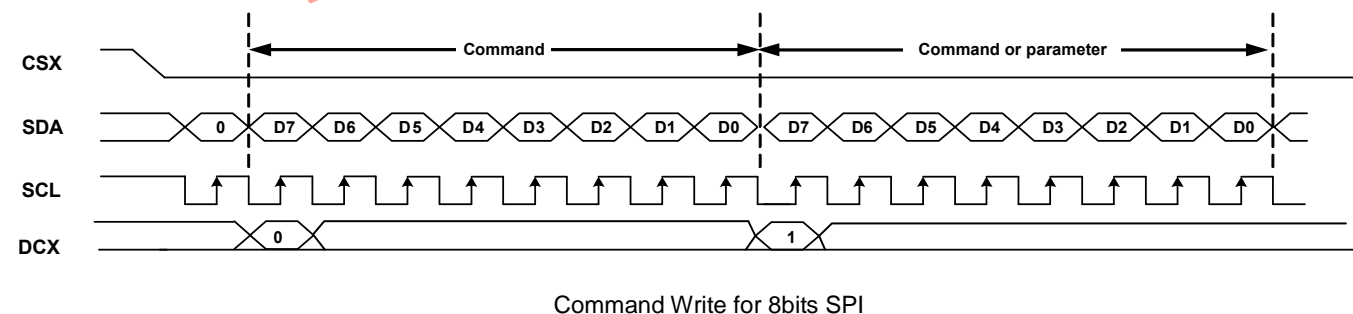
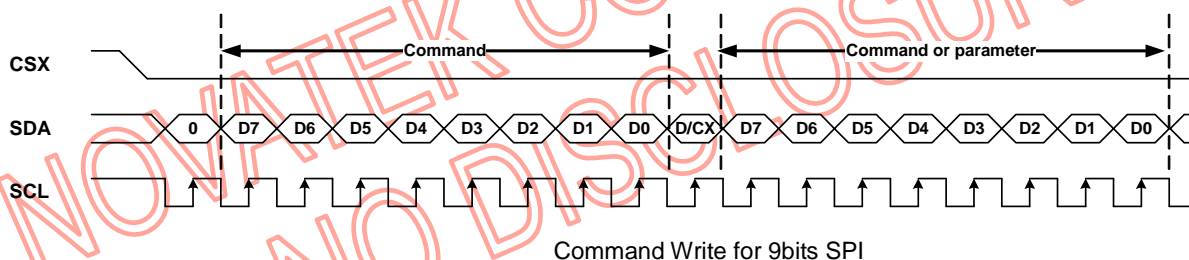
SCL is not a continuous clock and it can be stopped by the host CPU when SCL is low or high after a rising edge of SCL for D0 in the writing mode.

SCL and SDA can be high or low when there is a falling or rising edge of the CSX.

The 8bits serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]) which are not used, must be leave these unused pins to open. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

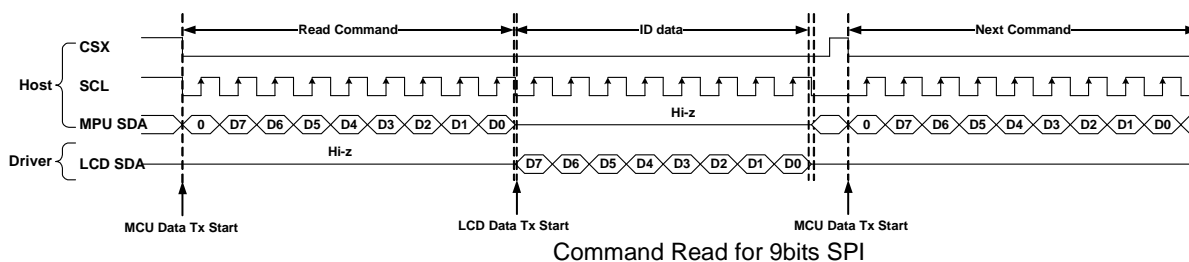
5.2.2 Command Write for LoSSI

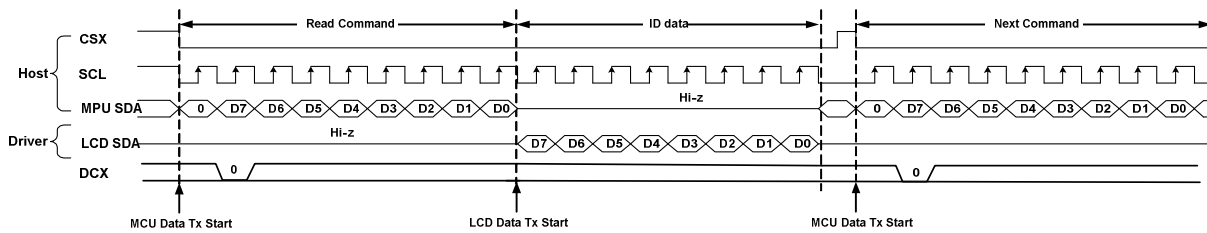
The host CPU drives the CSX pin low and starts by setting the D/CX-bit on SDA. The bit is read by the display on the first rising edge of SCL. On the next falling edge of SCL the MSB data bit (D7) is set on SDA by the CPU. On the next falling edge of SCL the next bit (D6) is set on SDA. This continues until all 8 Data bits have been transmitted as shown in Figure 33: Command Write.



5.2.3 Read Functions for LoSSI

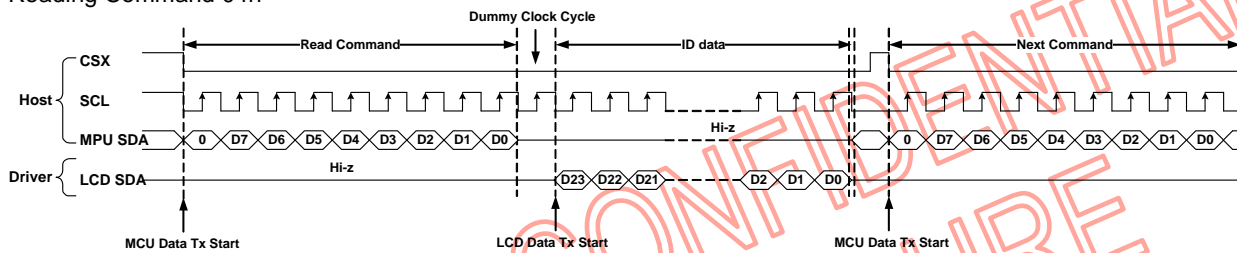
8-bits Reading Function Without Including Dummy Clock Cycle
 Reading Commands 05h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, DAh, DBh, DCh



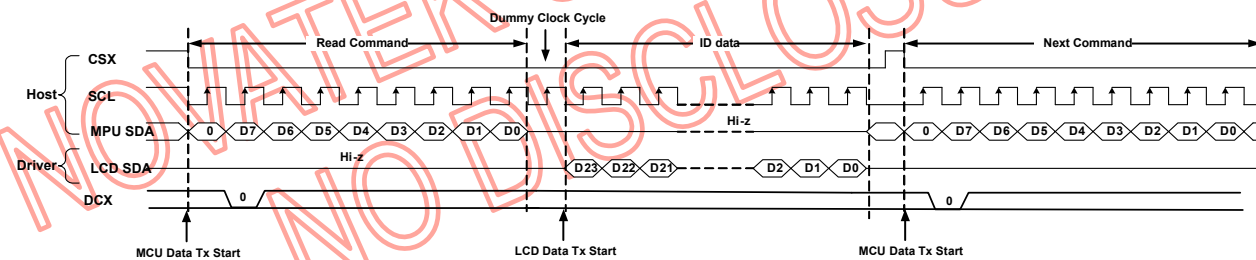


Command Read for 8bits SPI

24-bits Reading Function With Including Dummy Clock Cycle Reading Command 04h



Command Read for 9bits SPI

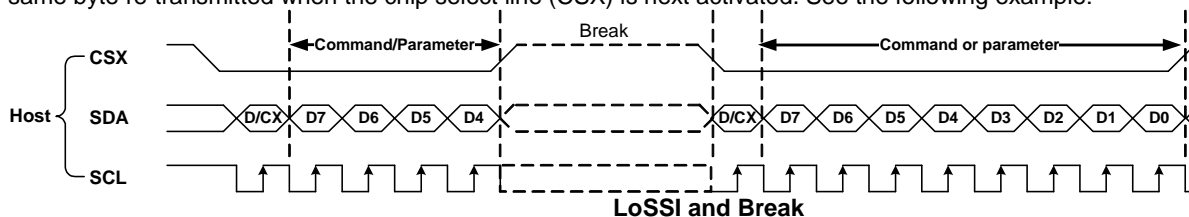


Command Read for 8bits SPI

Note: ID Data length is 24bits.

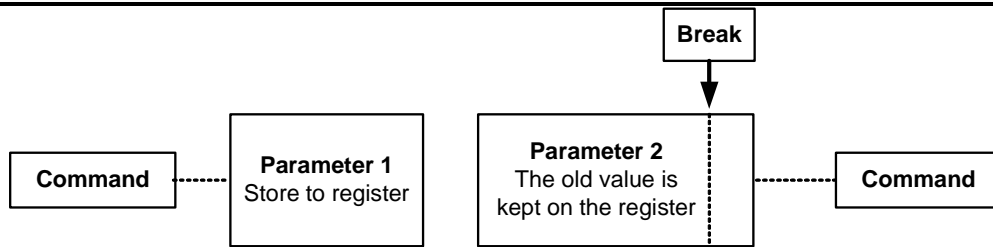
5.2.4 Display Module Data Transfer Recovery for LoSSI

If there is a break in data transmission while transferring command, Frame Memory Data or Multiple Parameter command Data, before a whole byte has been completed, then the Display Module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example:

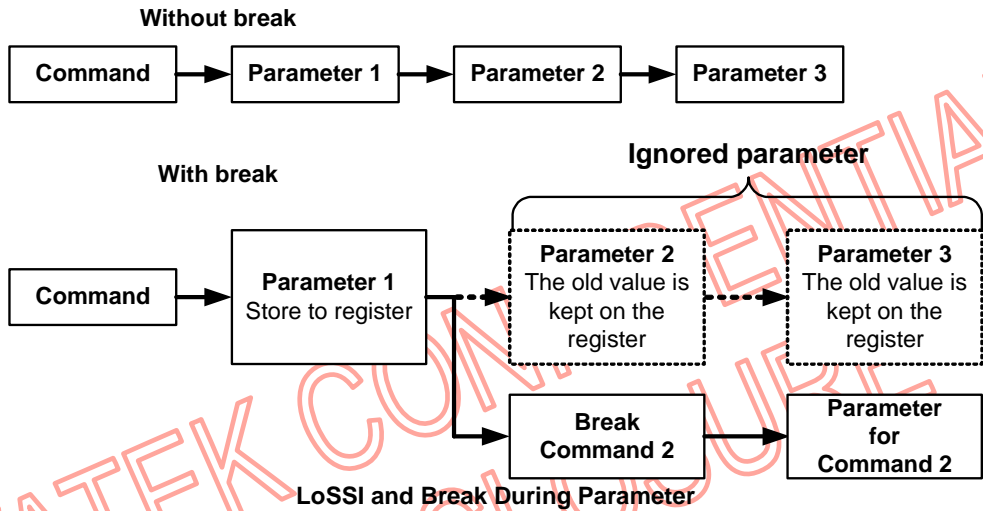


If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

1. Middle of frame



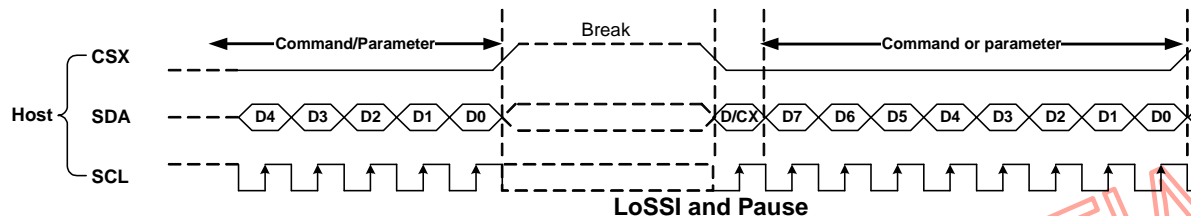
2. Between frames



Note: Break can be e.g. another command or noise pulse.

5.2.5 Display Module Data Transfer Pause for LoSSI

It will be possible when transferring Frame Memory Data, Command or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of Frame Memory Data, Command or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data, Command or Parameter Data Transmission from the point where it was paused as shown below:



There are 4 cases where there is possible to see this kind of pause:

- 1) Command – Pause – Command
- 2) Command – Pause – Parameter
- 3) Parameter – Pause – Command
- 4) Parameter – Pause – Parameter

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5.2.6 Display Module Data Transfer Modes for LoSSI

The Module has 2 kinds of color modes for transferring data to the display RAM. These are 16-bits color per pixel and 18-bits color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

5.2.6.1 Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

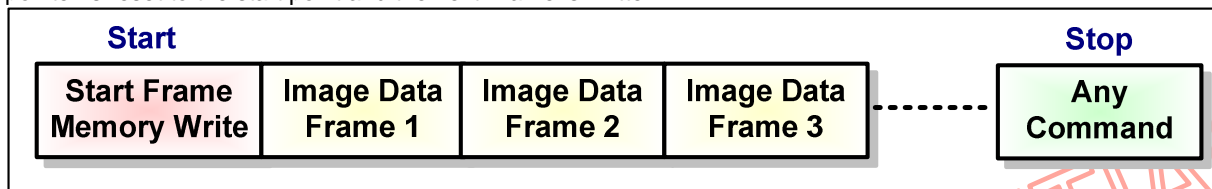


Figure: Data Transfer Method 1

5.2.6.2 Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

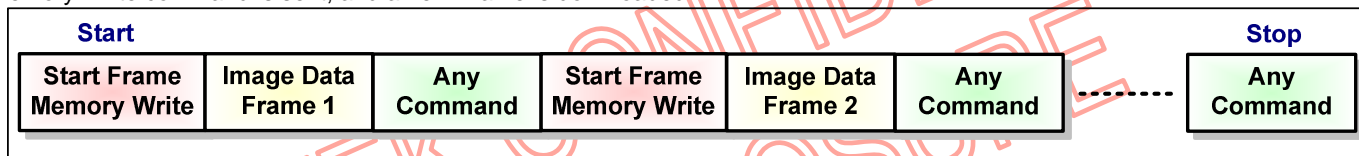


Figure: Data Transfer Method 2 with "Any Command" Break

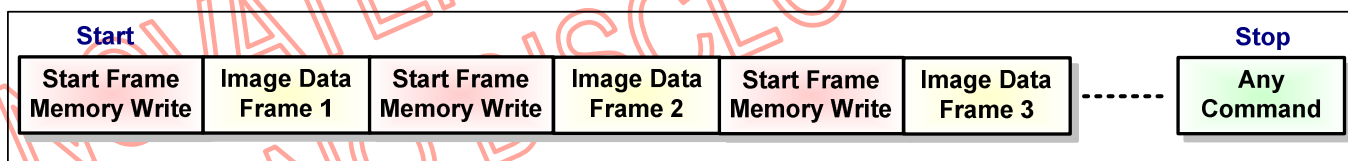


Figure: Data Transfer Method 2 with "Start Frame Memory Write" Break

Note:

- (1) These apply to all Data Transfer Color modes on both Serial and Parallel interfaces.
- (2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.
- (3) "Any Command" can be as same as "Start Frame Memory Write"
- (4) "Memory Write Continuously (3Ch)" or "Memory Read Continuously (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any command" has stopped the memory writing or reading.

5.3 Display Data Ram (DDRAM)

The NT35310 has an integrated 320x480x18-bits graphic type static RAM. This 345600-bytes memory allows to store a 320xRGBx480 image with 18-bits resolution (262K-color) on-chip. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

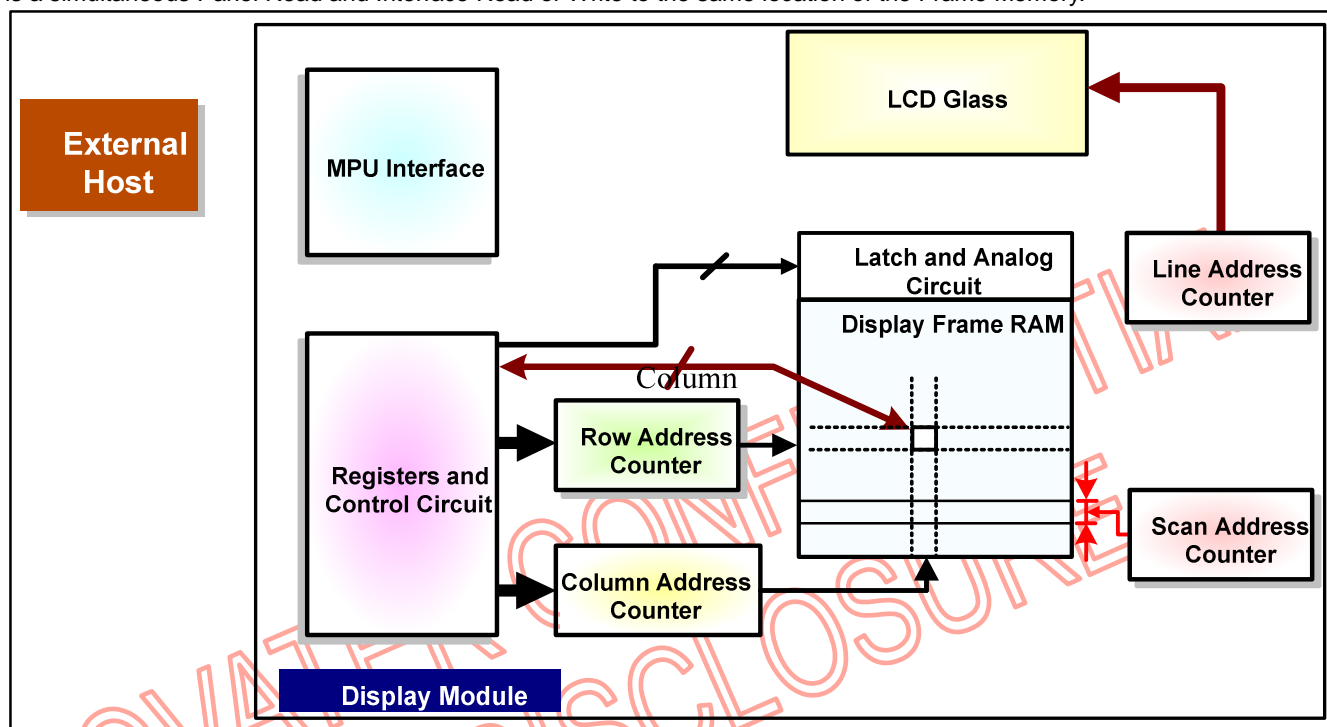


Figure 5.2.1 Display Data RAM

5.3.1 Serial Interface for DATA RAM write

Different display data formats are available for four colors depth supported by the LCM listed below:

- 65k colors, RGB 5, 6, 5-bits pixel data input.
- 262k colors, RGB 6, 6, 6-bits pixel data input.

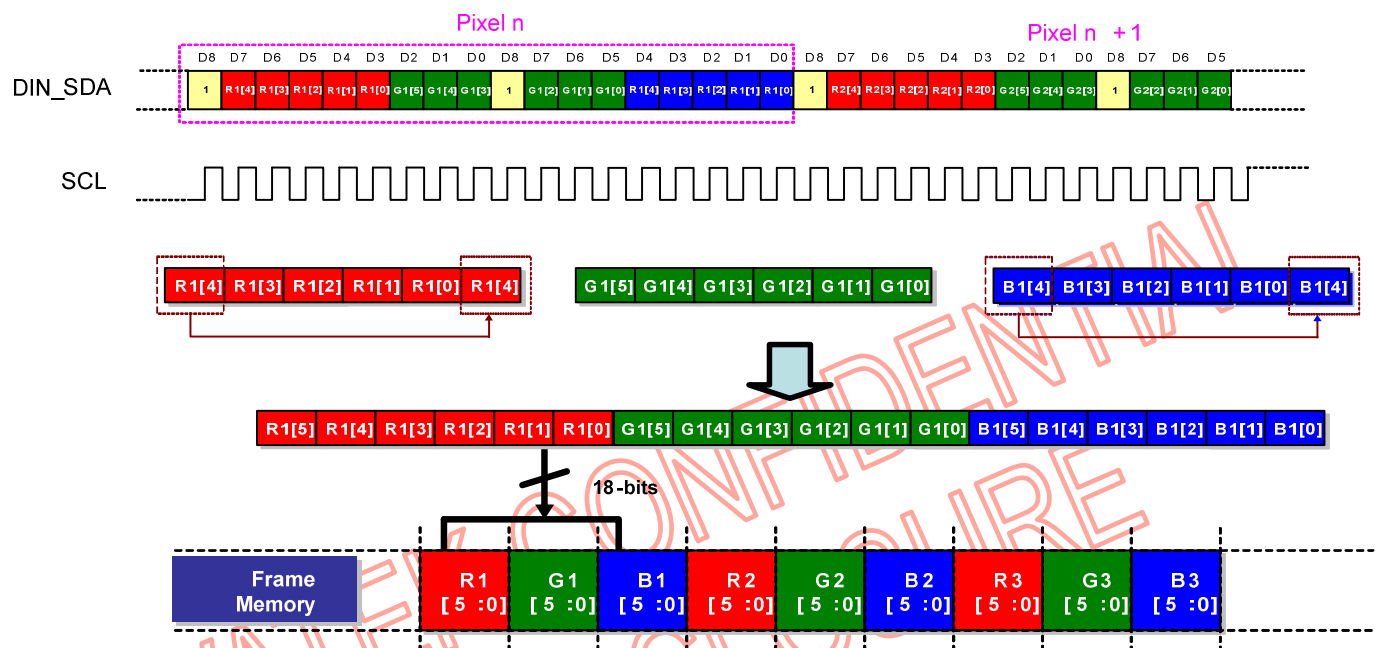


Figure 5.3.1: Write Image Data with RGB 5, 6, 5-bits Pixel Format via SPI

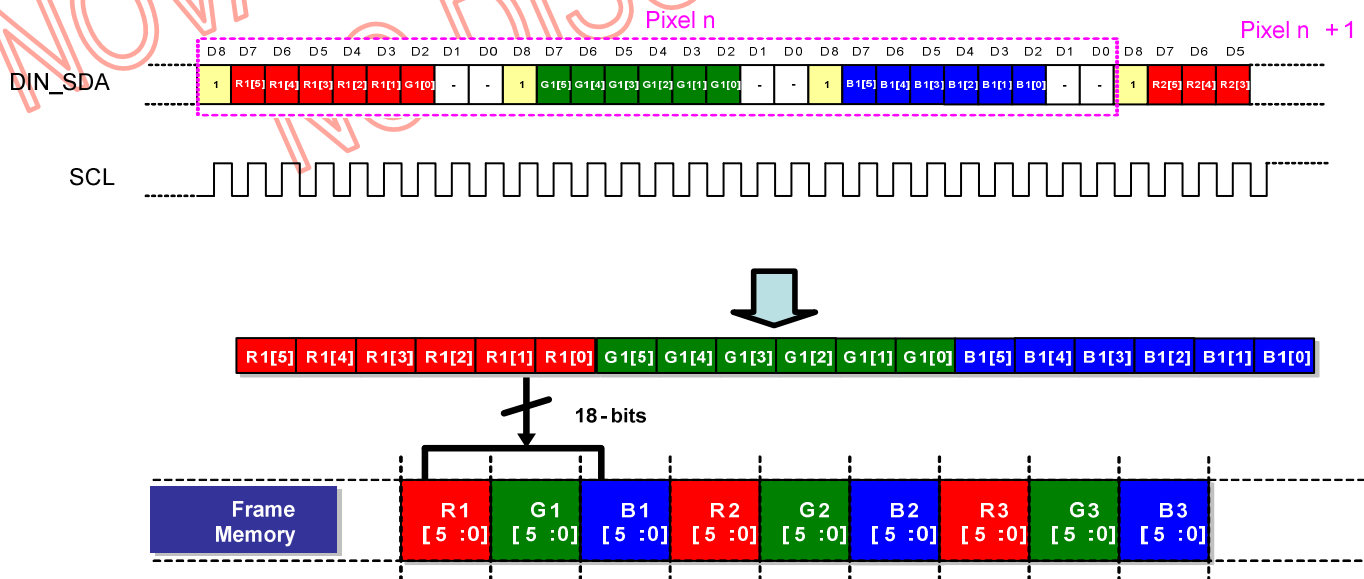


Figure 5.3.2 : Write Image Data with RGB 6, 6, 6-bits Pixel Format via SPI

5.3.2 8-Bits Parallel Interface for RAM Data Write

Different display data formats are available for three colors depth supported by the NT35310 listed below.

- 65k colors, RGB 5, 6, 5-bits pixel data input.
- 262k colors, RGB 6, 6, 6-bits pixel data input.

Register Command	D[17 : 8]	D7	D6	D5	D4	D3	D2	D1	D0	Register
	X	0	0	1	0	1	1	0	0	2Ch
3Ah	D[17 : 8]	D7	D6	D5	D4	D3	D2	D1	D0	Color Depth
05h	x	R4	R3	R2	R1	R0	G5	G4	G3	65k - Colors (1-pixels / 2-transfer)
	x	G2	G1	G0	B4	B3	B2	B1	B0	
06h	x	R5	R4	R3	R2	R1	R0	x	x	262k - Colors (1-pixels / 3-transfer)
	x	G5	G4	G3	G2	G1	G0	x	x	
	x	B5	B4	B3	B2	B1	B0	x	x	

Note. 'x' = Don't care - Can be set to '0' or '1'

Table 5.3.1 The Pixel Data Format via 80-Series 8-bits Parallel Interface

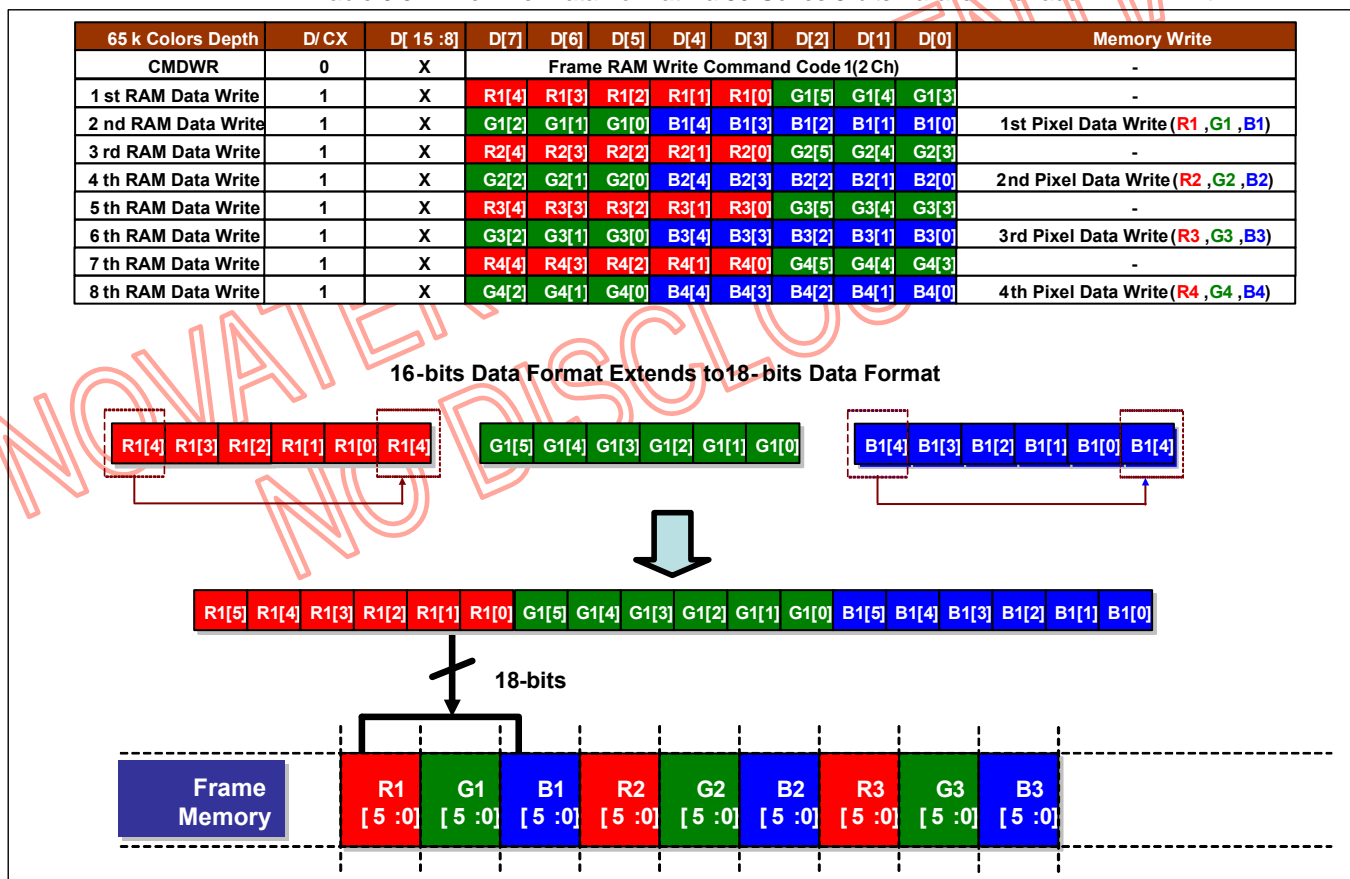


Figure 5.3.3 Write RGB 5-6-5-bits Pixel Data via 8-bits Parallel Interface (3Ah = "05h")

Note :

- (1) 2 times transfer is used to transmit 1 pixel data with the 16-bits color depth information.
- (2) The most significant bits are : Rx4, Gx5 and Bx4.
- (3) The least significant bits are : Rx0, Gx0 and Bx0.

262 k Colors Depth	D/CX	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Memory Write
CMDWR 1	0	X	Frame RAM Write Command Code 1 (2Ch)								-
1st RAM Data Write	1	X	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X	-
2nd RAM Data Write	1	X	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X	-
3rd RAM Data Write	1	X	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X	1st Pixel Data Write(R1, G1, B1)
4th RAM Data Write	1	X	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	X	X	-
5th RAM Data Write	1	X	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	X	X	-
6th RAM Data Write	1	X	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	X	X	2nd Pixel Data Write(R2, G2, B2)
7th RAM Data Write	1	X	R3[5]	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	X	X	-
8th RAM Data Write	1	X	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]	X	X	-

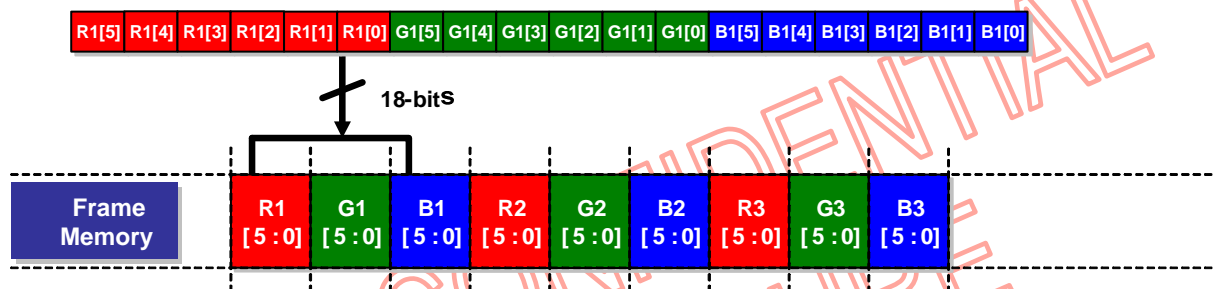


Figure 5.3.4 Write RGB 6-6-6-bits Pixel Data via 8-bits Parallel Interface (3Ah = "06h")

Note :

- (1) 3 times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
- (2) The most significant bits are : Rx5, Gx5 and Bx5.
- (3) The least significant bits are : Rx0, Gx0 and Bx0.

5.3.3 9-Bits Parallel Interface (80-system) for RAM Data Write

9-bits parallel interface only support 262k color.
 - 262k colors, RGB 6, 6, 6-bits pixel data input.

Register Command	D[17 : 9]	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	X	0	0	1	0	1	1	0	0	2Ch
3Ah	D[17 : 9]	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color Depth
06h	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262k - Colors (1-pixels / 2-transfer)
	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Note. 'x' = Don't care - Can be set to '0' or '1'

Table 5.3.3 The Pixel Data Format via 80-Series/68-Series 9-bits Parallel Interface

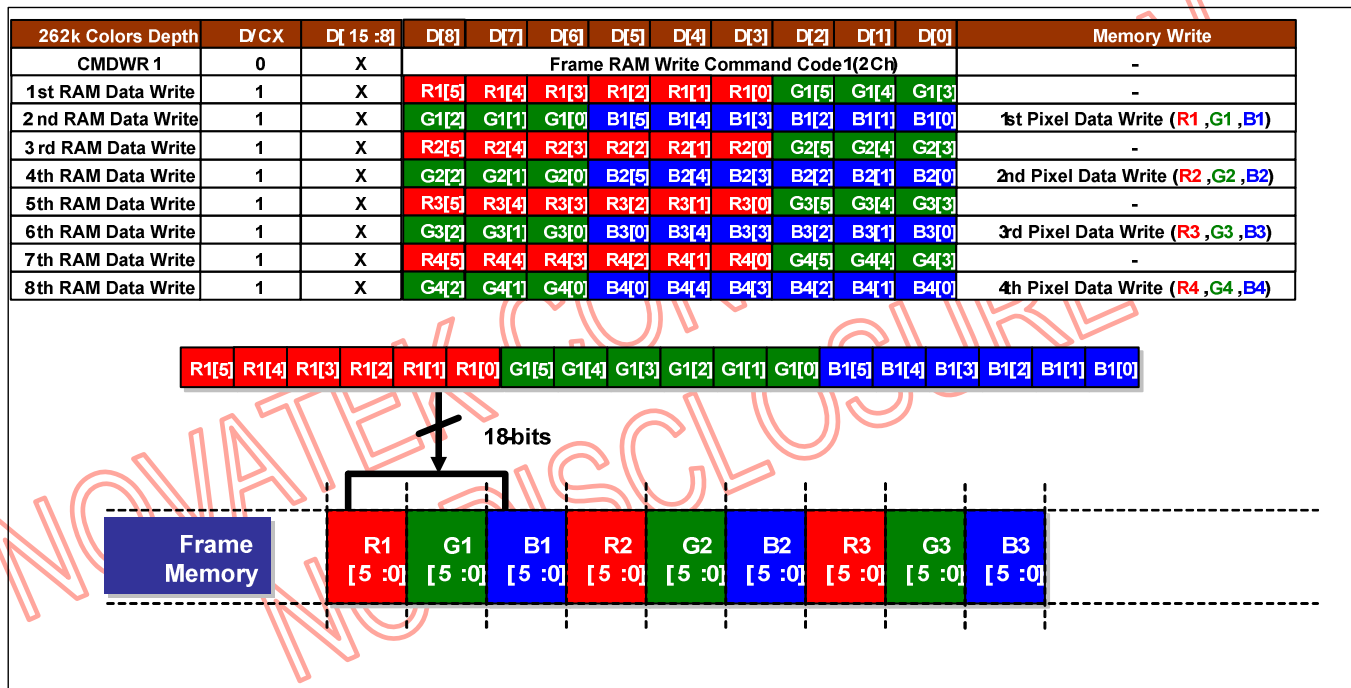


Figure 5.3.5 Write RGB 6-6-6-bits Pixel Data via 9-bits Parallel Interface (3Ah = "06h")

Note :

- (1) 2 times transfer is used to transmit 1 pixel data with the 18-bits color depth information.
- (2) The most significant bits are : Rx5, Gx5 and Bx5.
- (3) The least significant bits are : Rx0, Gx0 and Bx0.

5.3.4 16-Bits Parallel Interface for RAM Data Write

Different display data formats are available for four colors depth supported by listed below.

- 65k colors, RGB 5, 6, 5-bits pixel data input.
- 262k colors, RGB 6, 6, 6-bits pixel data input.

Register Command	D[17 : 16]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	2Ch
3Ah	D[17 : 16]	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color Depth
05h	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65k - Colors
06h	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262k - Colors (2-pixels/ 3-transfer)
	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Note: 'x' = Don't care - Can be set to '0' or '1'

Table 5.3.4 The Pixel Data Format via 80-Series/68-Series 16-bits Parallel Interface

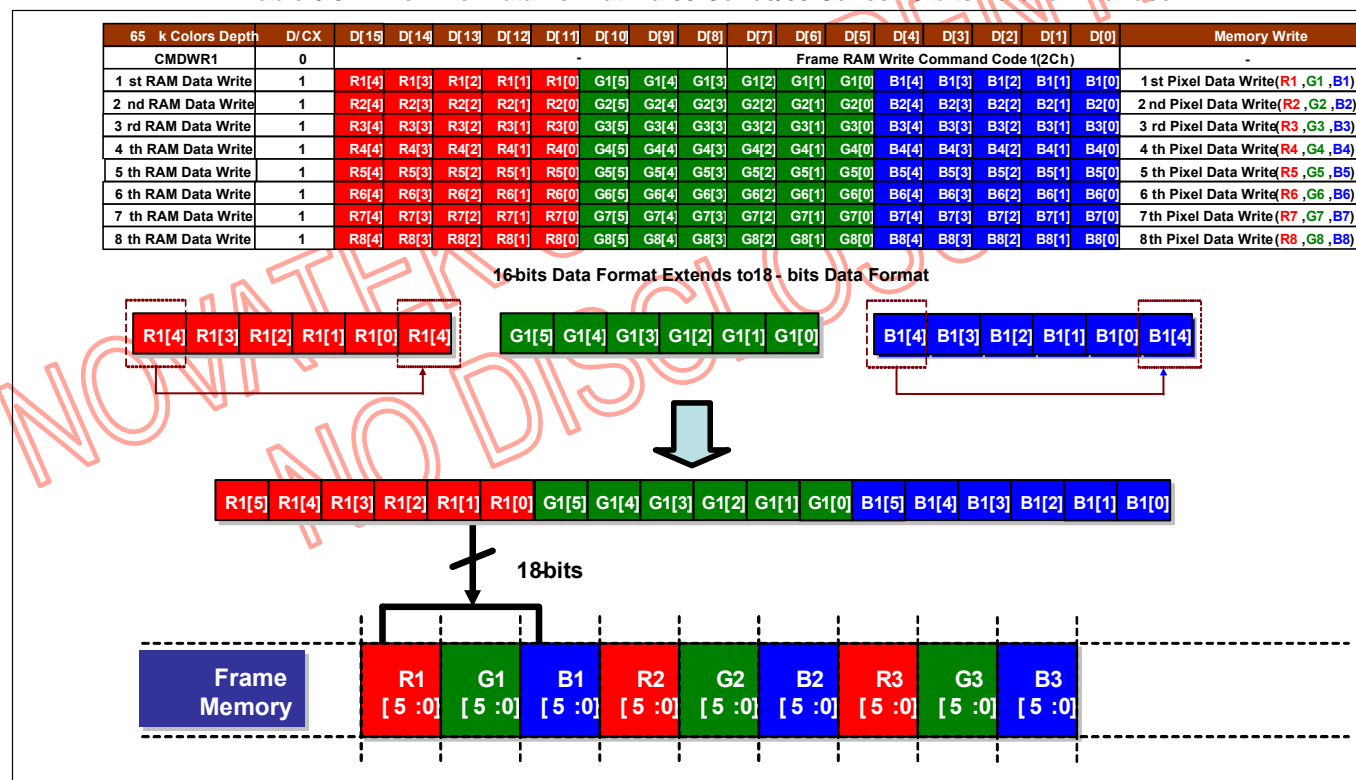


Figure 5.3.6 Write RGB 5-6-5-bits Pixel Data via 16-bits Parallel Interface (3Ah = "05h")

Note :

- (1) In one transfer (D15 to D0), 1 pixel data is transmitted with the 16-bits color depth information.
- (2) The most significant bits are : Rx4, Gx5 and Bx4.
- (3) The least significant bits are : Rx0, Gx0 and Bx0.

262 Colors Depth	D/CX	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Memory Write	
CMDWR1	0	-																Frame RAM Write Command Code 1(2Ch)	-
1 st RAM Data Write	1	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	x	x	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	x	x	-	
2 nd RAM Data Write	1	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	x	x	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	x	x	1 st Pixel Data Write (R1 ,G1 ,B1)	
3 rd RAM Data Write	1	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	x	x	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	x	x	2nd Pixel Data Write (R2 ,G2 ,B2)	
4 th RAM Data Write	1	R3[5]	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	x	x	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]	x	x	-	
5 th RAM Data Write	1	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	x	x	R4[5]	R4[4]	R4[3]	R4[2]	R4[1]	R4[0]	x	x	3rd Pixel Data Write (R3 ,G3 ,B3)	
6 th RAM Data Write	1	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]	x	x	B4[5]	B4[4]	B4[3]	B4[2]	B4[1]	B4[0]	x	x	4 th Pixel Data Write (R4 ,G4 ,B4)	
7 th RAM Data Write	1	R5[5]	R5[4]	R5[3]	R5[2]	R5[1]	R5[0]	x	x	G5[5]	G5[4]	G5[3]	G5[2]	G5[1]	G5[0]	x	x	-	
8 th RAM Data Write	1	B5[5]	B5[4]	B5[3]	B5[2]	B5[1]	B5[0]	x	x	R6[5]	R6[4]	R6[3]	R6[2]	R6[1]	R6[0]	x	x	5 th Pixel Data Write (R5 ,G5 ,B5)	

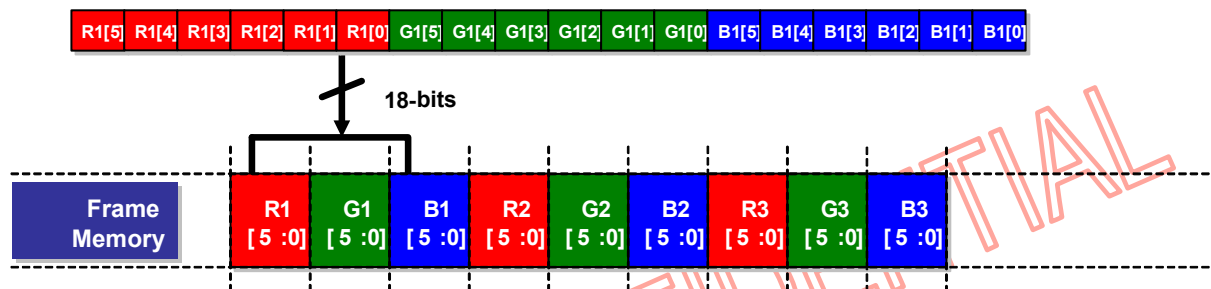


Figure 5.3.7 Write RGB 6-6-6-bits Pixel Data via 16-bits Parallel Interface (3Ah = "06h")

- Note :
- (1) 3 times transfer is used to transmit 2 pixels data or 2 times transfer are used to transmit 1 pixel data with the 18-bits color depth information..
 - (2) The most significant bits are : Rx5, Gx5 and Bx5.
 - (3) The least significant bits are : Rx0, Gx0 and Bx0.

5.3.5 18-Bits Parallel Interface for RAM Data Write

Different display data formats are available for four colors depth supported by listed below.
 - 262k colors, RGB 6, 6, 6-bits pixel data input.

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	2Ch
3Ah	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color Depth
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262k - Colors

Note: 'x' = Don't care - Can be set to '0' or '1'

Table 5.3.5 The Pixel Data Format via 80-Series/68-Series 18-bits Parallel Interface

262 k Colors Depth	D/CX	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Memory Write	
CMDWR1	0	-																		Frame RAM Write Command Code 1(2Ch)	-
1 st RAM Data Write	1	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	1 st Pixel Data Write (R1 ,G1 ,B1)	
2 nd RAM Data Write	1	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	2 nd Pixel Data Write (R2 ,G2 ,B2)	
3 rd RAM Data Write	1	R3[5]	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]	B3[5]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	3 rd Pixel Data Write (R3 ,G3 ,B3)	
4 th RAM Data Write	1	R4[5]	R4[4]	R4[3]	R4[2]	R4[1]	R4[0]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]	B4[5]	B4[4]	B4[3]	B4[2]	B4[1]	B4[0]	4 th Pixel Data Write (R4 ,G4 ,B4)	
5 th RAM Data Write	1	R5[5]	R5[4]	R5[3]	R5[2]	R5[1]	R5[0]	G5[5]	G5[4]	G5[3]	G5[2]	G5[1]	G5[0]	B5[5]	B5[4]	B5[3]	B5[2]	B5[1]	B5[0]	5 th Pixel Data Write (R5 ,G5 ,B5)	
6 th RAM Data Write	1	R6[5]	R6[4]	R6[3]	R6[2]	R6[1]	R6[0]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]	B6[5]	B6[4]	B6[3]	B6[2]	B6[1]	B6[0]	6 th Pixel Data Write (R6 ,G6 ,B6)	
7 th RAM Data Write	1	R7[5]	R7[4]	R7[3]	R7[2]	R7[1]	R7[0]	G7[5]	G7[4]	G7[3]	G7[2]	G7[1]	G7[0]	B7[5]	B7[4]	B7[3]	B7[2]	B7[1]	B7[0]	7 th Pixel Data Write (R7 ,G7 ,B7)	
8 th RAM Data Write	1	R8[5]	R8[4]	R8[3]	R8[2]	R8[1]	R8[0]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]	B8[5]	B8[4]	B8[3]	B8[2]	B8[1]	B8[0]	8 th Pixel Data Write (R8 ,G8 ,B8)	

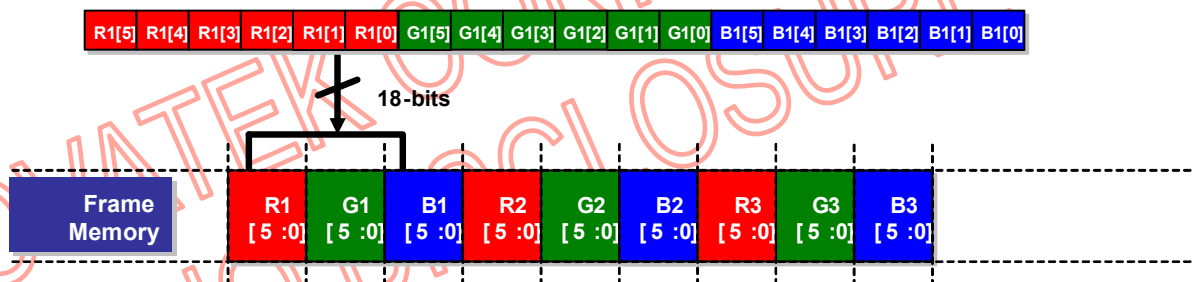
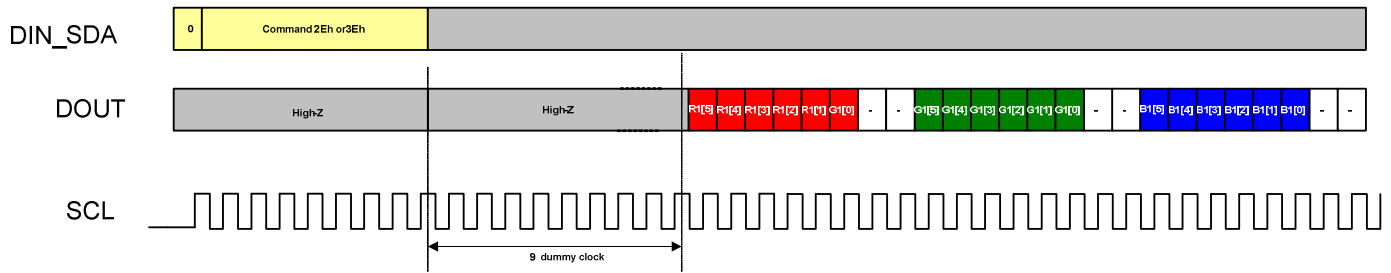


Figure 5.3.8 Write RGB 6-6-6-bits Pixel Data via 18-bits Parallel Interface (3Ah = "06h")

Note :

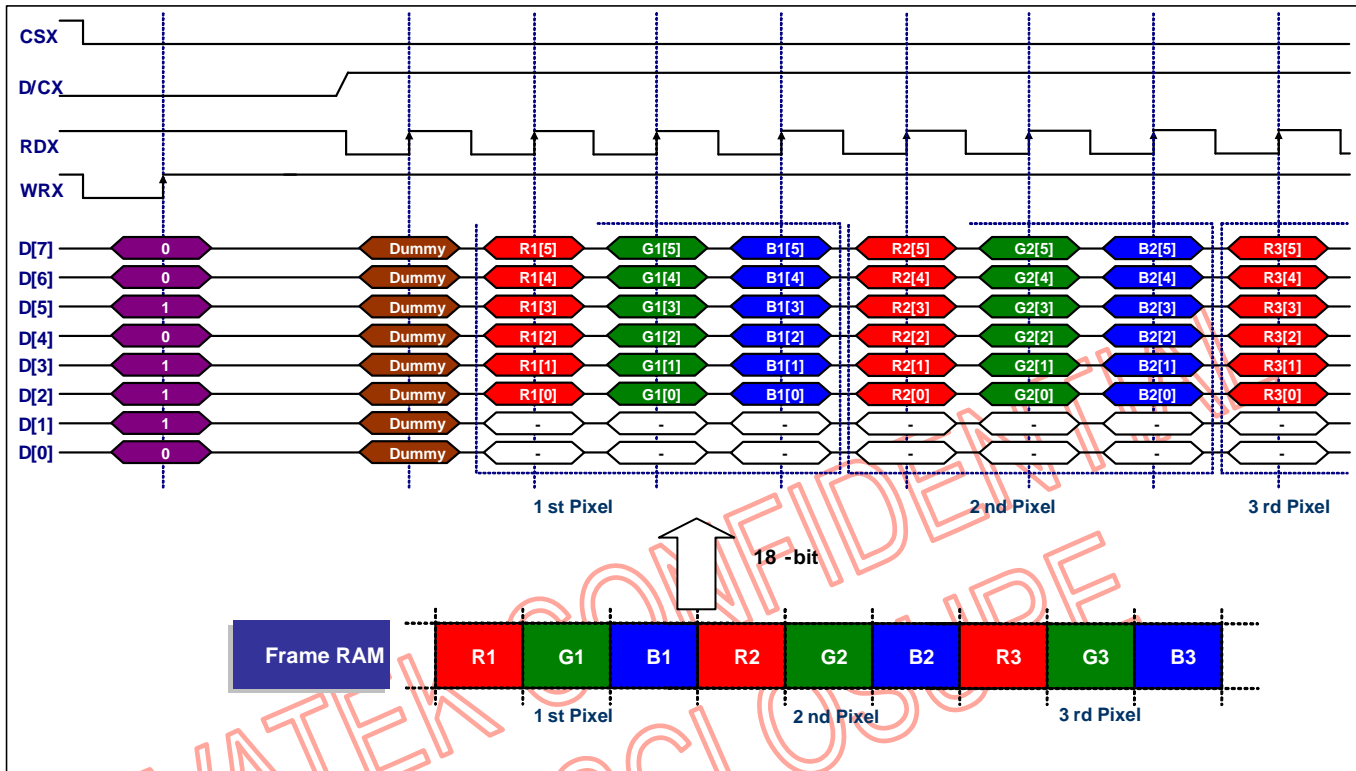
- (1) The most significant bits are : Rx5, Gx5 and Bx5.
- (2) The least significant bits are : Rx0, Gx0 and Bx0.

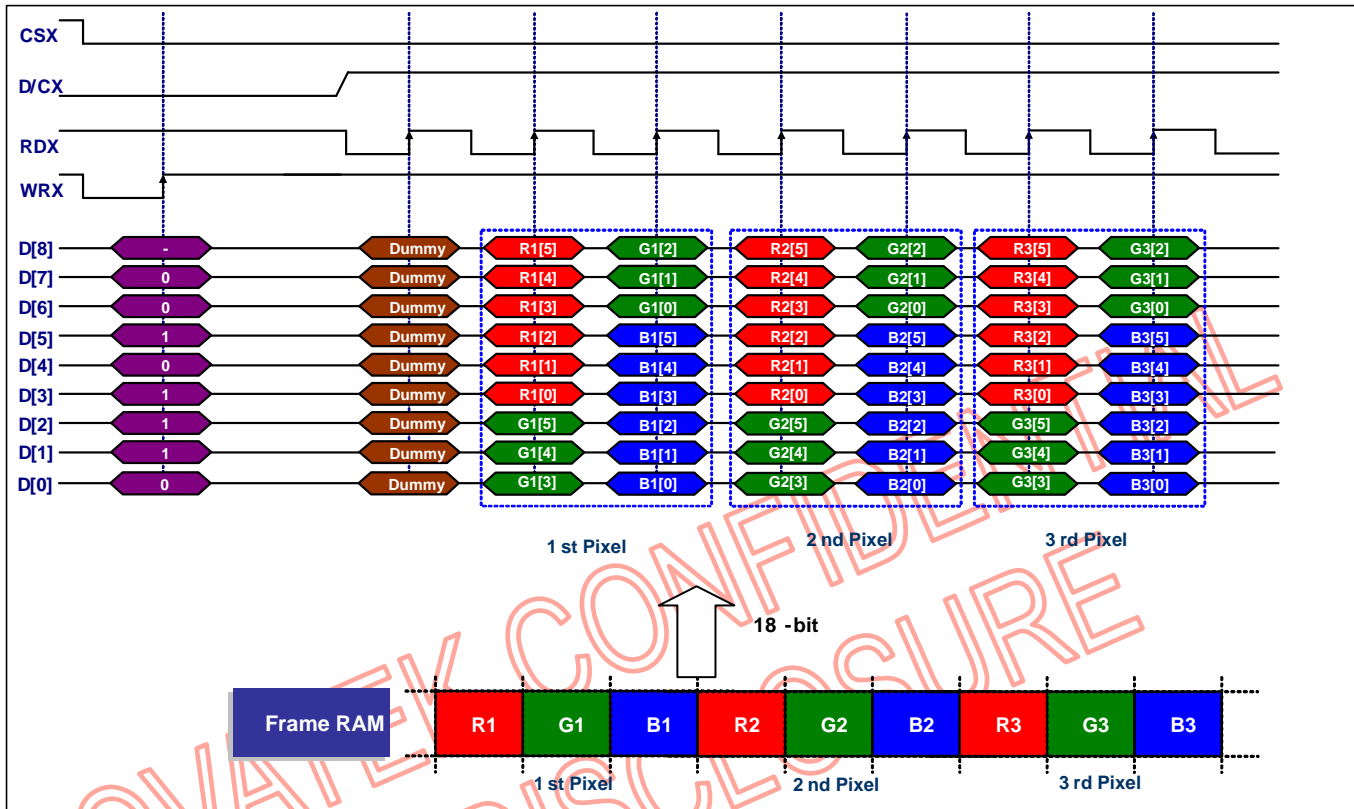
5.3.6 Serial Interface Signals for RAM Data Read


Note: when SDA_EN=0, data output in DOUT.

Figure 5.3.9 Read RAM Data via SPI

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5.3.7 80-8-bits Parallel Interface Signals for RAM Data Read

Figure 5.3.10 Read RAM Data via 80-8 bits Parallel Interface

5.3.8 80-9-bits Parallel Interface Signals for RAM Data Read

Figure 5.3.11 Read RAM Data via 80-9 bits Parallel Interface

5.3.9 80-16-bits Parallel Interface Signals for RAM Data Read

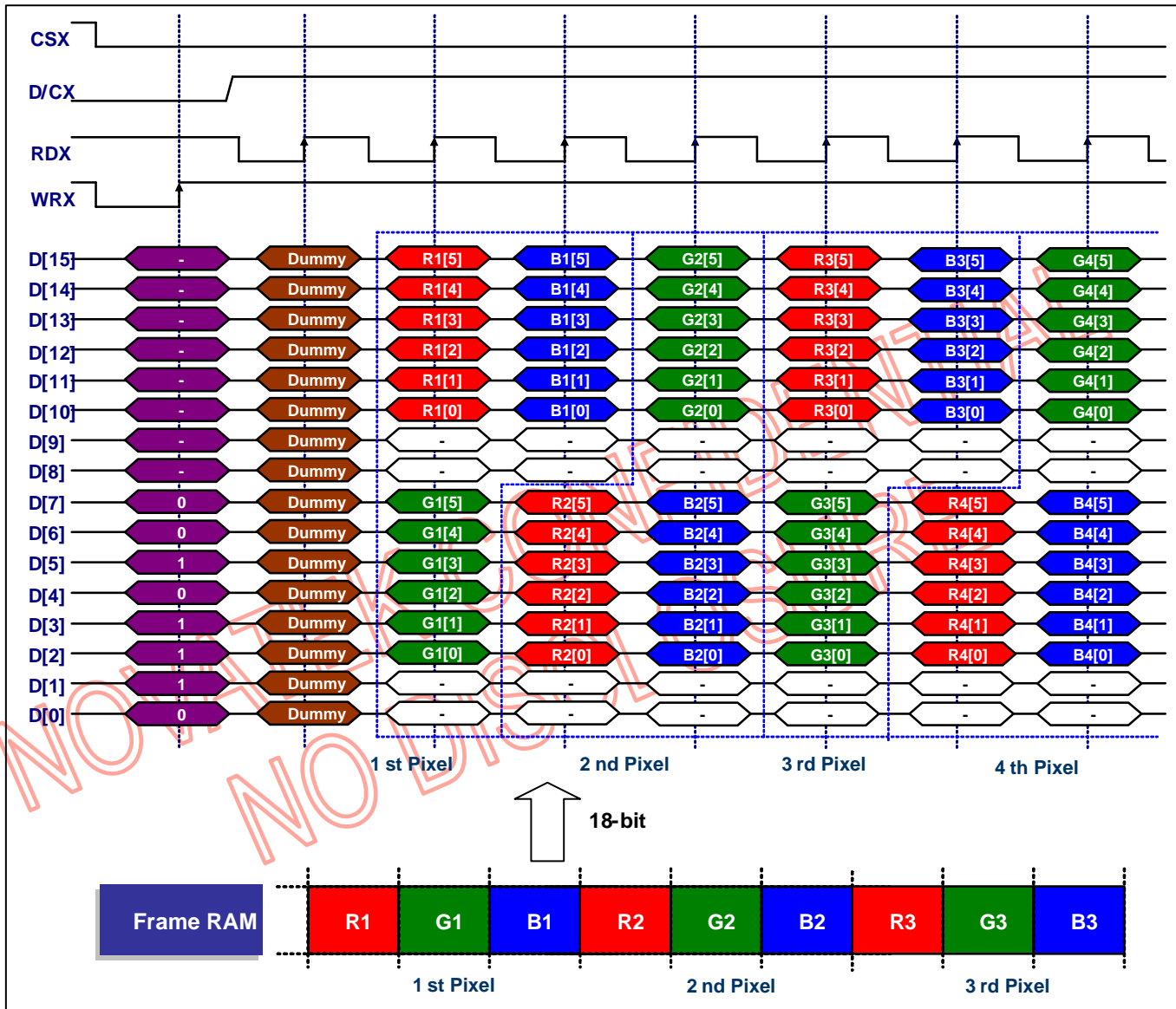


Figure 5.3.12 Read RAM Data with 6-6-6-bits Pixel Format via 80-16 bits Parallel Interface

5.3.10 80-18-bits Parallel Interface Signals for RAM Data Read

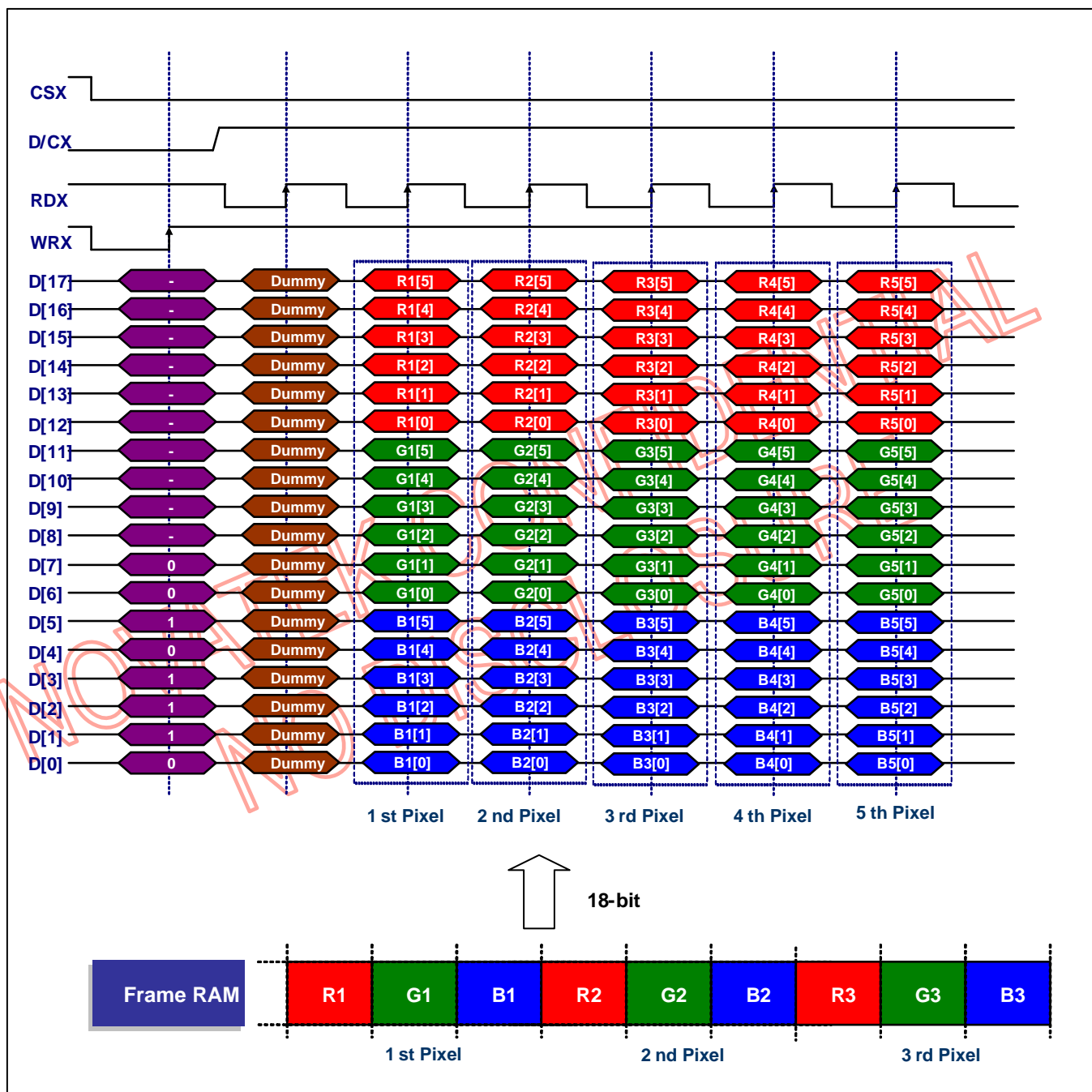


Figure 5.3.13 Read RAM Data with 6-6-6-bits Pixel Format via 80-18 bits Parallel Interface

5.4 RGB Interface

5.4.1 General Description

The module uses 16- and 18- bits parallel RGB interface which includes: VS, HS, DE, PCLK, D[17:0]. 16-bits parallel RGB interface only support 65k color depth (R3A00h = 0050h), 18-bits parallel RGB interface only support 262k color depth (R3Ah = 60h). Beside these setting, other mode is setting inhibits. Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[17:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. sleep in mode etc. Vertical synchronization (VS) is used to show when there is received a new frame of the display. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal. Horizontal synchronization (HS) is used to show when there is received a new line of the frame. This is negative ('0', low) active and its state is read to the display module by a rising edge of the PCLK signal. Data Enable (DE) is used to show when there is received RGB information that should be transferred on the display. This is a positive ('1', high) active and its state is read to the display module by a rising edge of the PCLK signal. D[17:0] are used to show what is the information of the image that is transferred on the display (When DE= '1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal. The PCLK cycle is described in the following figure.

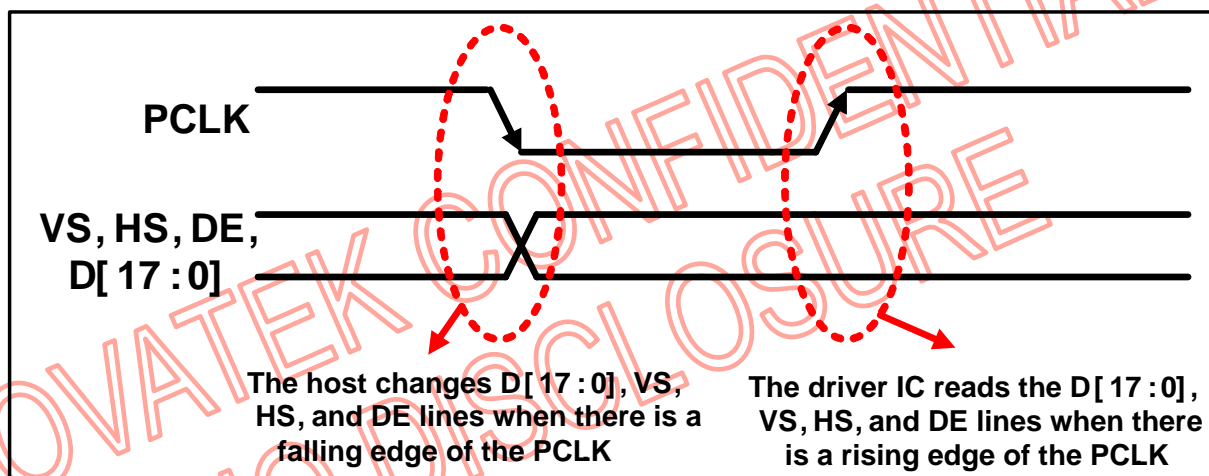


Figure 5.4.1 PCLK cycle

Note: PCLK is an unsynchronized signal (It can be stopped).

5.4.2 General Timing Diagram

In normal operation, host processor should continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts.

The display image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels. With each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicated the beginning of each frame of the displayed image.

Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16- or 18-bits data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

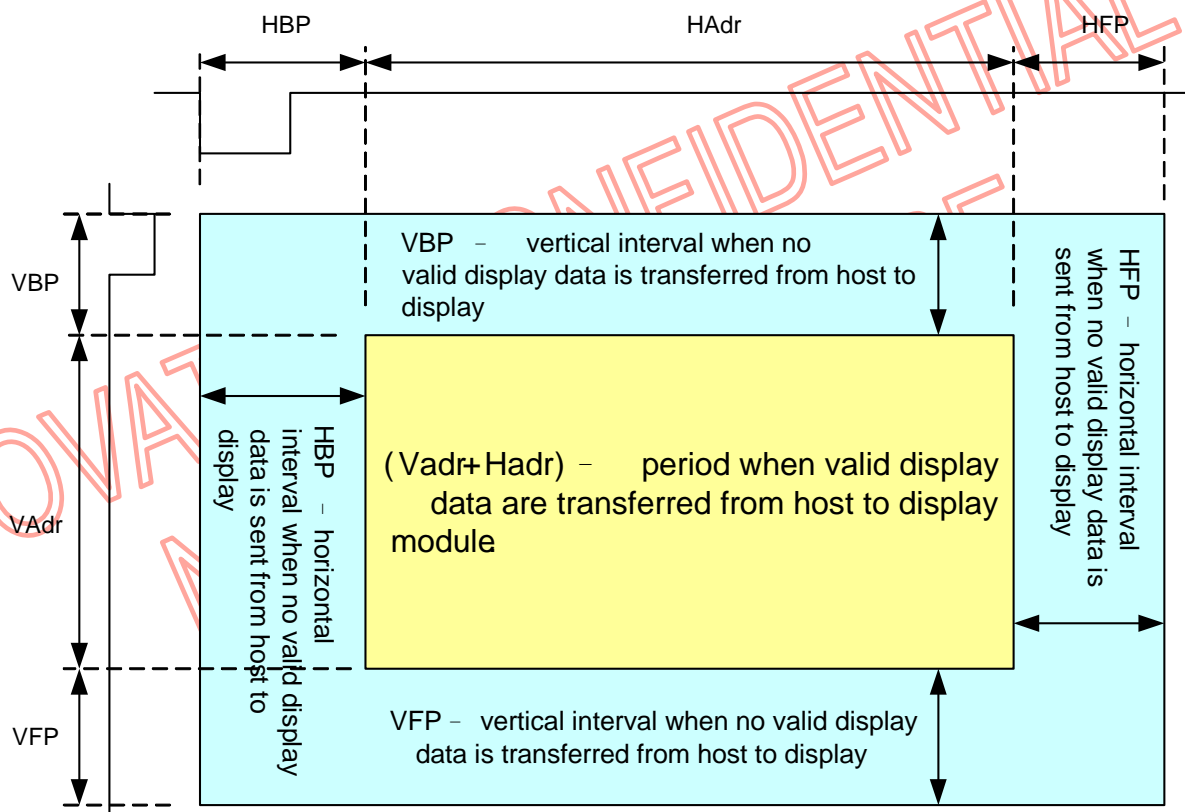


Figure 5.4.2 RGB General Timing Diagram.

5.4.3 RGB Interface Bus Width Set

Table specifies the mapping of data bit, as components of primary pixel color value R, G, and B, to signal lines at the interface.

Table 5.3.1 RGB Interface Bus Width for 16-bits Interface

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	3Ah
x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	50h (16-bits data)

Table 5.3.2 RGB Interface Bus Width for 18-bits Interface

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	3Ah	
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	60h (18-bits data)

Note 1: R0 is the LSB for the red component; G0 is the LSB for the green component, etc.

Note 2: For 16-bits pixels, R primary color MSB is R4, G primary color MSB is G5 and B primary color MSB is B4.

Note 3: For 18-bits pixels, R primary color MSB is R5, G primary color MSB is G5 and B primary color MSB is B5.

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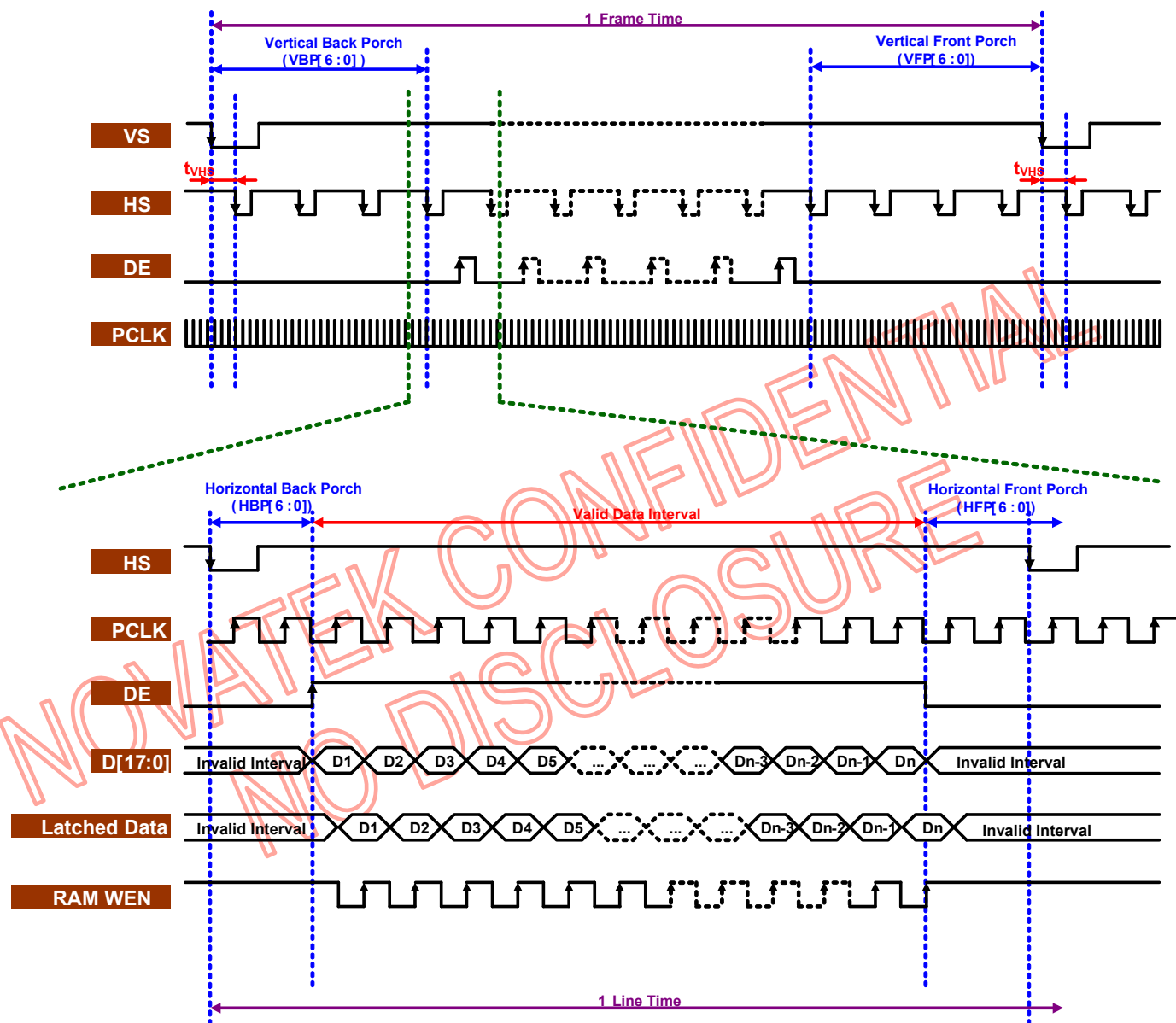
5.4.4 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D17-D0	VS	HS	Register VBP[6:0], HBP[6:0], VFP[6:0], HFP[6:0]
RGB Mode 1	Used	Used	Used	Used	Used	Not used
RGB Mode 2	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D17 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35310.

In RGB Mode 2, back porch of Vsync is defined by VBP[6:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[6:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[6:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[6:0] of RGBPRCTR command.

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5.4.5 RGB Interface Mode 1 & Mode 2 Timing Chart

Fig. 5.4.5.1 Video Signal Data Writing Method in RGB Mode 1 Interface

Constraint : V-Porch (VBP \geq TBD , VFP \geq TBD , VBP > BP)

Note: tVHS \geq TBD

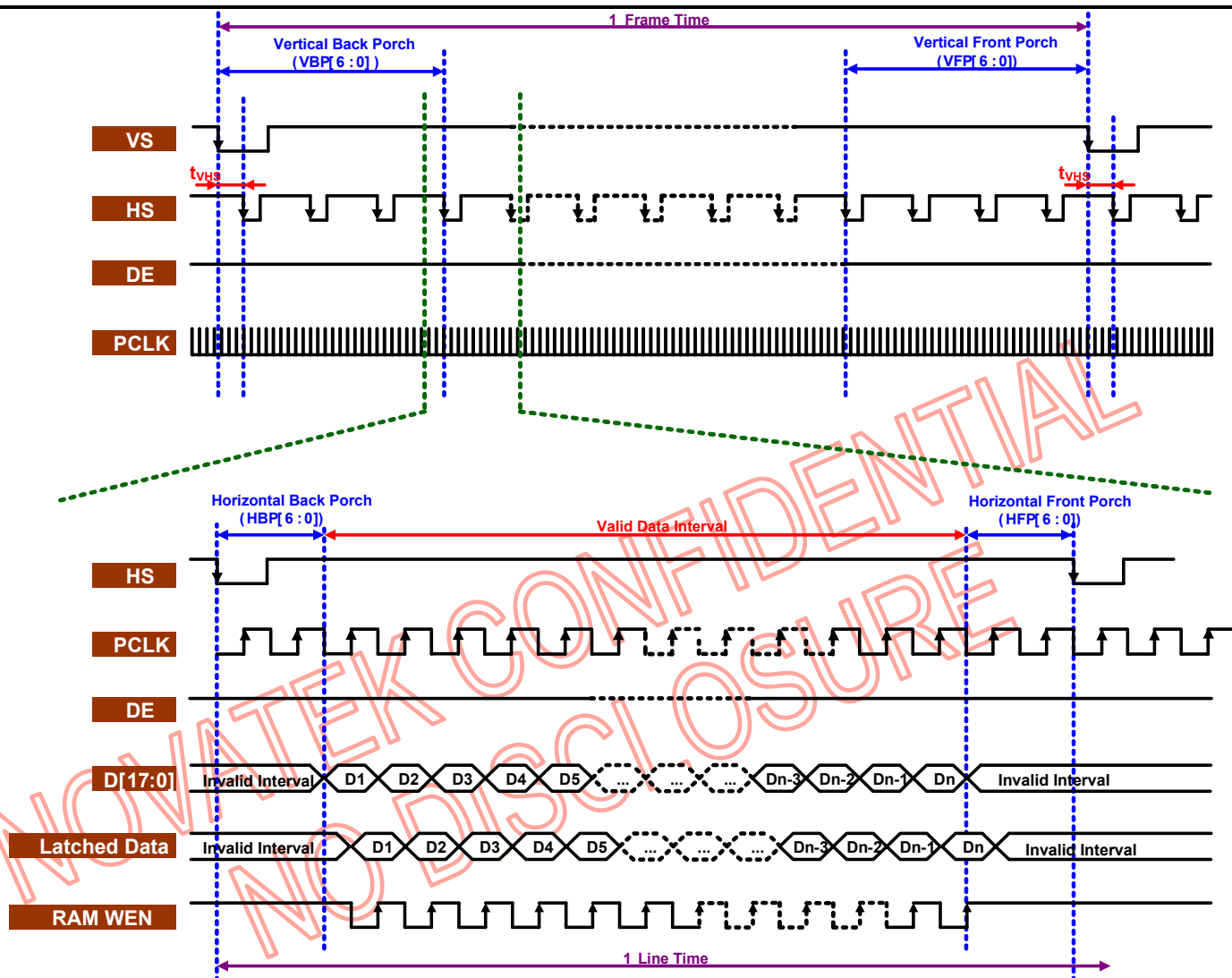
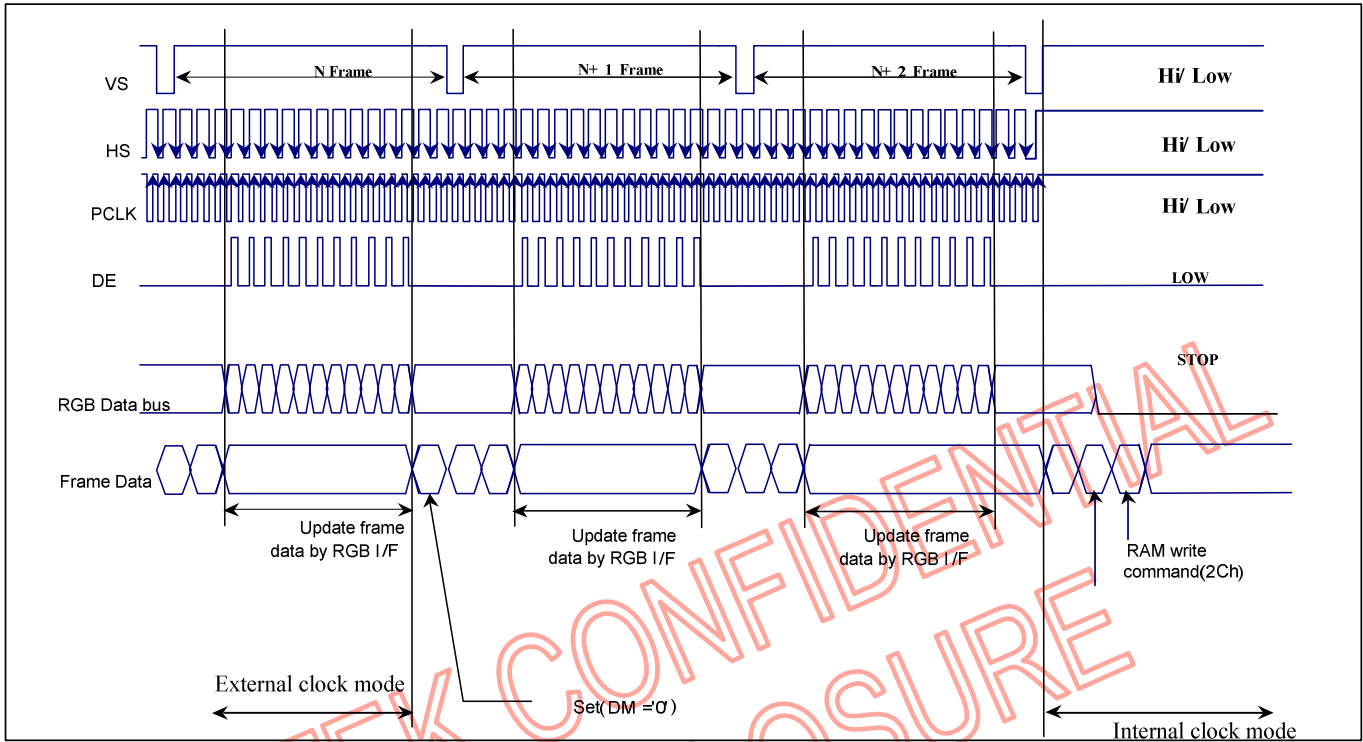
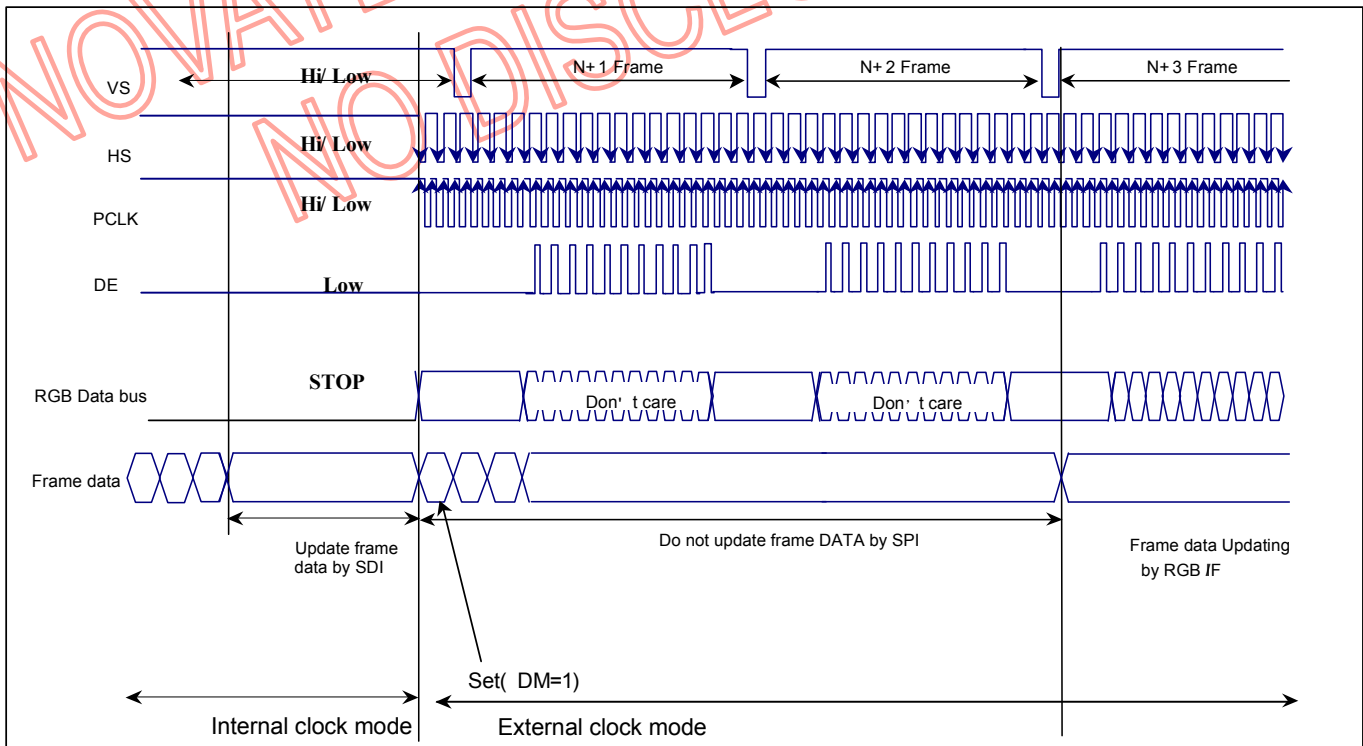


Figure 5.4.5.2 Video Signal Data Writing Method in RGB Mode 2 Interface

Constraint : Vporch (VBP \geq TBD , VFP \geq TBD , VBP > BP)

Note: tVHS \geq TBD


Figure 5.4.5.3 Enter Internal Clock mode(DM=0) Timing sequence

Figure 5.4.5.4 Exit Internal Clock mode(DM=1) Timing sequence

5.5 Frame Tearing Effect Interface

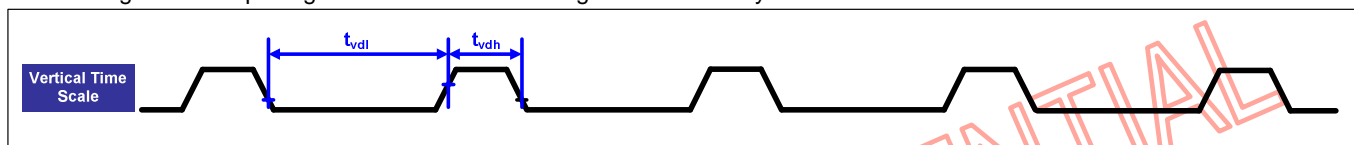
The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off and On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.5.1 Tearing Effect Line Modes

There are mode A, B and C for tearing effect line modes. Below figures are used to give examples based on 480 Horizontal lines condition.

Mode A

The Tearing Effect Output signal consists of V-Blanking Information only :

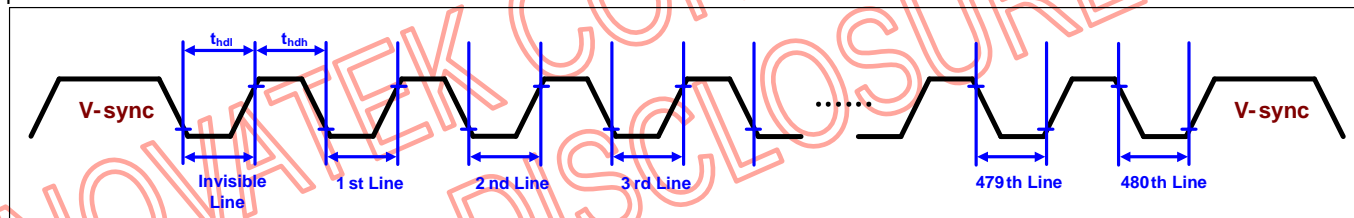


tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode B

The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one Mode A TE and 480H-sync pulses per field.



thh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

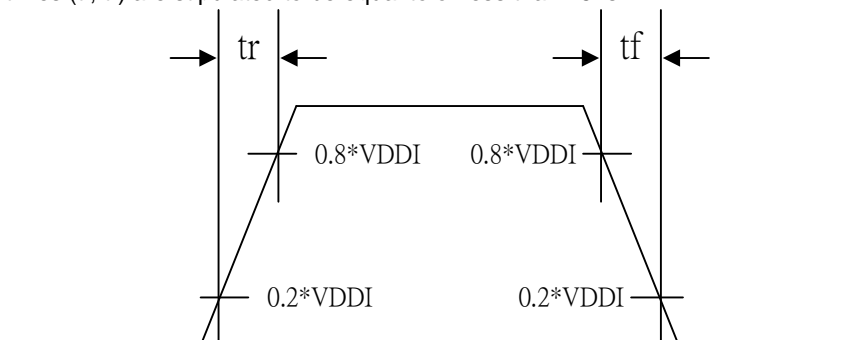
AC characteristics of Tearing Effect Signal

Idle Mode Off

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μ S	
thdl	Horizontal Timing Low Duration	16	-	μ S	
thdh	Horizontal Timing High Duration	-	500	μ S	

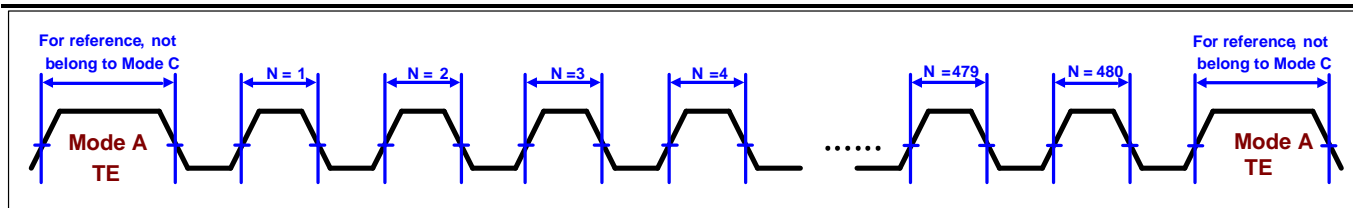
NOTE: This timings apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



Mode C

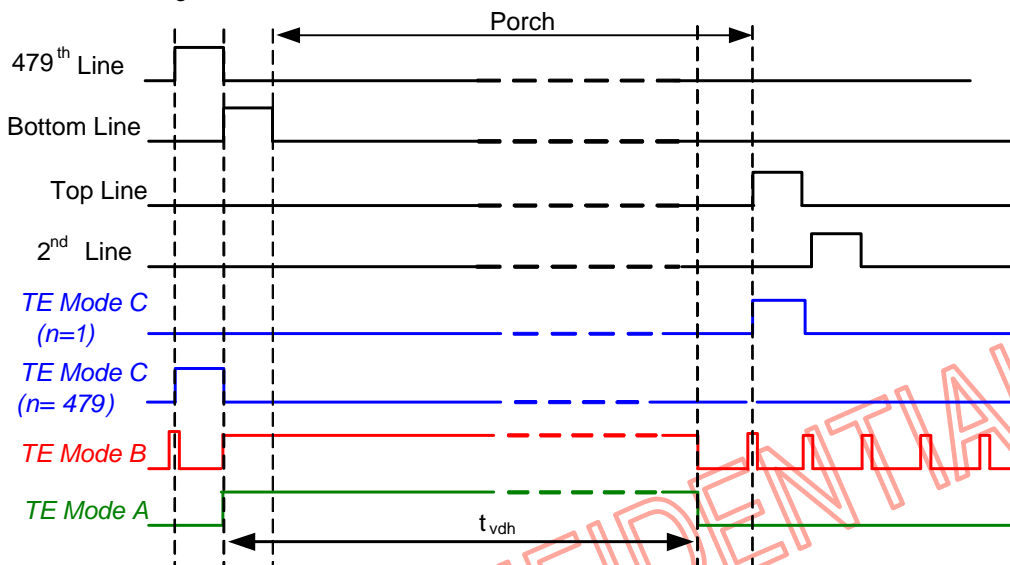
This mode turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



35h	44h	TE Output
M	N	
0	0	TE high in V-porch region (A)
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

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Mode A, Mode B, and Mode C timing chart is shown in below:



Note:

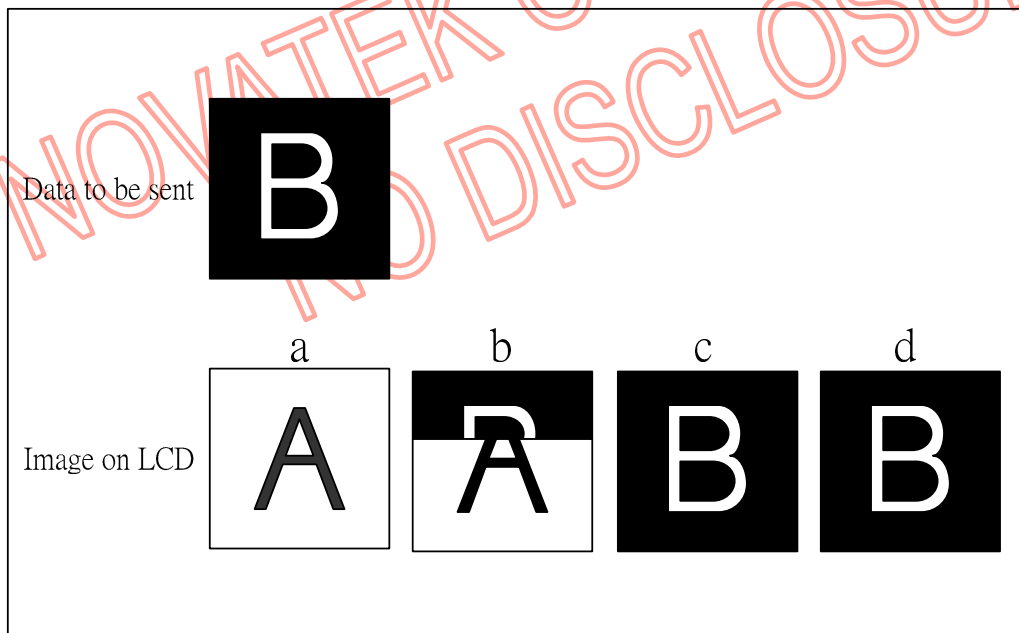
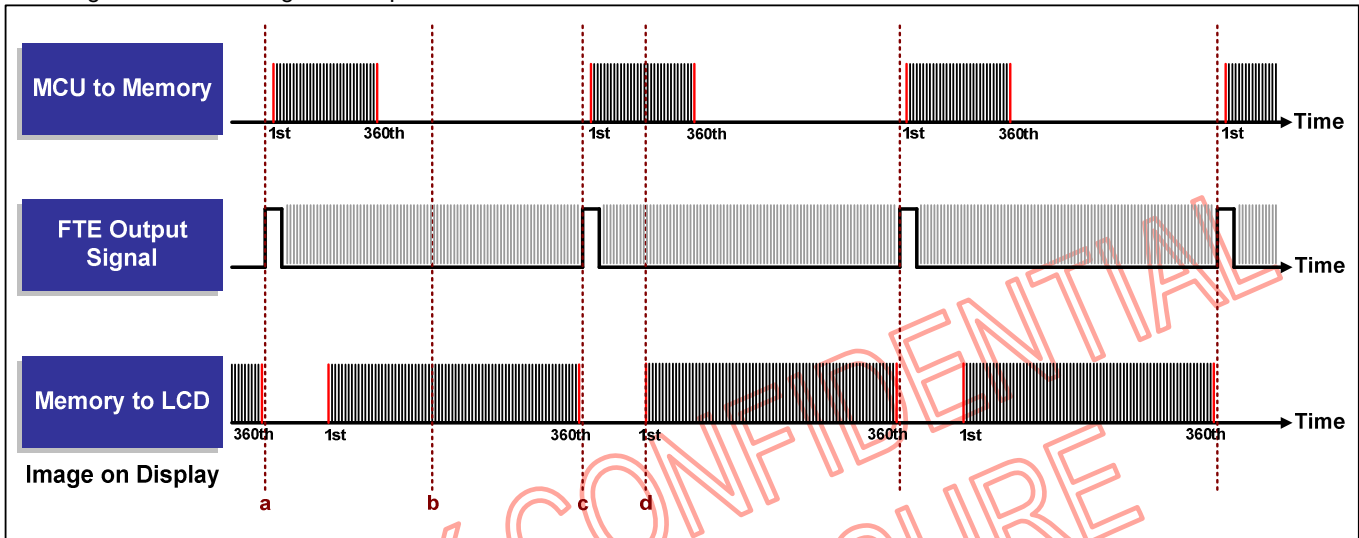
1. During sleep-in mode, the Tearing Output pin is active Low
2. $N \geq$ "Horizontal line number" will be ignore in TE mode C. "Horizontal line number" is decided by GM[2:0] pins.

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5.5.2 Example 1: MPU write is faster than panel read

Data write to Frame Memory is now synchronized to the panel scan (leading mode). It should be written next one horizontal sync pulse after FTE signal. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

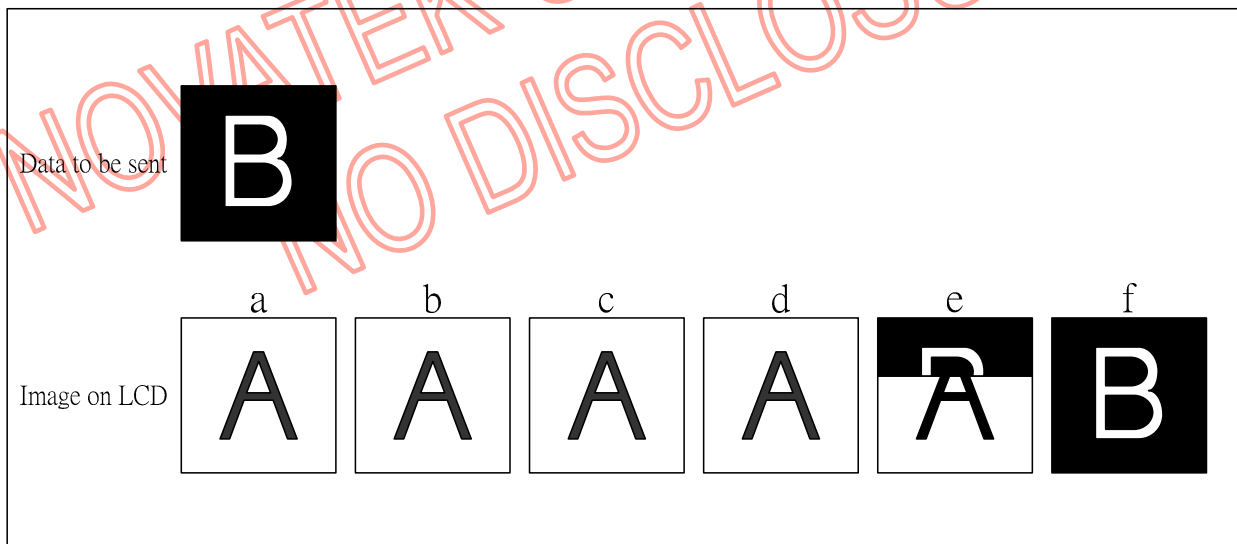
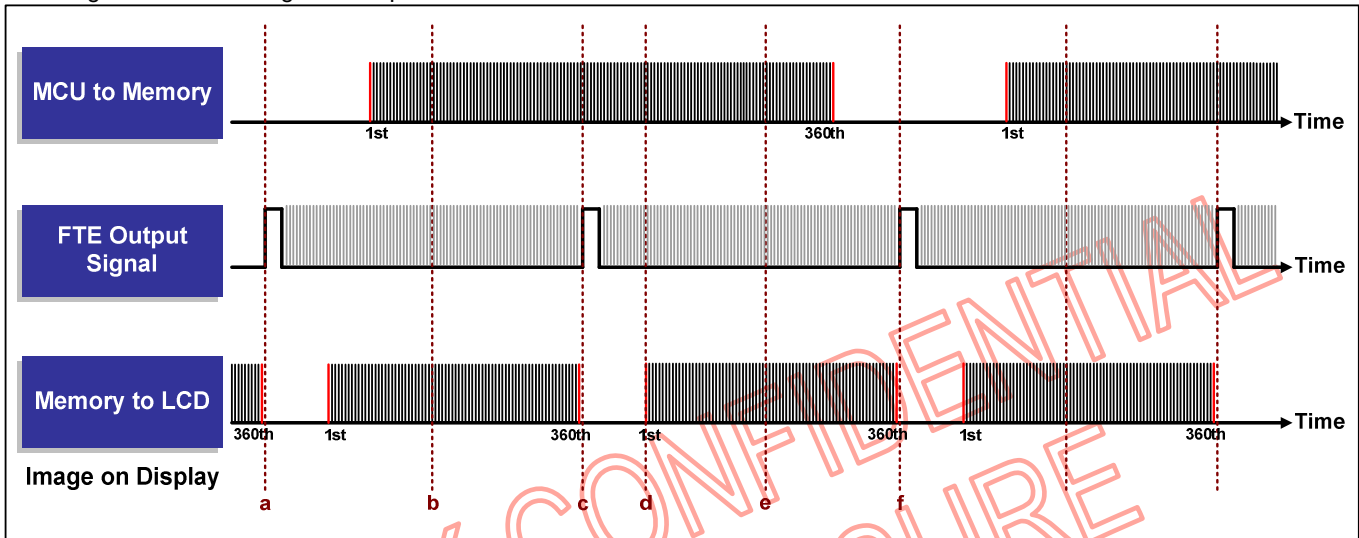
Below figures are used to give examples based on 360 Horizontal lines condition.



5.5.3 Example 2: MPU write is slower than panel read

The MPU to Frame Memory write begins just after Panel Read has commenced (lagging mode). This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

Below figures are used to give examples based on 360 Horizontal lines condition.



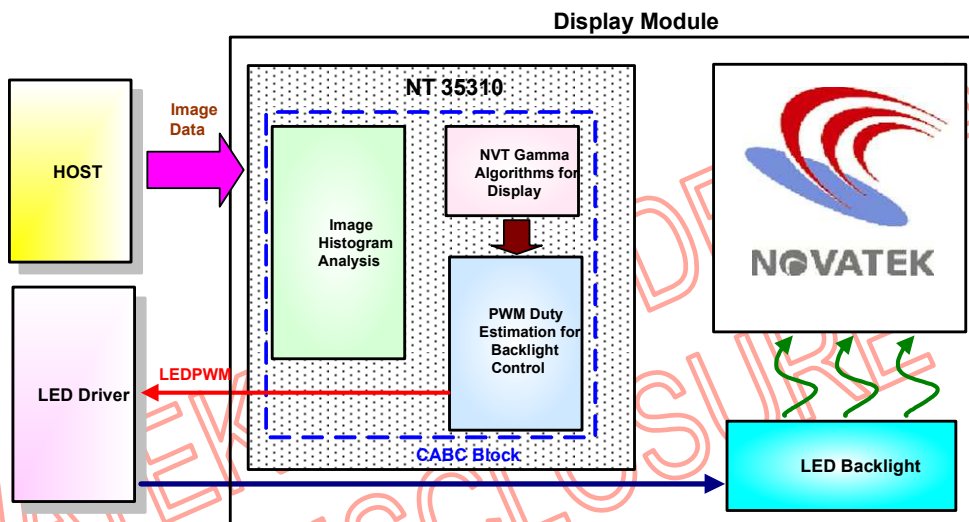
The TE interface has a minimum RAM write speed requirement. Therefore, the RAM Write Speed must be faster than the values calculated from the following formulas:TBD

5.4 Content Adaptive Brightness Control (CABC) function

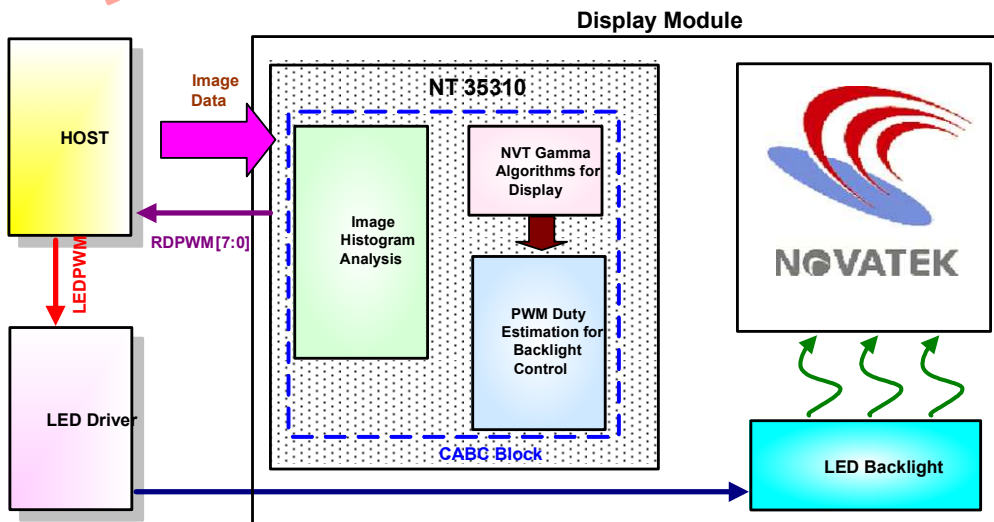
5.3.1 Dynamic Backlight Control Function

The NT35310 supports Backlight-Control function to control brightness of backlight and to process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image. The display image is dynamically controlled by CABC block. The availability of this function ranges from moving picture such as TV image to still picture such as menu. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image. The Backlight-Control function is supported for the following two architectures:

1. When bit BL of "Write CTRL Display (53h)" command is '1', the PWM signal is used to directly control the LED driver IC. The LED driver IC is controlled entirely via the NT35310.



2. When bit BL of "Write CTRL Display (53h)" command is '0', the host processor reads LED brightness information internally generated by CABC processing from the NT35310. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the NT35310.



5.3.1.1 CONTENT ADAPTIVE BRIGHTNESS CONTROL

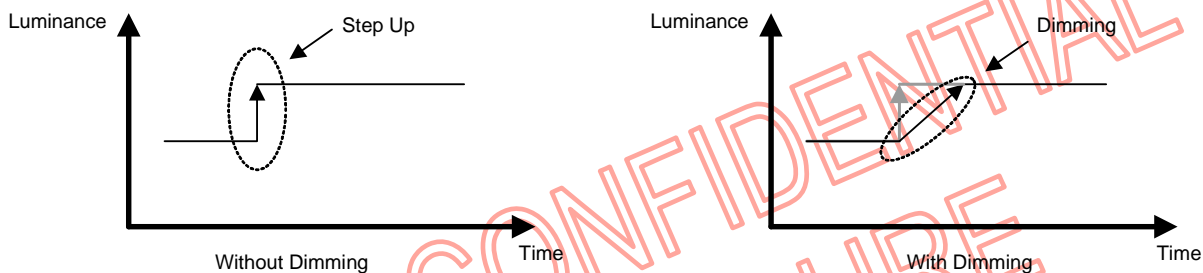
A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image.

This function and its different modes can be controlled. See command "Write Content Adaptive Brightness Control (55h)" (bit: 0 and 1) for more information. Definition of Modes:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

5.3.1.2 Display Backlight Dimming Control

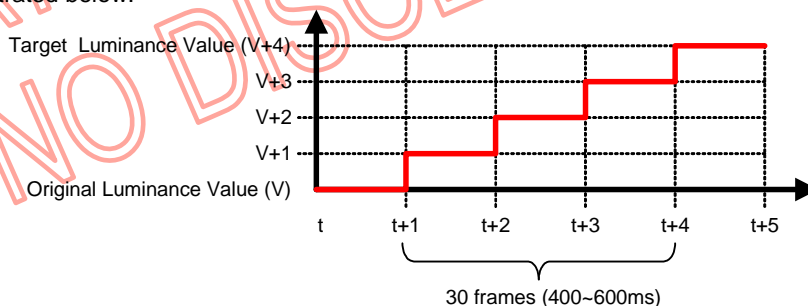
A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.



Dimming function can be enabled and disabled. See command "Write CTRL Display (53h)" (bits DD) for more information.

From the original brightness value to the target brightness value, the transferring time steps between these two brightness values are equal making the transition linear. The dimming function is working similarly in both upward and downward directions.

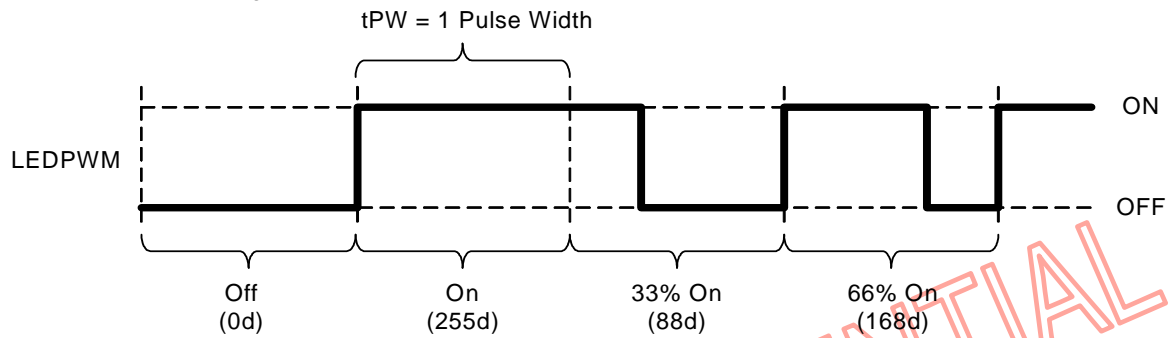
An upward example is illustrated below:



5.3.1.3 BRIGHTNESS CONTROL LINE

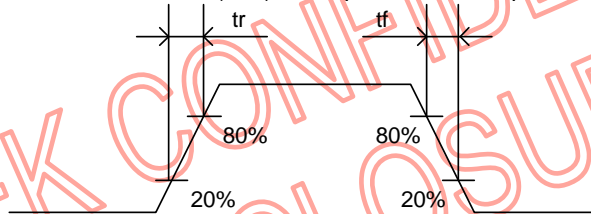
The brightness control (LEDPWM) line is sending control information to the display brightness control unit which can be a power supply for the display brightness.

The Brightness Control Line Timings are described below:



Symbol	Parameter	min	max	unit	description
tPW	Pulse Width	0.0333	8.33	ms	

Note: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



5.6 MDDI Interface (Mobile Display Digital Interface)

The NT35310 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following four lines: HSSI_D0_P/N and HSSI_CLK_P/N. The specifications of MDDI supported by the NT35310 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA). The NT35310 offers the Bi-direction Link to use for the register and display data read / write. For power saving, the NT35310 offers both Hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption. The NT35310 supports Type-1 of the MDDI specifications Version 1.2 and the application diagram is illustrated as Figure 5.6.1.

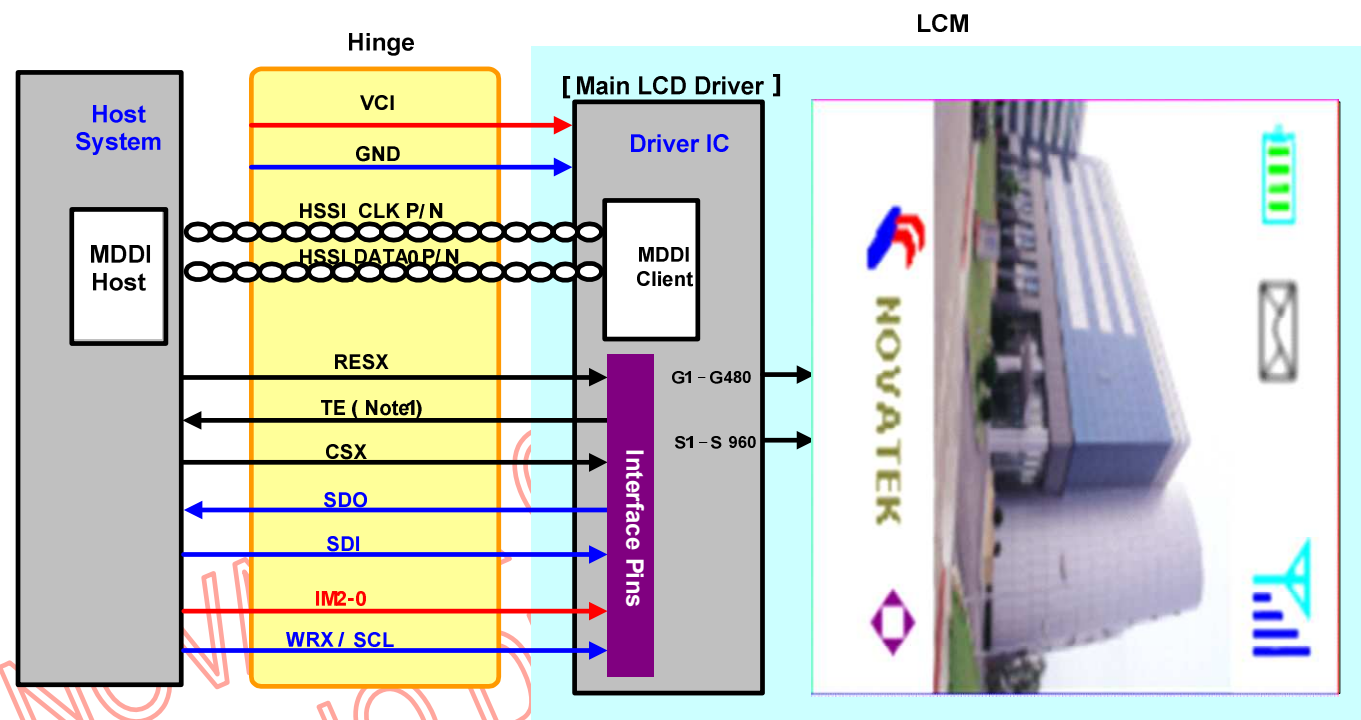


Figure 5.6.1 MDDI Interface Application

- Notes:
- (1) Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effort.
 - (2) When enter to the MDDI interface from other interface, the Host need to wait 100ms and can start to send any packet. For example wake up packet.
 - (3) After shutting down the MDDI interface the Host need to wait 500ns and can start to send wake up packet to wake up the MDDI link.

5.6.1 MDDI Link Protocol

The NT35310's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol. Do not send any packets that are not supported by the NT35310 into a system containing the NT35310. Supported MDDI packets are as follows:

Table 5.6.1 Summary of MDDI packets supported by the NT35310

NT35310 MDDI packets	Packet Name	Packet Type	Direction
Link Control Packet	Sub-frame Header Packet	15359 (0x3BFF)	Forward
	Filler Ppacket	0	Forward/Reverse
	Link Shutdown Packet	69 (0x45)	Forward
	Reverse Link Encapsulation Packet	65 (0x41)	Forward
	Round-trip Delay Measurement Packet	82 (0x52)	Forward
	Client Capability Packet	66 (0x42)	Reverse
	Client Request and Status Packet	70 (0x46)	Reverse
Register Access Packet	Register Access Packet	146 (0x92)	Forward/Reverse
Basic Media Stream Packet	Video Stream Packet	16 (0x10)	Forward

5.6.2 MDDI Link Packet descriptions

Sub-frame Header Packet:

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub- frame Header Packet								
Packet Length	Packet Type (0x3BFF)	Unique Word (0x005A)	Reserved1	Sub- frame Length	Protocol Version	Sub- frame Count	Media- frame Count	CRC
2 Bytes	2 Bytes	2 Bytes	2 Bytes	4 Bytes	2 Bytes	2 Bytes	4 Bytes	2 Bytes
Packet Contents : Packet Length: Packet length not including the packet length field Packet Type: Packet type is 0x3BFF Unique Word: Unique word is 0x005A Reserved 1 : Not used Sub - frame Length : Specify the number of bytes per sub - frame Bit [15 : 2]: Set it to zero Bit [1 : 0]: Sub - frame operational mode 00b- Sub - frame lengths strictly followed 01b- Sub - frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame lengths has been transmitted 10b - Sub - frame lengths are unlimited.No more sub - frame packets are required to be transmitted after the first sub - frame packet at startup Sub - frame Count Specify the number of sub - frame header packet Media - frame Count Specify the number of media - frames CRC: Error check								

Figure 5.6.2 Sub-frame Header Packet Structure

Filler Packet:

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

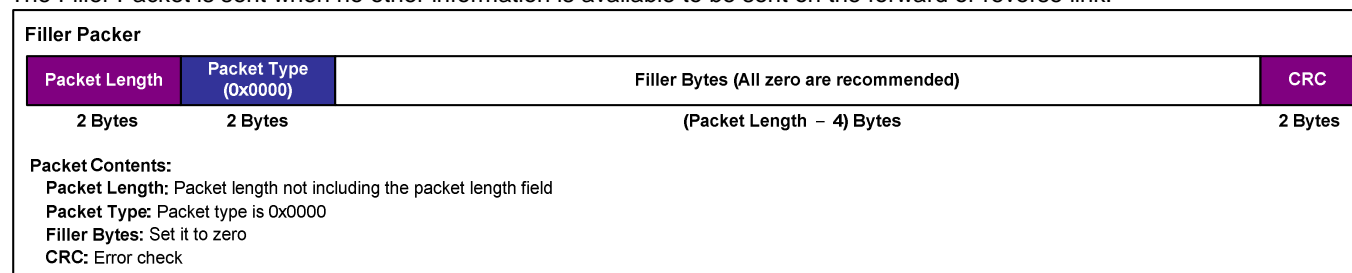


Figure 5.6.3 Filler Packet Structure

Link Shutdown Packet:

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.

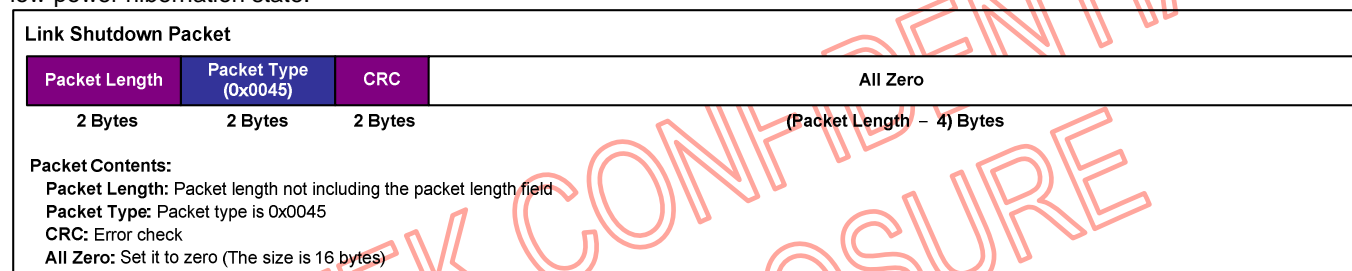


Figure 5.6.4 Link Shutdown Packet Structure

Reverse Link Encapsulation Packet:

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.

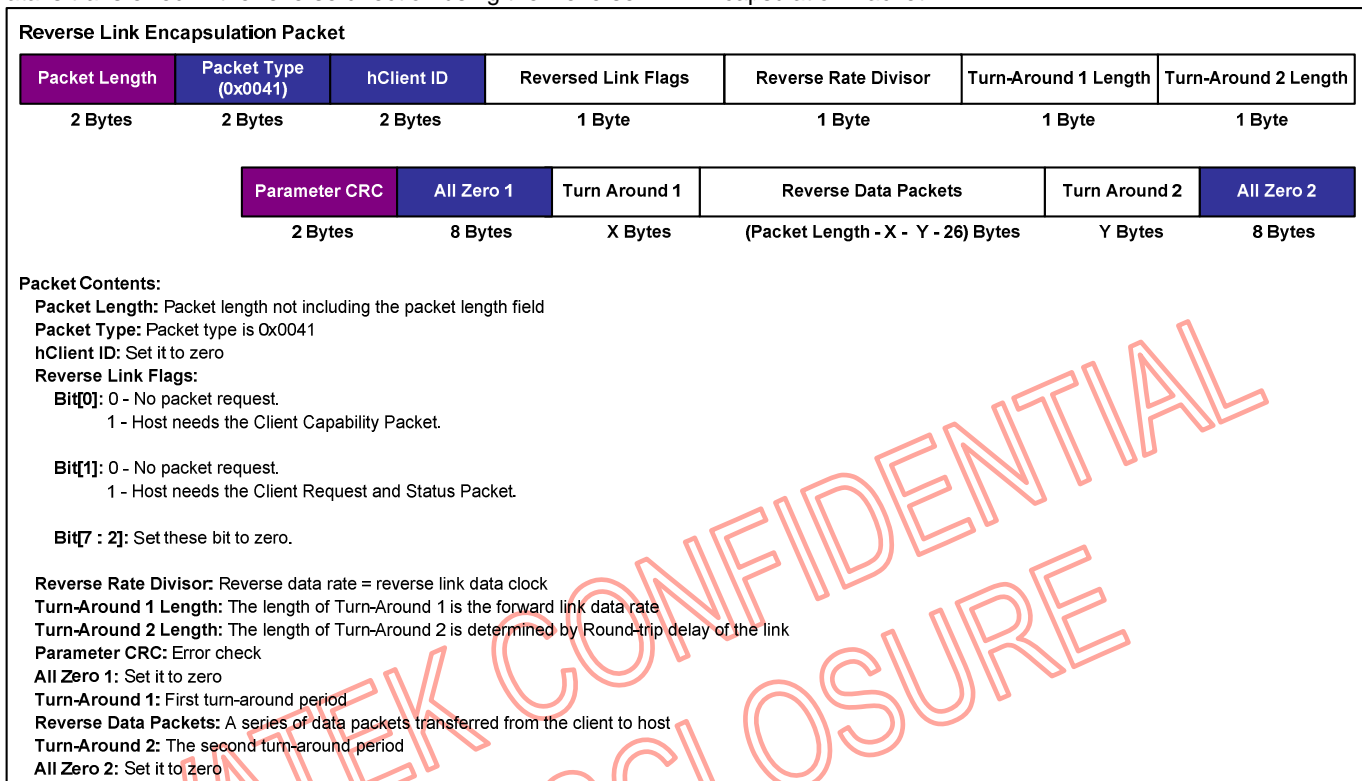


Figure 5.6.5 Reverse Link Encapsulation Packet

Round-Trip Delay Measurement Packet:

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

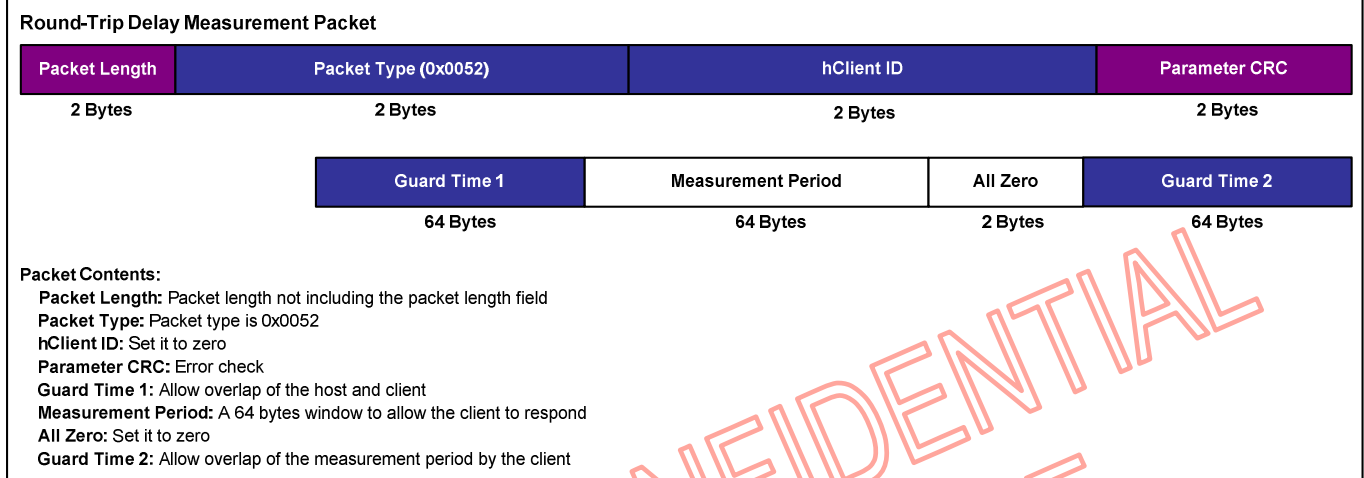


Figure 5.6.6 Round-Trip Delay Measurement Packet

The Figure 5.6.7 illustrates the timing of events during the Round-Trip Delay Measurement Packet.

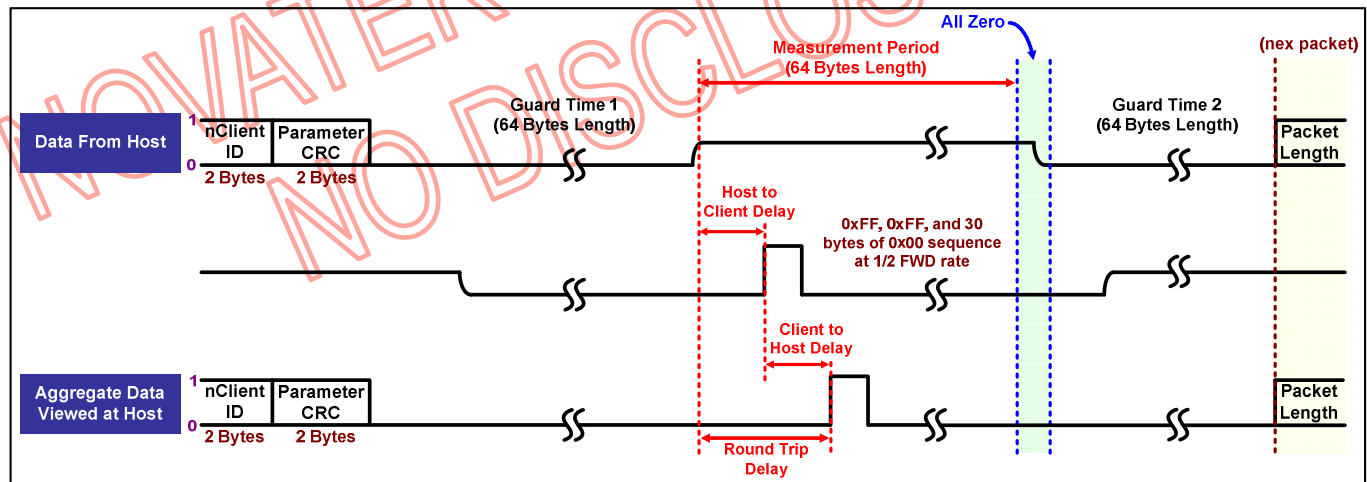


Figure 5.6.7 Round-Trip Delay Measurement Timing

Client Capability Packet:

It is recommended that the client send a Client Capability Packet to the host after forward link synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

Client Capability Packet							
Packet Length	Packet Type (0x0042)	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability	
2 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes	1 Byte	
Number of Alt Display	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size	
1 Byte	2 Bytes	2 Bytes	2 Bytes	2 Bytes	2 Bytes	4 Bytes	
Color Map RGB Width	RGB Capability	Monochrome Capability	Reserved 1	Y Cb Cr Capability	Bayer Capability	Reserved 2	
2 Bytes	2 Bytes	1 Byte	1 Byte	2 Bytes	2 Bytes	2 Bytes	
Client Feature Capability	Max Video Frame Rate	Min Video Frame Rate	Min Sub-frame Rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample Rate Capability	
4 Bytes	1 Byte	1 Byte	2 Bytes	2 Bytes	2 Bytes	2 Bytes	
Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name	
1 Byte	1 Byte	2 Bytes	1 Byte	1 Byte	2 Bytes	2 Bytes	
Product Code	Reserved 3	Serial Number	Week of Mfr	Year of Mfr	CRC		
2 Bytes	2 Bytes	4 Bytes	1 Byte	1 Byte	2 Bytes		

Packet Contents:

- Packet Length: Packet length not including the packet length field
- Packet Type: Packet type is 0x0042
- cClient ID: Set it to zero
- Protocol Version: Set it to 0x0002
- Min Protocol Version: Specify the minimum protocol version, set it to 0x0001
- Pre-Calibration Data Rate Capability: Specify the maximum data rate the client can receive (190h)
- Interface Type Capability: Set it to 0x00
- Number of Alt Displays: Set it to zero
- Post-Calibration Data Rate Capability: Specify the maximum data rate the client can receive (190h)
- Bitmap Width: Specify the width of the bitmap
- Bitmap Height: Specify the height of the bitmap
- Display Window Width: Specify the width of the display window
- Display Window Height: Specify the height of the display window
- Color Map Size: Set it to zero
- Color Map RGB Width: Set it to zero
- RGB Capability: Specify the resolution of RGB format (0x8666)
- Monochrome Capability: Set it to zero
- Reserved 1: Set it to zero
- Y Cb Cr Capability: Set it to zero
- Bayer Capability: Set it to zero
- Reserved 2: Set it to zero
- Client Feature Capability Indicators: 0x004C8000
- Maximum Video Frame Rate Capability: Specify the maximum video frame (3Ch)
- Minimum Video Frame Rate Capability: Specify the minimum video frame (00h)
- Minimum Sub-frame Rate: Specify the minimum sub-frame rate (0x01)
- Audio Buffer Depth: Set it to zero
- Audio Channel Capability: Set it to zero
- Audio Sample Rate Capability: Set it to zero
- Audio Sample Resolution: Set it to zero
- Mic Audio Sample Resolution: Set it to zero
- Mic Sample Rate Capability: Set it to zero
- Keyboard Data Format: Set it to zero
- Pointing Device Data Format: Set it to zero
- Content Protection Type: Set it to zero
- Mfr Name: Set it to 0xB9F6
- Product Code: Set it to 0x5310
- Reserved 3: Set it to zero
- Serial Number: Set it to zero
- Week of Manufacture: Set it to zero
- Year of Manufacture: Set it to 0x0C
- CRC: Error check

Figure 5.6.9 Client Capability Packet

Client Request and Status Packet:

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Packet Length	Packet Type (0x0046)	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 Bytes	2 Bytes	2 Bytes	2 Bytes	1 Byte	1 Byte	2 Bytes	2 Bytes

Packet Contents:

Packet Length: Packet length not including the packet length field

Packet Type: Packet type is 0x0046

cClient ID: Set it to zero

Reverse Link Request: Specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.

CRC Error Count: Count the number of CRC errors occurred

Client Status:

- Bit[0]:** 1 - Capability has changed
0 - Capability has not changed
- Bit[1]:** Indicates the client has detected an error
- Bit [7 : 2]:** Set it to zero

Client Busy Flags:

- Bit[0]:** Bitmap block transfer function is busy
- Bit[1]:** Bitmap area fill function is busy
- Bit[2]:** Bitmap pattern fill function is busy
- Bit[3]:** The graphics subsystem is busy
- Bit[15 : 4]:** Set it to one

CRC: Error check

Figure 5.6.10 Client Request and Status Packet

Register Access Packet:

Register Access Packet is utilized when setting instruction to the NT35310. This packet cannot be used for RAM access..

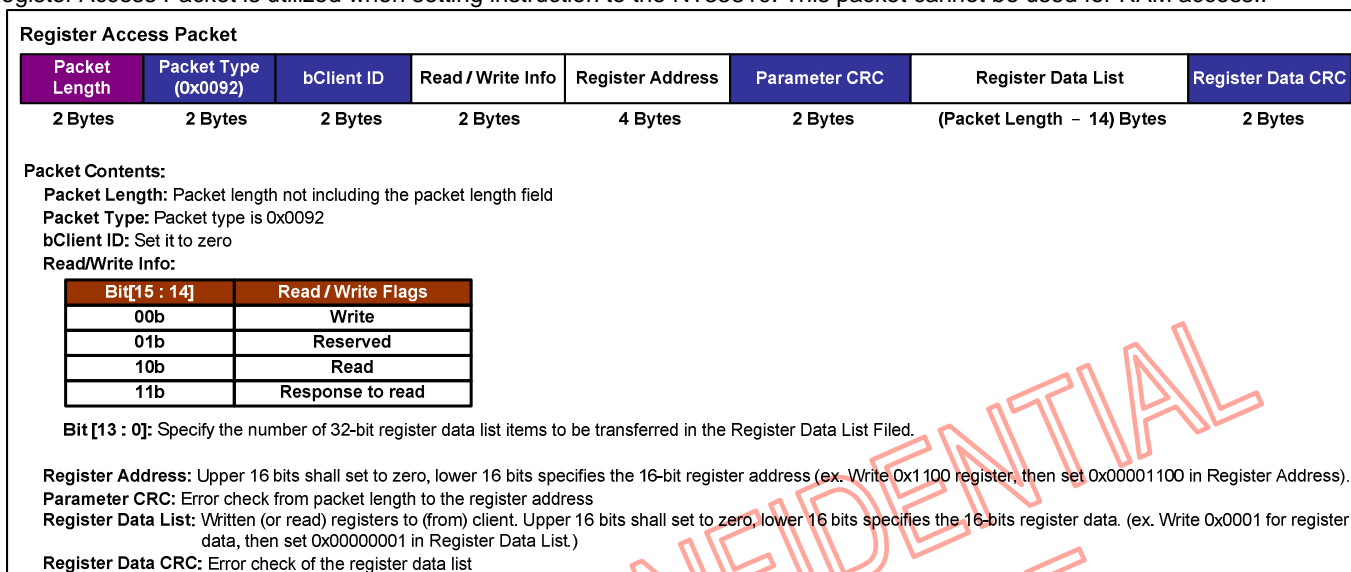


Figure 5.6.11 Register Access Packet

Multi Register Write Packet

Multi Register Access Packet

Packet Length	Packet Type (0x0092)	bClient ID	Read / Write Info	Register Address (= 0x80000000)	Parameter CRC	Register Data List	Register Data CRC
2 Bytes	2 Bytes	2 Bytes	2 Bytes	4 Bytes	2 Bytes	(Packet Length - 14) Bytes	2 Bytes

Packet Contents:

Packet Length: Packet length not including the packet length field

Packet Type: Packet type is 146 (0x0092)

bClient ID: Set it to zero

Read/Write Info:

Bit[15 : 14]	Bit[13 : 0]	Read / Write Flags
00b	0xnn	The number of Register Write (Register Address + Register Data)

Register Address: If the parameter of Register Address set to 0x80000000, Multi Register Write Packet is selected. Multiple register can be written at one packet. The number of write registers is defined on parameter "Read/Write Info"

Parameter CRC: Error check from packet length to the register address

Register Data List: Written (or read) registers to (from) client

Bit[31 : 16]	Bit[15 : 0]	Function Description
Register Address ID[15 : 0]	Register Data IB[15 : 0]	Both index and instruction set are stored in Register Data so that consecutive instruction setting is possible without setting the index in Register Address each time instructions are transferred.

Register Data CRC: Error check of the register data list

Multi Register Write Packet Example (1 Command Writing)

Packet Length	Packet Type (0x0092)	Client ID	Read / Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 Bytes	2 Bytes	2 Bytes	2 Bytes	4 Bytes	2 Bytes	4 Bytes	2 Bytes
0x0012	0x0092	0x0000	0x0001	0x80000000	CRC	Upper: ID1[15 : 0] Lower: IB1[15 : 0]	CRC

Multi Register Write Packet Example (2 Command Writing)

Packet Length	Packet Type (0x0092)	Client ID	Read / Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 Bytes	2 Bytes	2 Bytes	2 Bytes	4 Bytes	2 Bytes	8 Bytes	2 Bytes
0x0016	0x0092	0x0000	0x0002	0x80000000	CRC	Upper: ID1[15 : 0] Lower: IB1[15 : 0] Upper: ID2[15 : 0] Lower: IB2[15 : 0]	CRC

Figure 5.6.12 Multi Register Access Packet

Video Stream Packet

The NT35310 supports the Video Stream Packet to transfer display data including RGB data to RAM.

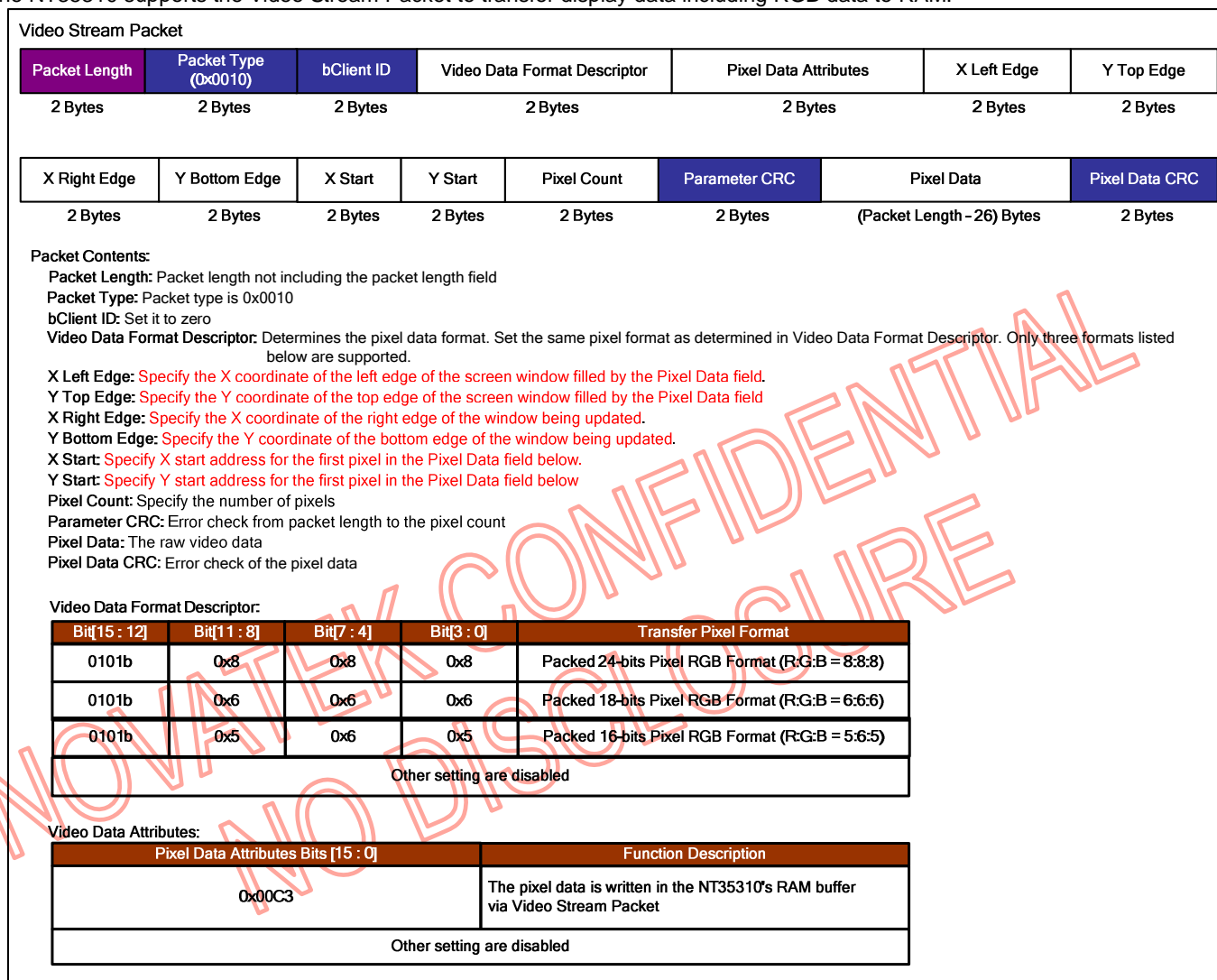


Figure 5.6.13 Video Stream Packet

Table 5.6.2 Pixel Data Format

MDDI Data Byte		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Colors
R G B 5 : 6 : 5	Byte N-th	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	65K Colors (1 Pixel / 16-bits RGB Format)
	Byte (N + 1)-th	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	
R G B 6 : 6 : 6	Byte N-th	G1[1]	G1[0]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	262K Colors (1 Pixel / 18-bits RGB Format)
	Byte (N + 1)-th	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	
	Byte (N + 2)-th	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	R1[5]	R1[4]	
	Byte (N + 3)-th	R2[1]	R2[0]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	
	Byte (N + 4)-th	B3[3]	B3[2]	B3[1]	B3[0]	R2[5]	R2[4]	R2[3]	R2[2]	
	Byte (N + 5)-th	G3[5]	G3[4]	G3[3]	G3[2]	G3[1]	G3[0]	B3[5]	B3[4]	
R G B 8 : 8 : 8	Byte N-th	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	16.7M Colors (1 Pixel / 24-bits RGB Format)
	Byte (N + 1)-th	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	
	Byte (N + 2)-th	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	

Note:

NT35310 can accept 8-8-8 pixel format Video stream packet in MDDI I/F. However, due to NT35310's RAM buffer is 18 bits depth per pixel, also the Source driver is 6 bits per channel, therefore only MSB 6 bits of each R/G/B sub-pixel can be stored in memory and displayed in LCD panel.

5.6.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.

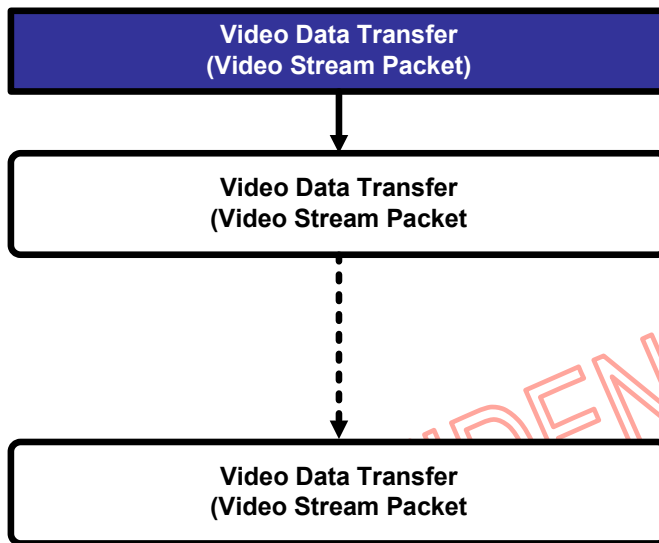


Figure 5.6.14 Writing Video Data to Memory Sequence

5.6.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.



Figure 5.6.15 Writing Register Sequence

5.6.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel Only), the following sequence should be programmed. Memory read command (2E00h) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

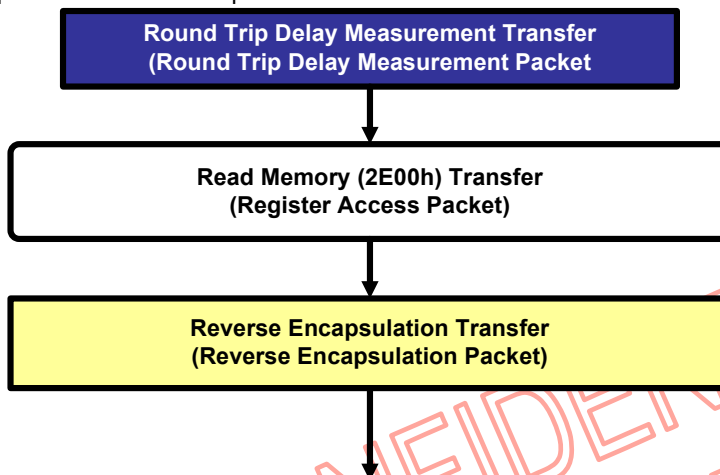


Figure 5.6.16 Reading Video Data from Memory Sequence

5.6.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. MDDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

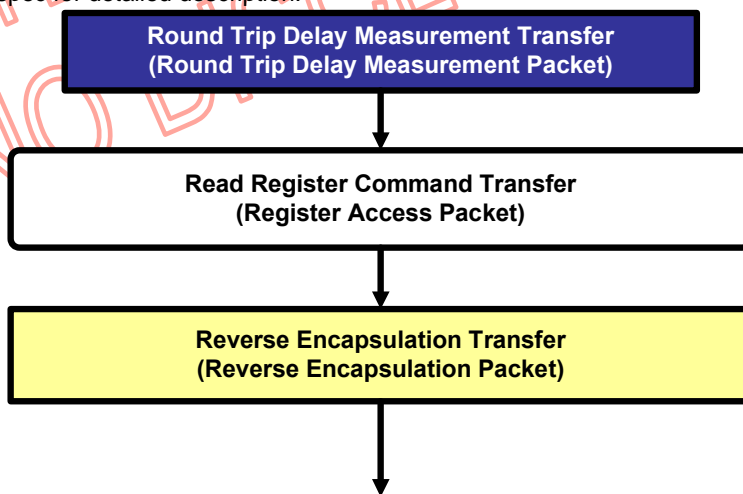


Figure 5.6.17 Reading Register Sequence

5.6.7 Hibernation Setting

The Client MDDI of the NT35310 provides a Hibernation setting. The methods for waking up the Hibernation mode can be determined based on actual usage.

Table 5.7.3 Hibernation Wake-up

Wake-up	Condition
Host-Initiated Wake-up	Wake up the MDDI link by MDDI Host
FTE-Initiated Wake-up	Use the FTE to wake up the MDDI link

Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained.

Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

Hibernation Setting Sequence:

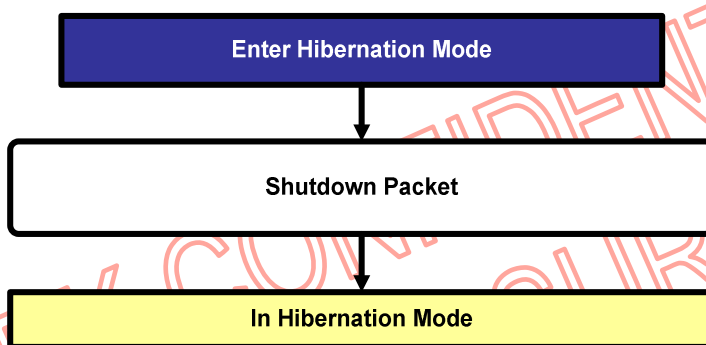


Figure 5.6.18 Hibernation Setting Sequence

Hibernation Wake-up Sequence:

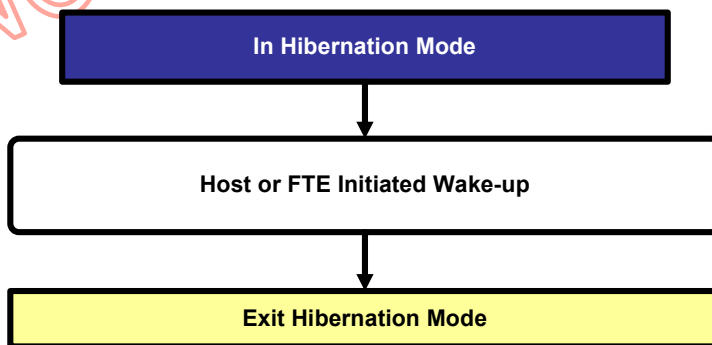


Figure 5.6.19 Hibernation Wake-up Sequence

5.6.8 Deep Standby Mode Setting by MDDI

The Client MDDI of the NT35310 includes a deep standby mode setting so it can enter a standby state and reduce power consumption during Hibernation mode. The MDDI enters Hibernation mode when a Shutdown Packet is sent. The standby power needs of the Client MDDI can be reduced, even while the MDDI Link is maintained in Hibernation mode.

When entering deep standby mode, the NT35310 stops operation rather than maintaining Hibernation mode. Input low pulse 3 msec from RESX pin to cancel deep standby mode, after which a Host-Initiated Wake-up should cancel the Hibernation mode. When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled. Follow the sequence indicated in the VESA MDDI specifications when initiating or canceling the Hibernation mode.

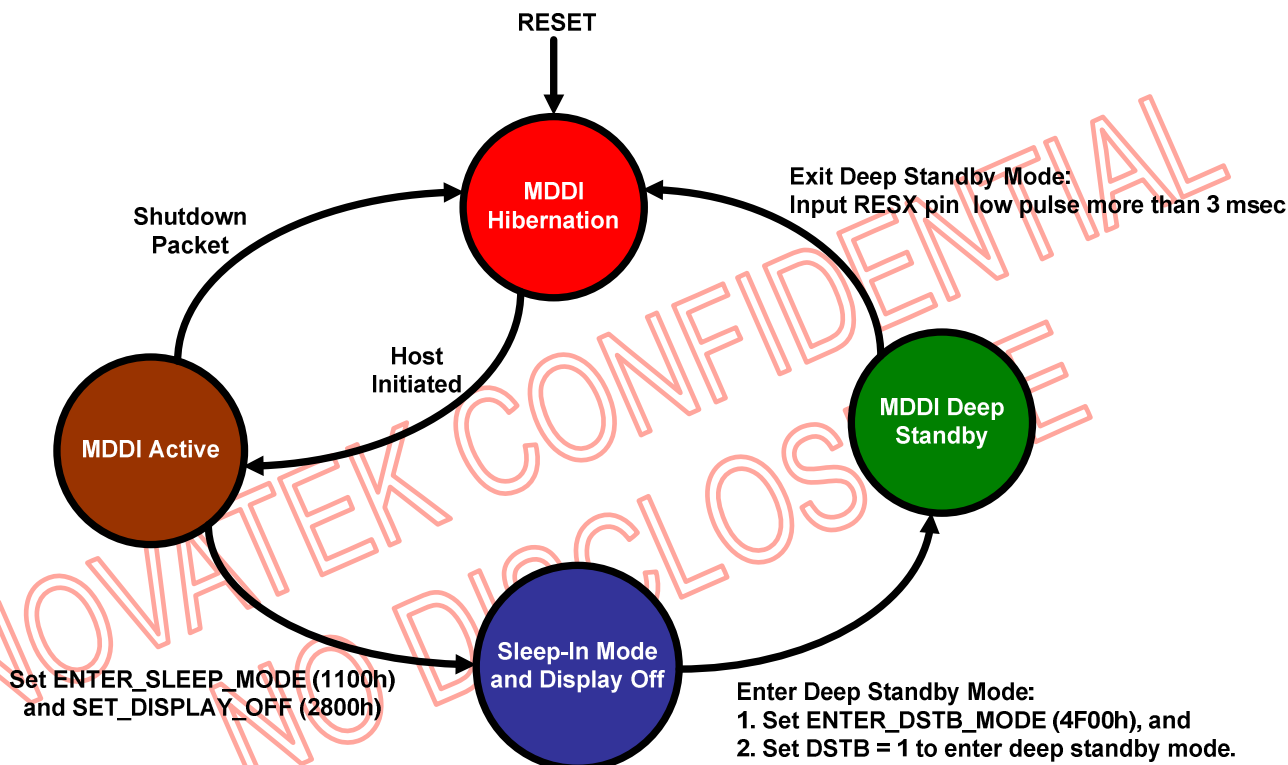
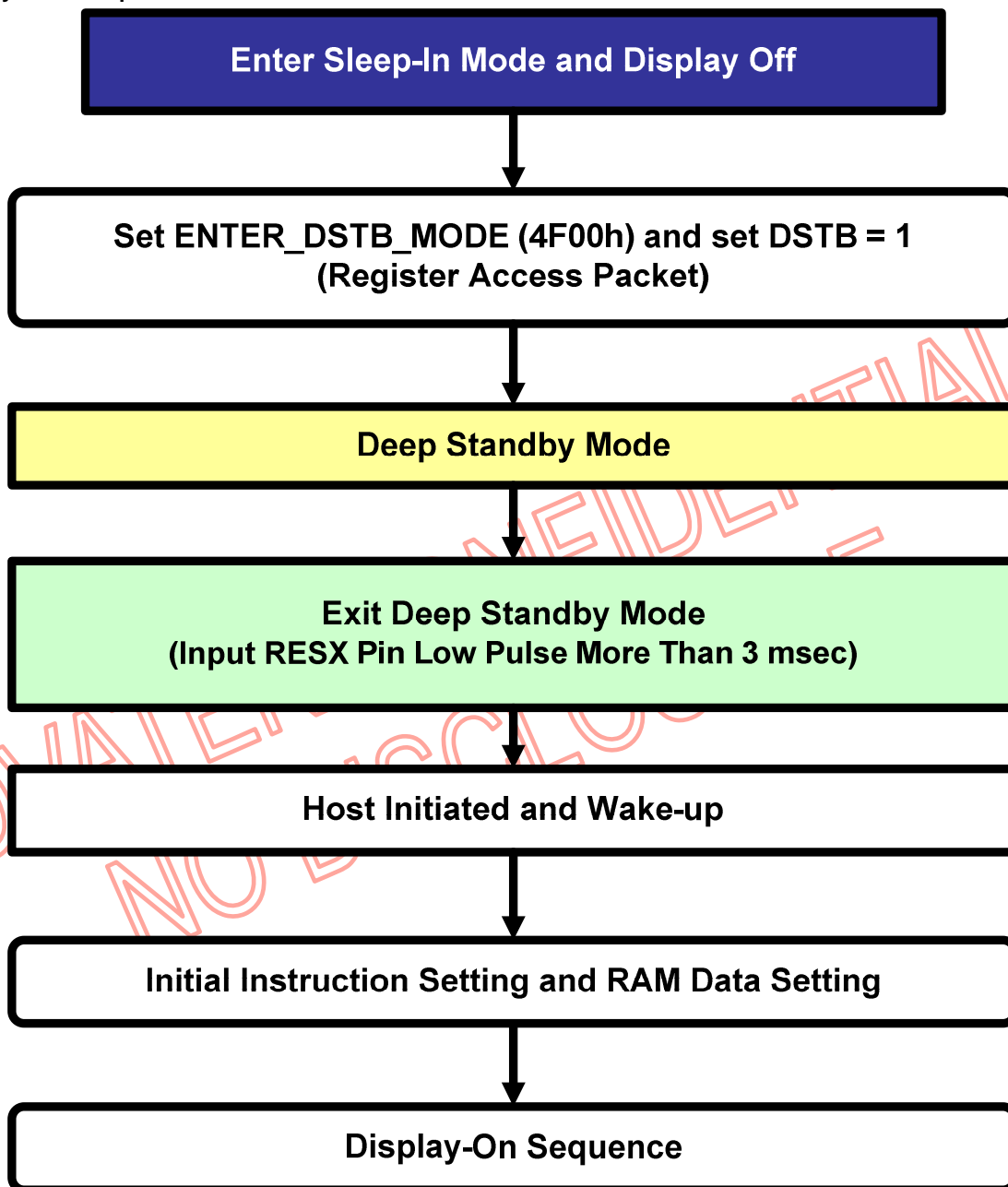


Figure 5.6.20 State Transitions in Deep Standby Mode

Note: When the NT35310 is in the MDDI Hibernation mode or MDDI deep standby mode, both the links are in the link hibernation states.

Deep Standby Mode Sequence

Figure 5.6.21 Deep Standby Mode Sequence

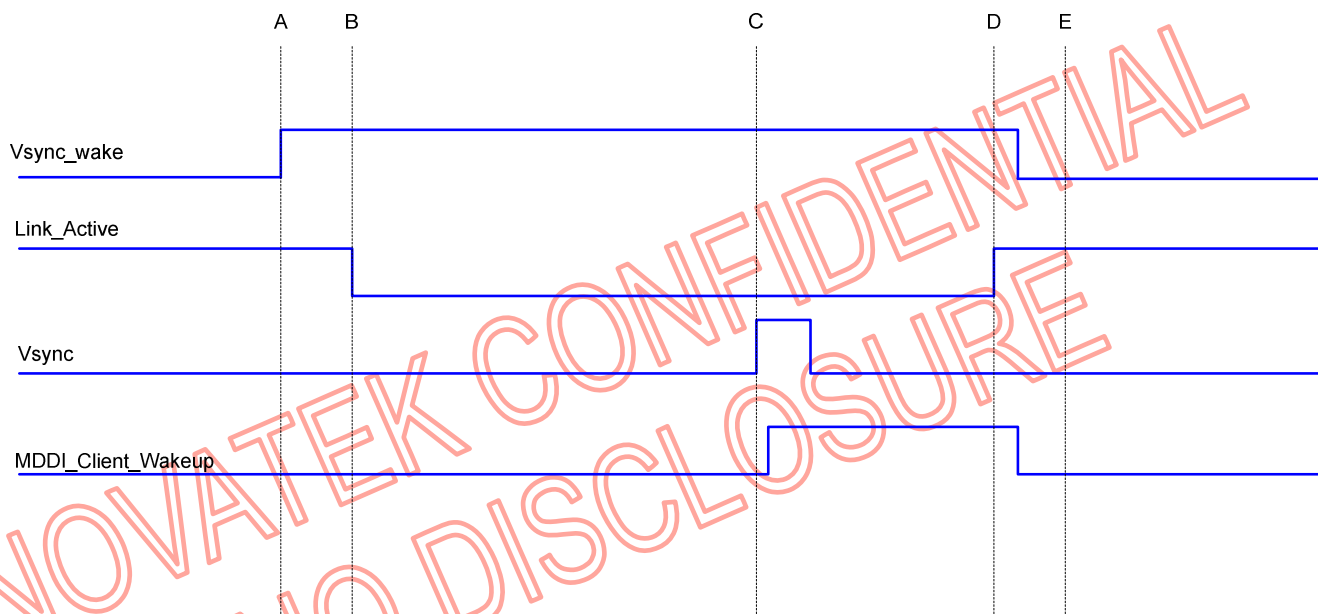
Note: When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

5.6.9 Vsync Based Link Wakeup

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register(0xAD00: VWAKE_EN) is set, followed by host set the link into hibernation, client initiated wake-up is executed in synchronization with the internal vertical-sync signal which generated in NT35351. Using VSYNC based link wake-up, tearingless display can be accomplished if interface speed and wake-up time is well known.

The diagram illustrait a wakeup based on a VSYNC wakeup request.



- (A) MDDI host write to the VSYNC wakeup register(0xAD00 : VWAKE_EN) to enable a wakeup based on Vsync.
- (B) Link_Active goes low when the host puts the link into hibernation after all data has been sent to client.
- (C) Vsync signal goes high indicating that update pointer has wrapped around, and Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.
- (D) Link_Active goes high after the host brings the link out of hibernation.
- (E) As the Link_Active goes high, MDDI_Client_Wakeup signal and the VSYNC based link wake-up register(0xAD00: VWAKE_EN) are cleared.

5.7 MIPI Interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

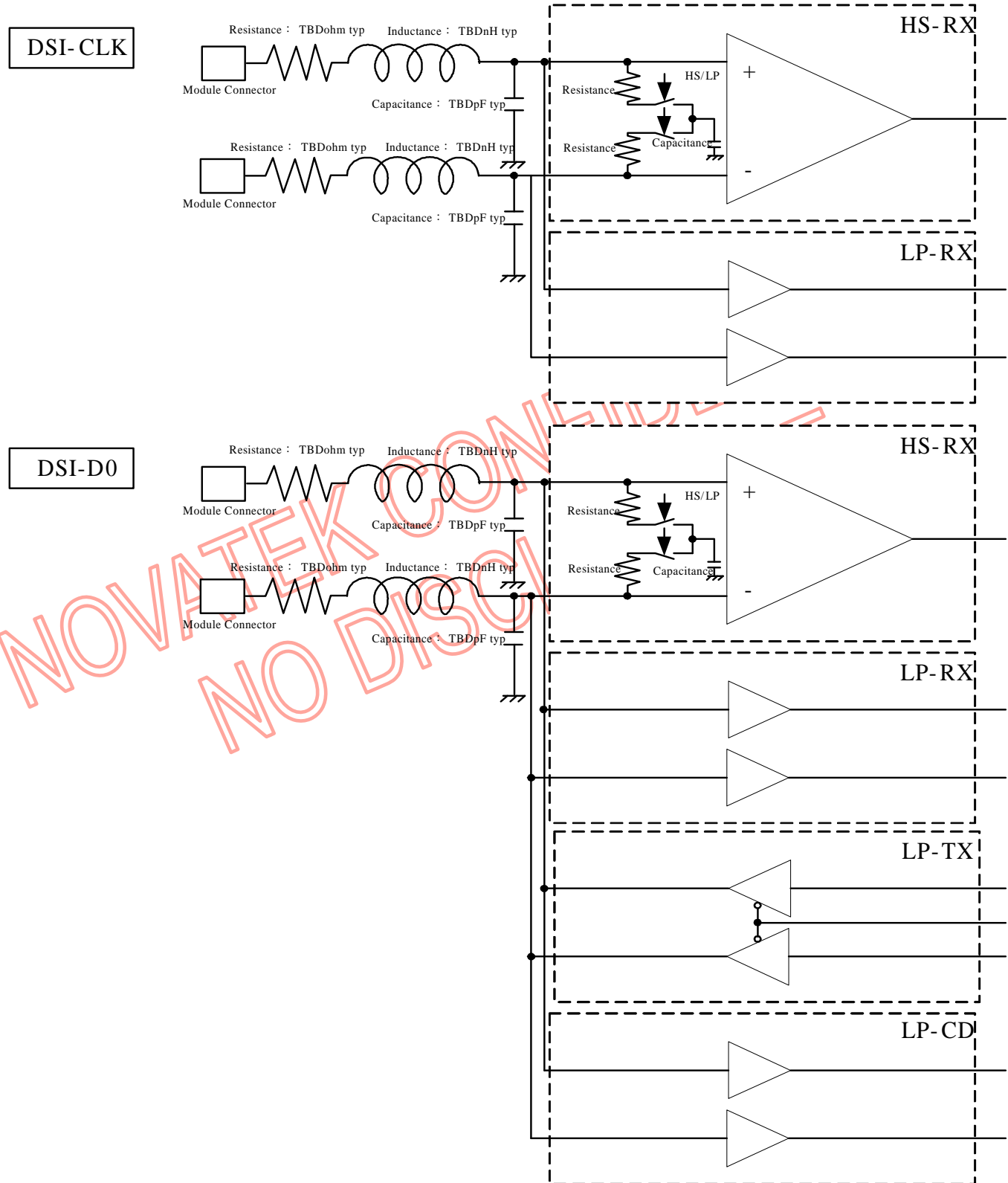
Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane <ul style="list-style-type: none"> ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0	Bi-directional Lane <ul style="list-style-type: none"> ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT

5.7.1 Display Module Pin Configuration for DSI


5.7.2 Display Serial Interface (DSI)

5.7.2.1 General Description

Communication sequences between the MCU and the display module are described on chapter “5.8.2.3.3 Communication Sequences”. The communication can be separated 2 different levels between the MCU and the display module:

Low level communication what is done on the interface level

High level communication what is done on the packet level

5.7.2.2 Interface Level Communication

5.7.2.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-3M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

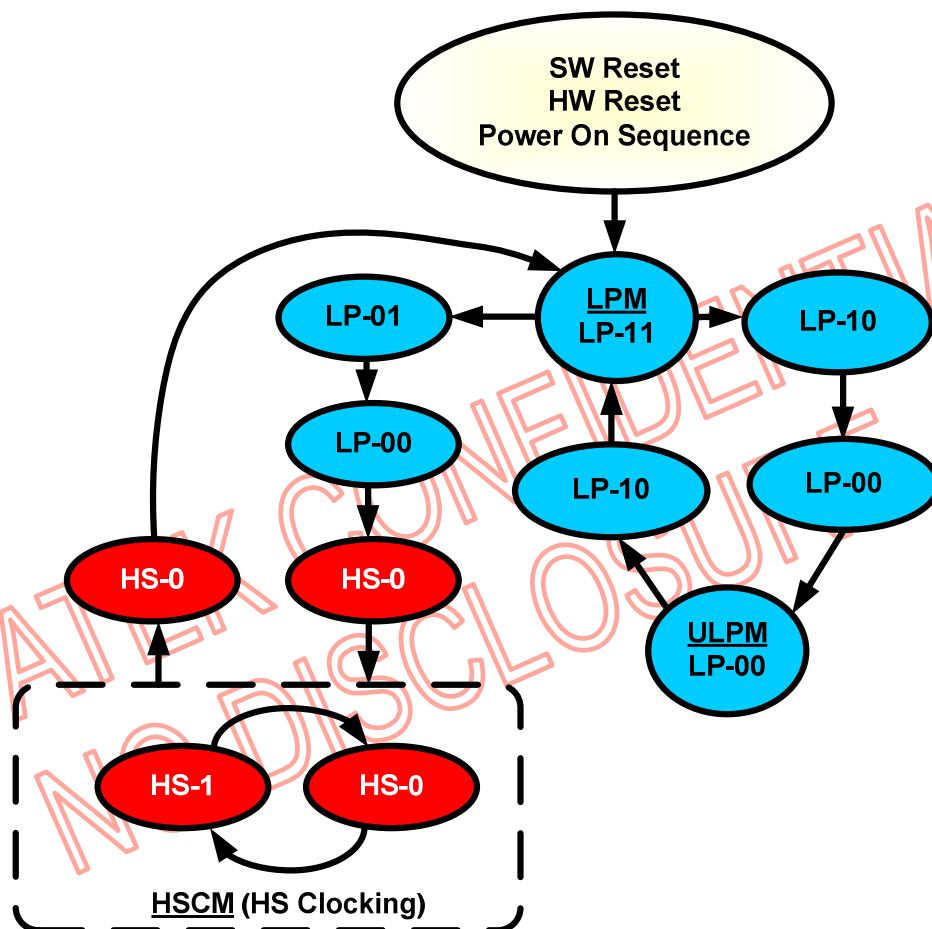
Lane Pair State Code	Line DC Voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dx+ - line	Dx- - line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

5.7.2.2.2 DSI-CLOCK Lane

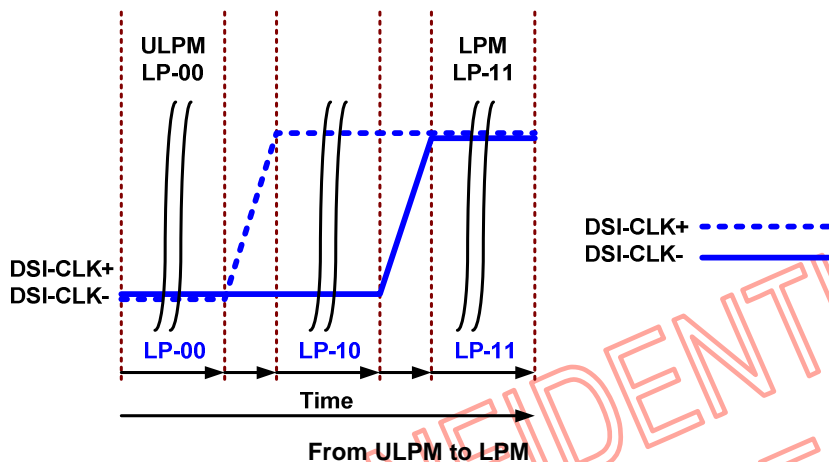
DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences. The principle flow chart of the different clock lanes power modes is illustrated below


Figure 5.7.1 Clock Lanes Power Mode

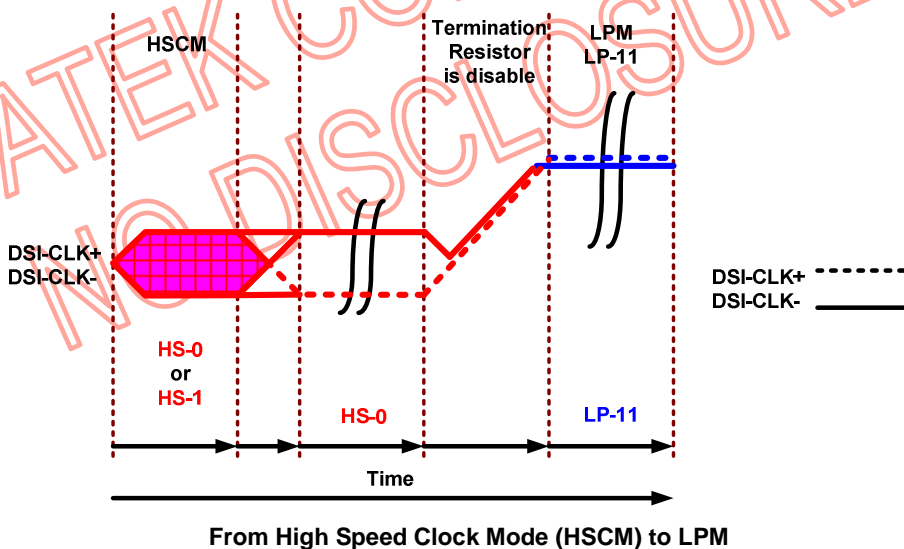
5.7.2.2.1 Low Power Mode (LPM)

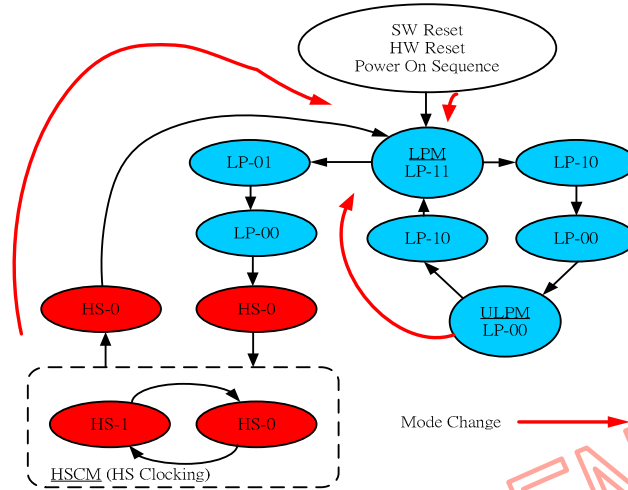
DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- (1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- (2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



- (3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.



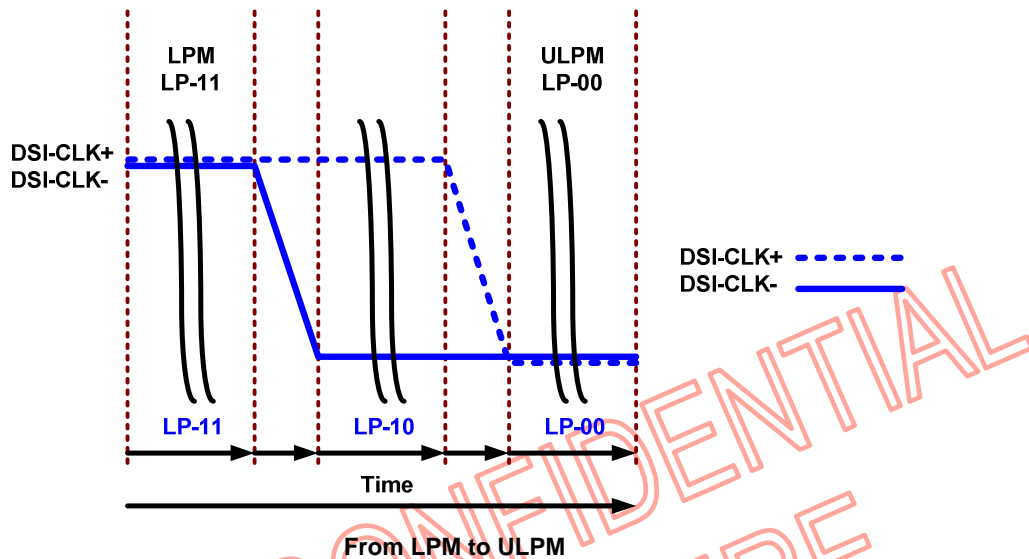


All Three Mode Changes to LPM on the Flow Chart

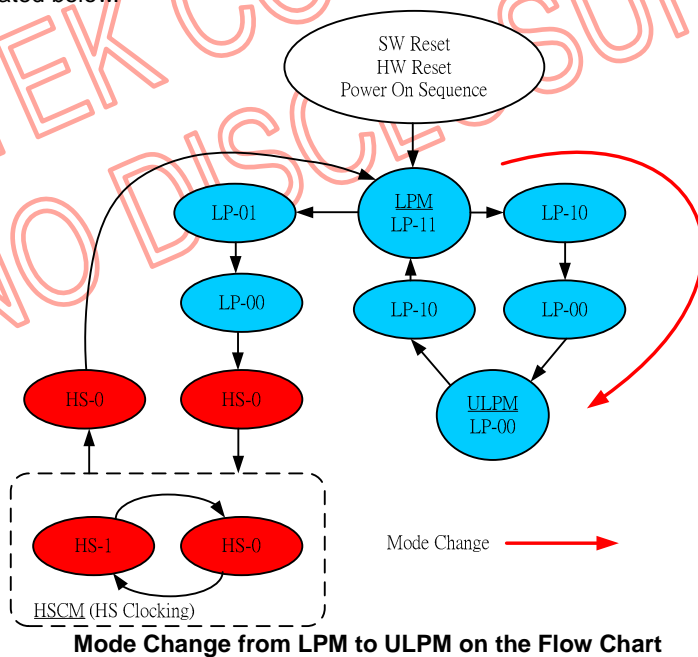
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5.7.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.

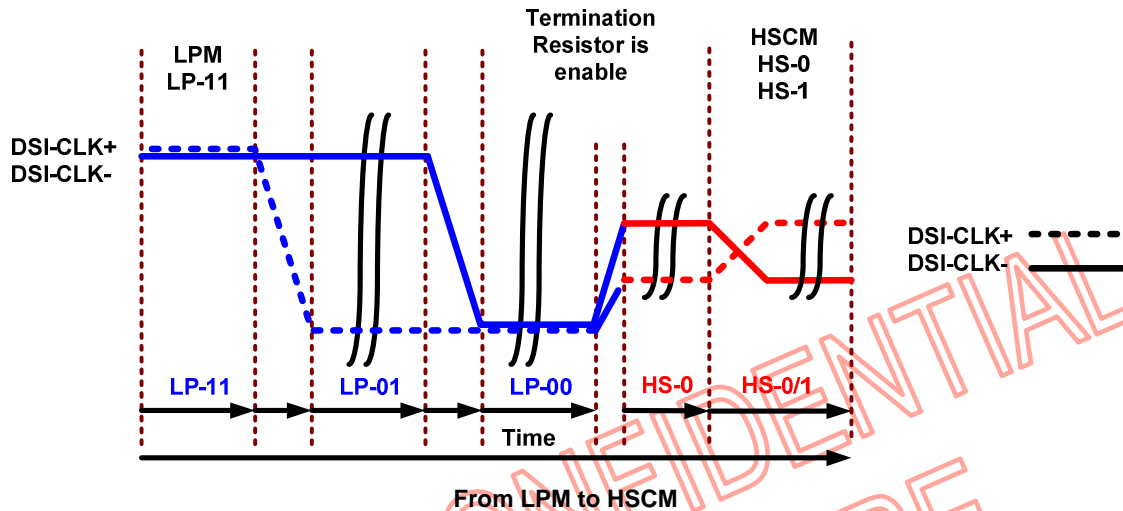


The mode change is also illustrated below.

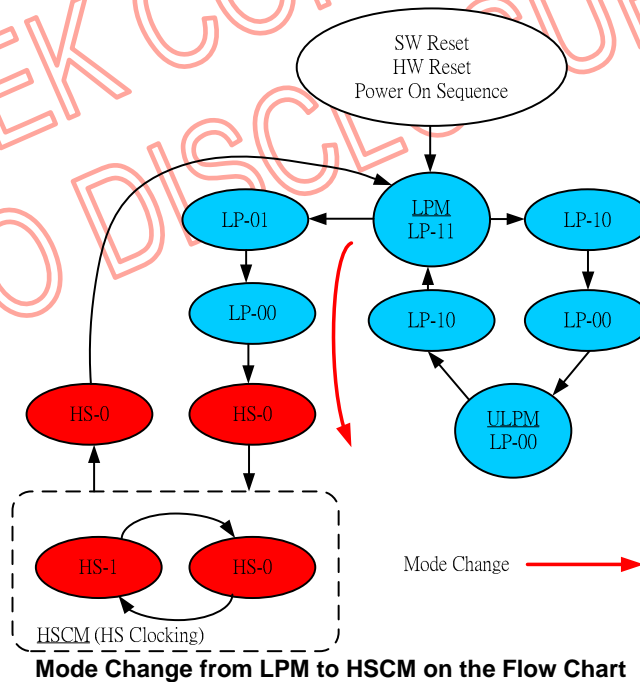


5.7.2.2.3 High Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



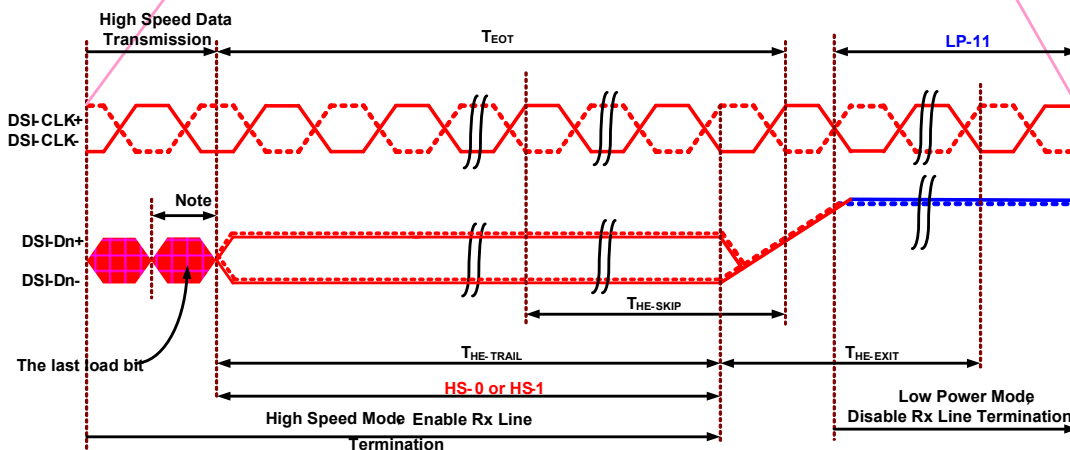
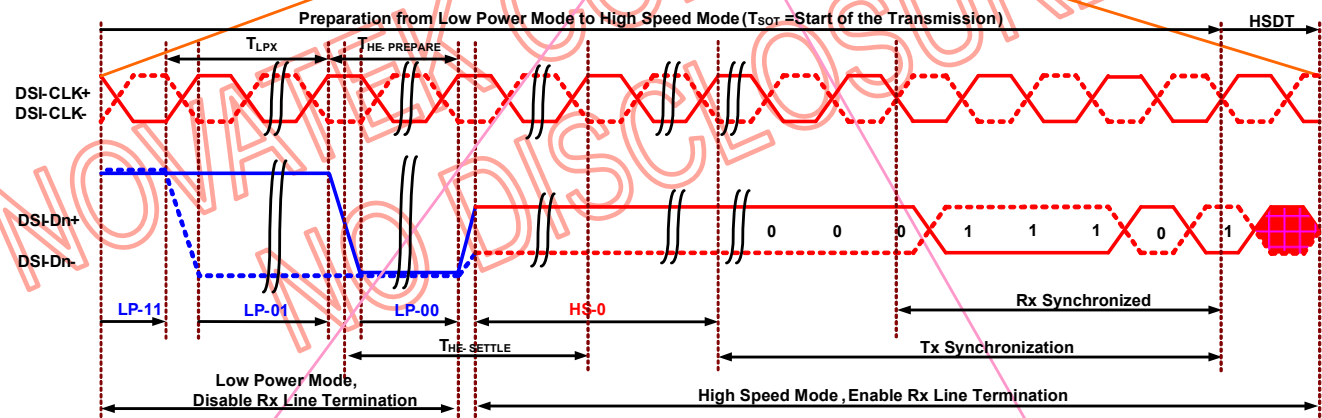
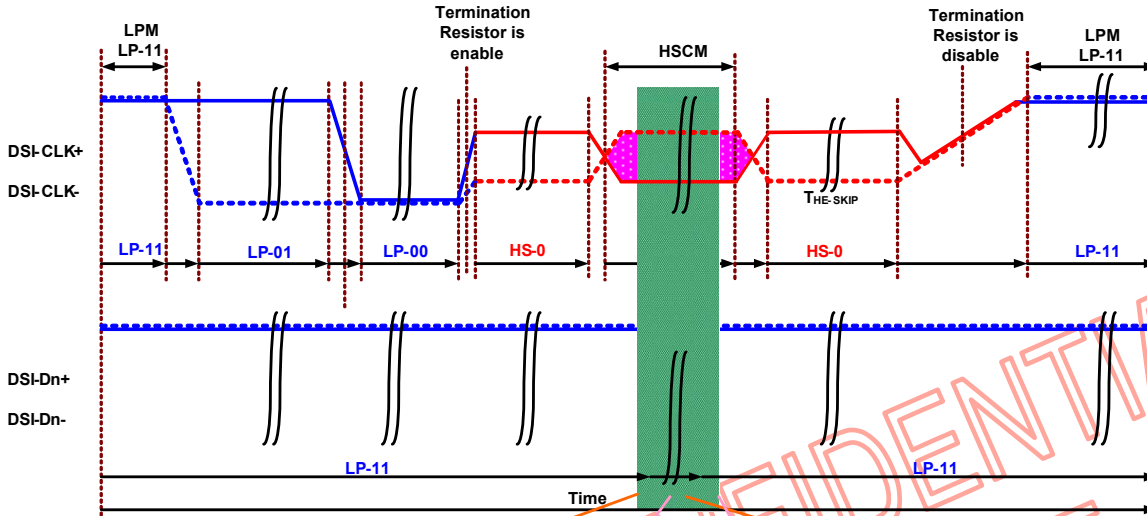
The mode change is also illustrated below.



The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of :

- o Even number of transitions
- o Start state is HS-0
- o End state is HS-0



Note :
 If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
 If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-Dn+ -----
 DSI-CLK-, DSI-Dn- _____

High Speed Clock Burst

Hig

5.7.2.2.3 DSI-DATA Lanes
5.7.2.2.3.1 General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode(only DSI_D0+/- data lane is used)
- High-Speed Data Transmission(all data lanes are used)
- Bus Turnaround Request(only DSI_D0+/- data lane is used)

These modes and their entering codes are defined on the following table.

Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z, Note

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5.7.2.2.3.2 Escape Mode

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

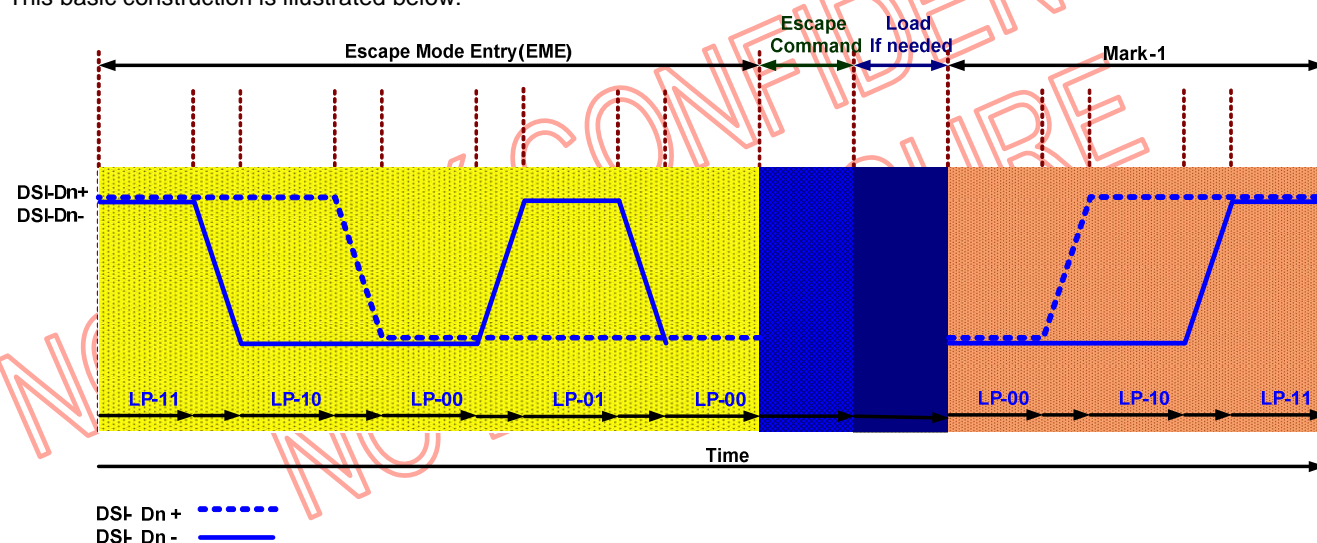
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-Dn+ = 1, DSI-Dn- = 0) e.g. when DSI-Dn- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-Dn+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

Escape Commands

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 bin
Ultra-Low Power Mode	Mode	0001 1110 bin
Underfined-1, Note	Mode	1001 1111 bin
Underfined-2, Note	Mode	1101 1110 bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin
Unknow-5, Note	Trigger	1010 0000 bin

Note: This Escape command support has not been implemented on the display module.

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Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):

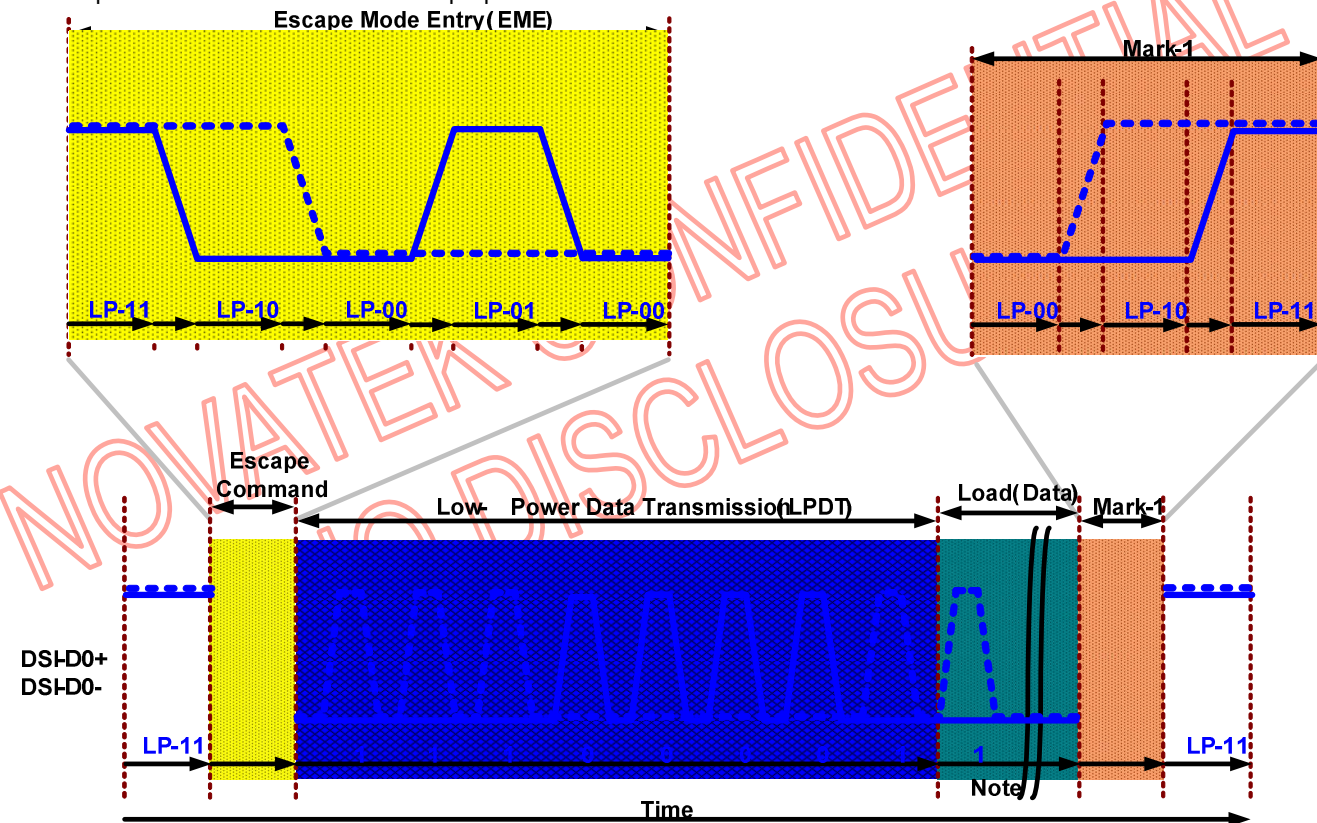
One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

- Mark-1: LP-00 =>LP-10 =>LP-11

- End: LP-11

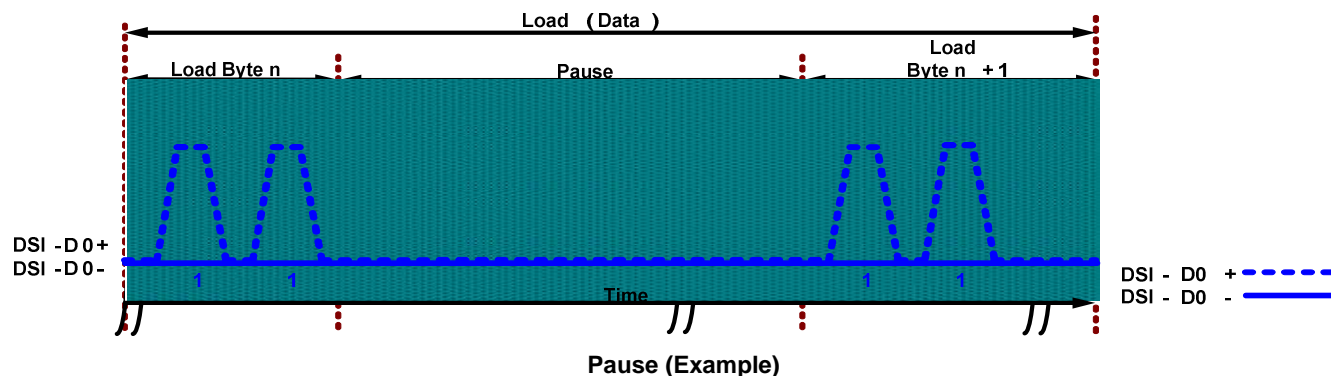
This sequence is illustrated for reference purposes below:



Note : Load(Data) is presenting that the first bit is logical '1' in this example

DSI- D0 + : - - - - -
DSI- D0 - : _____

Low-Power Data Transmission (LPDT)



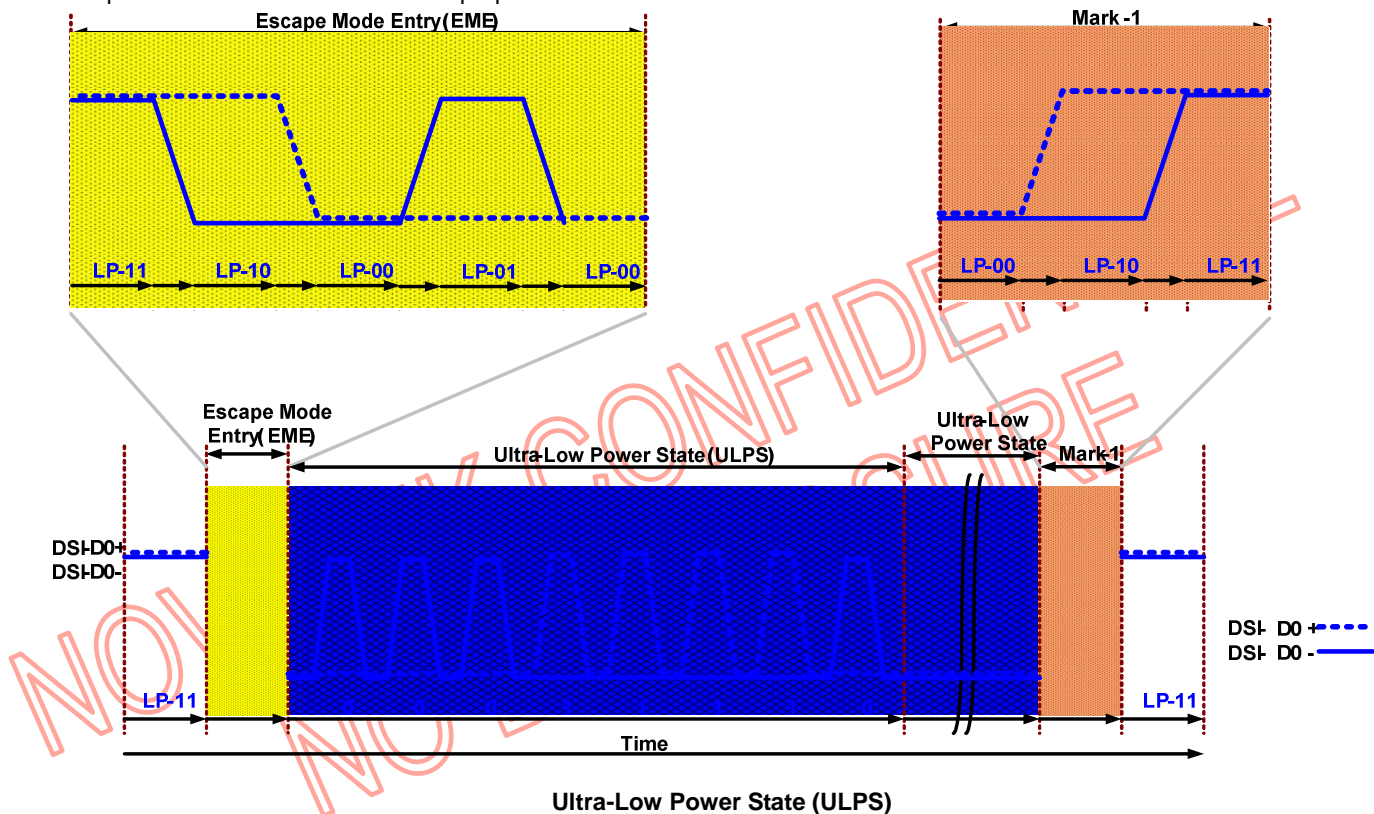
Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



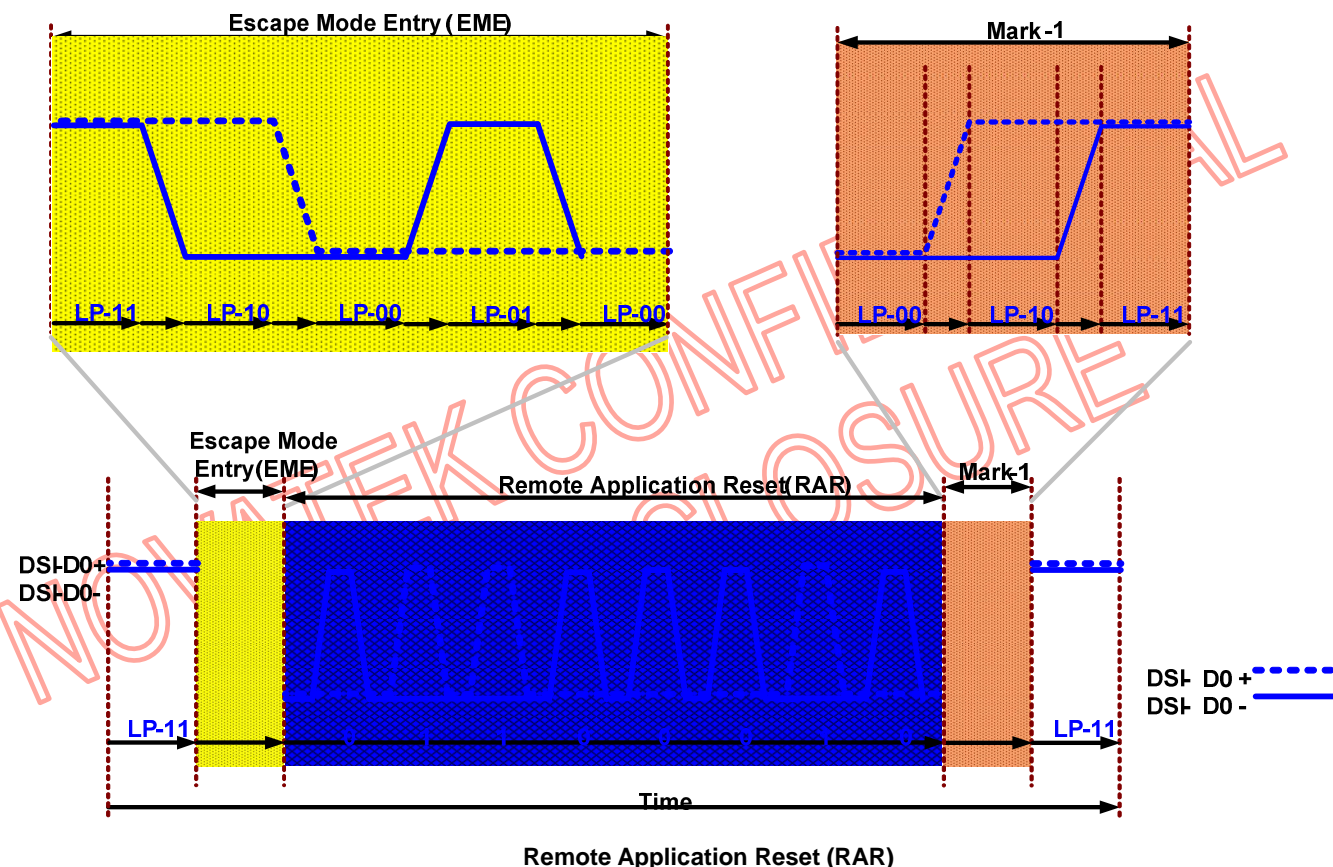
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



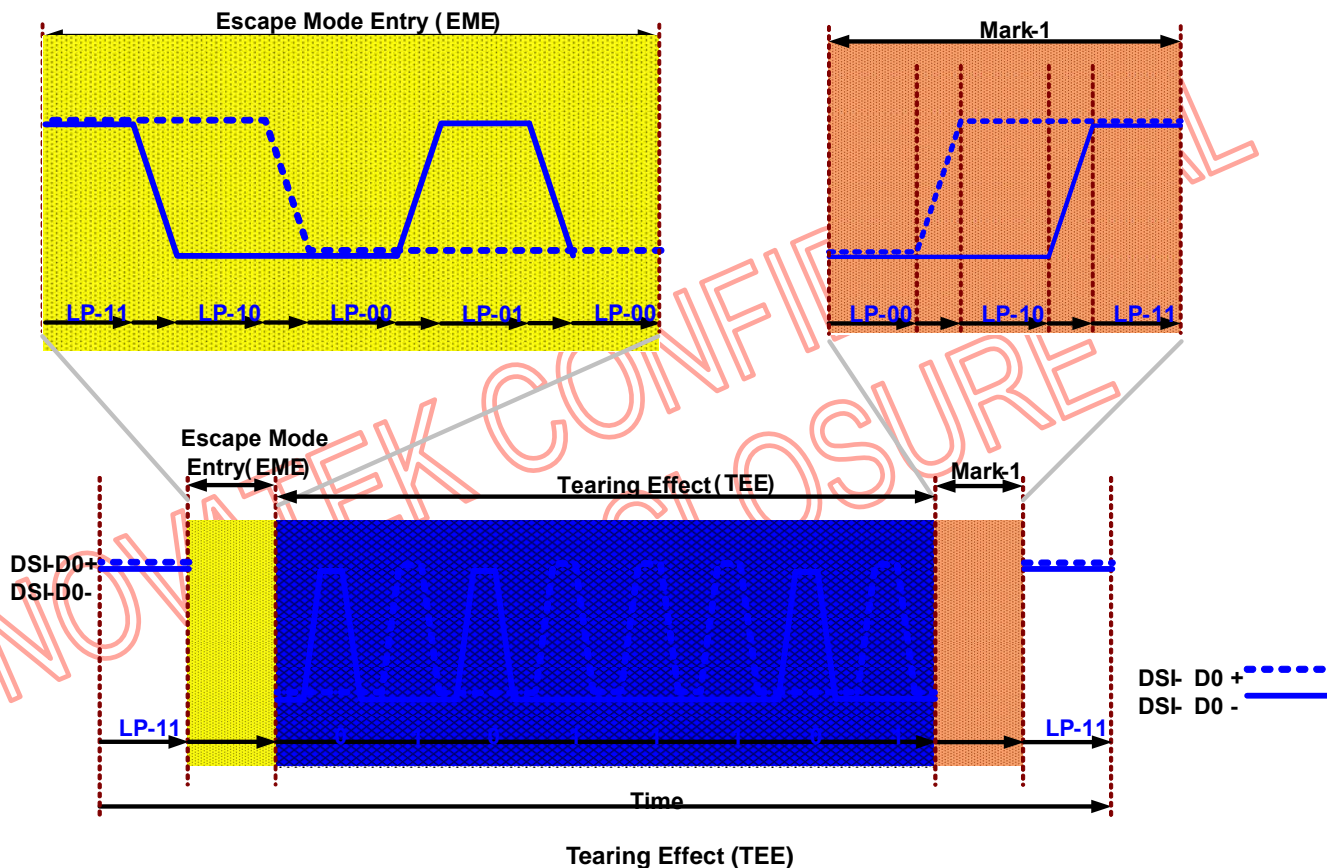
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



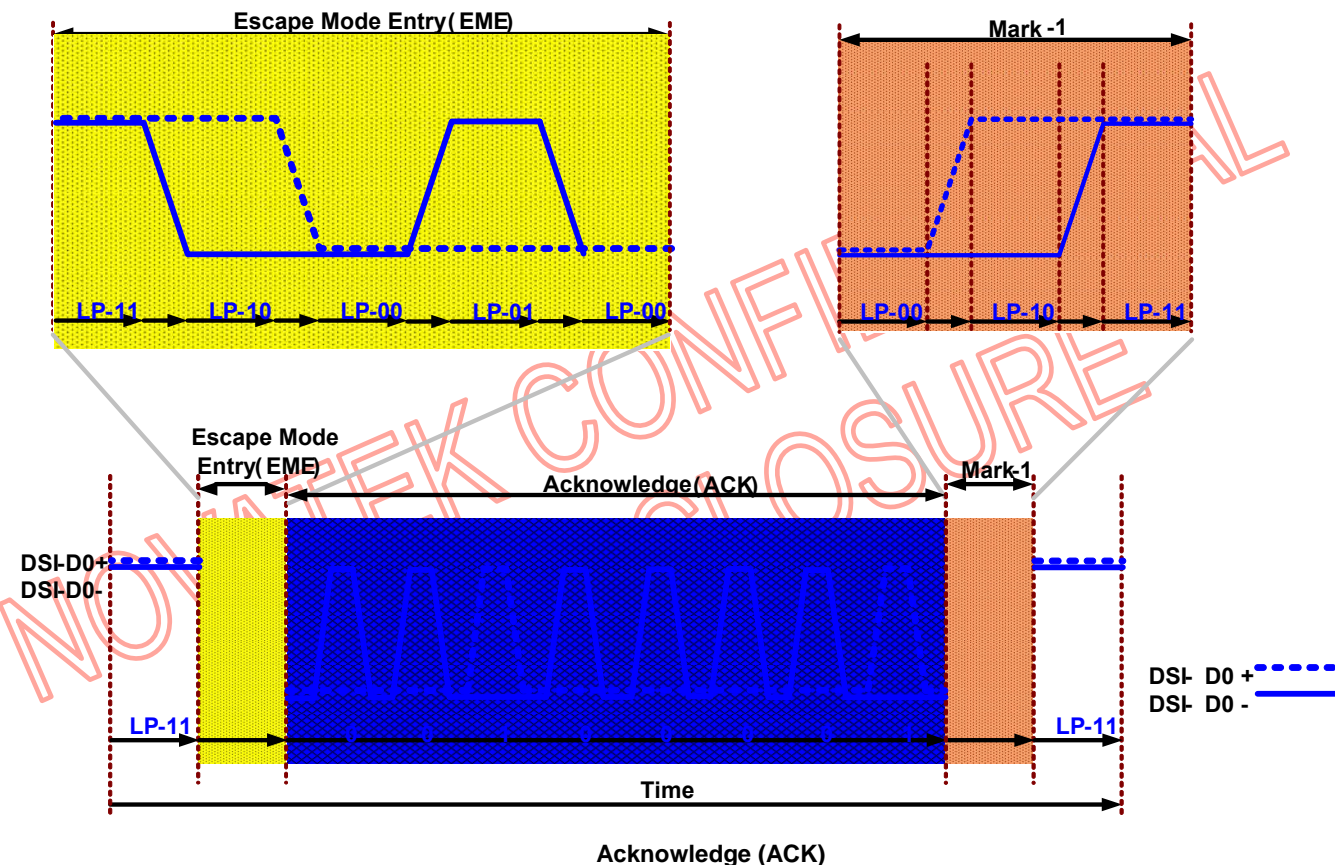
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



5.7.2.2.3.3 High Speed Data Transmission

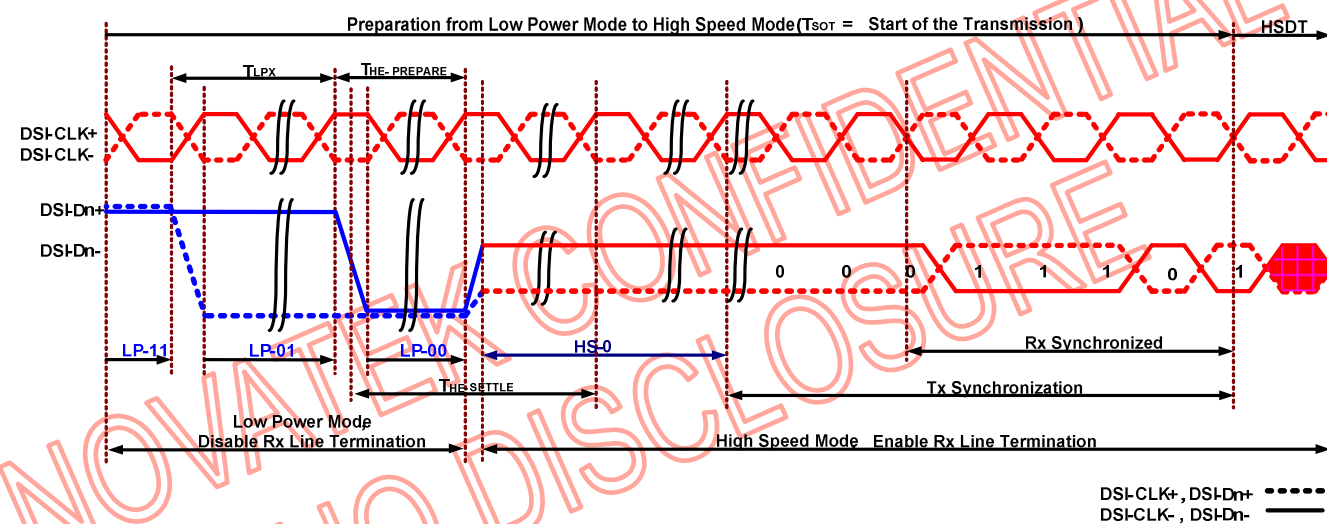
Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Ent

ering High-Speed Data Transmission (T_{SOT} of HSDT)

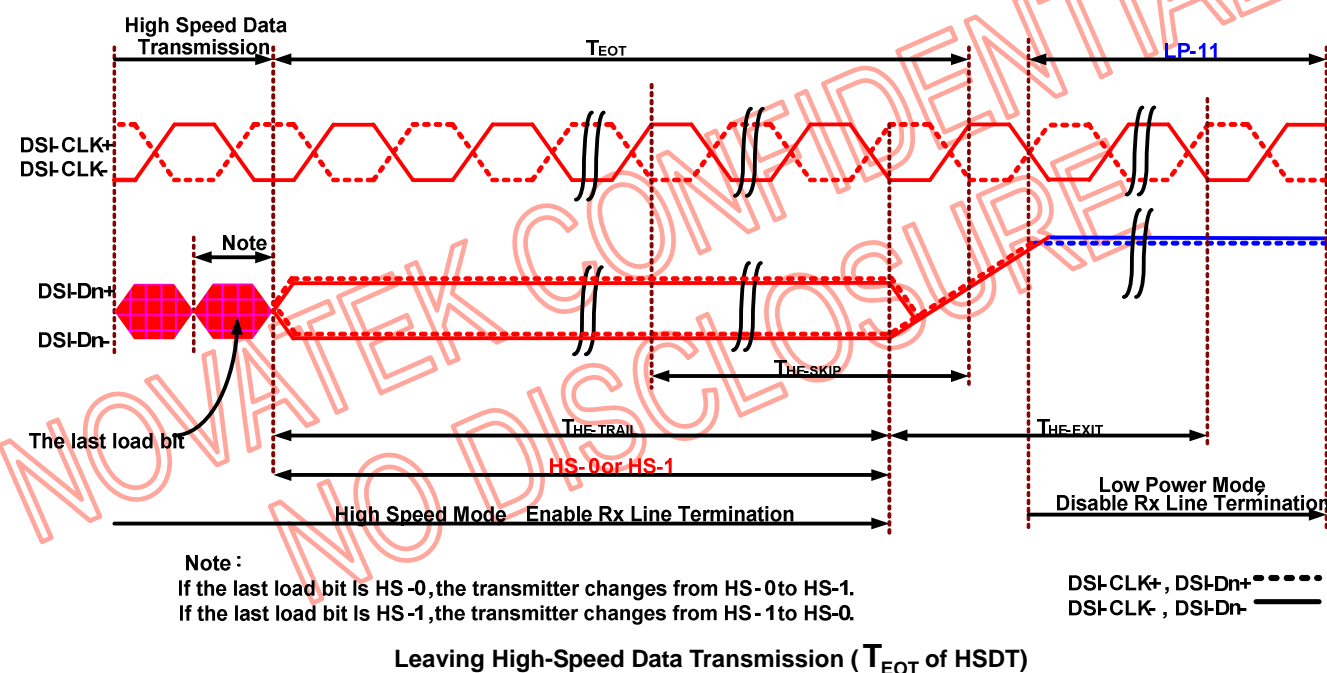
Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

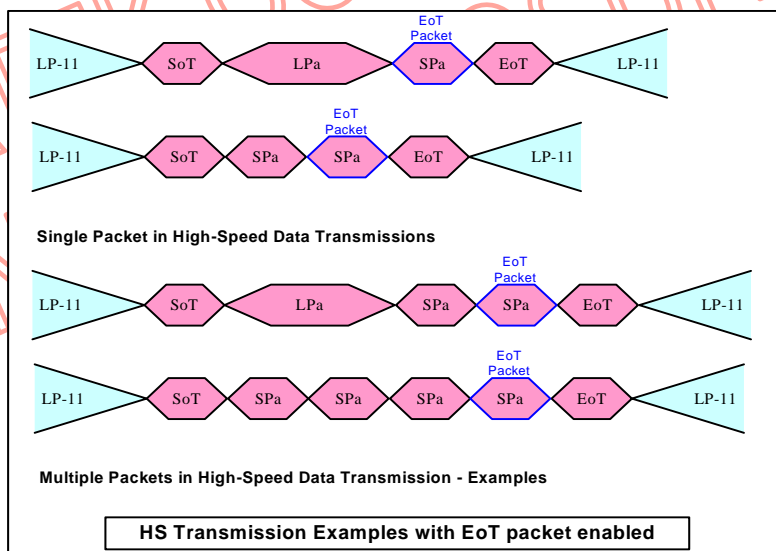
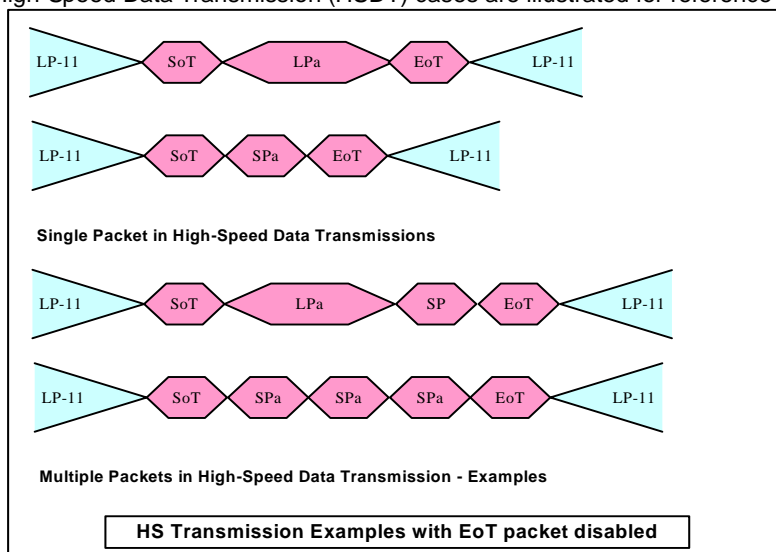
This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "Short Packet (SPa) and Long Packet (LPa) Structures".

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Abbreviations

Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

5.7.2.3 Packet Level Communication

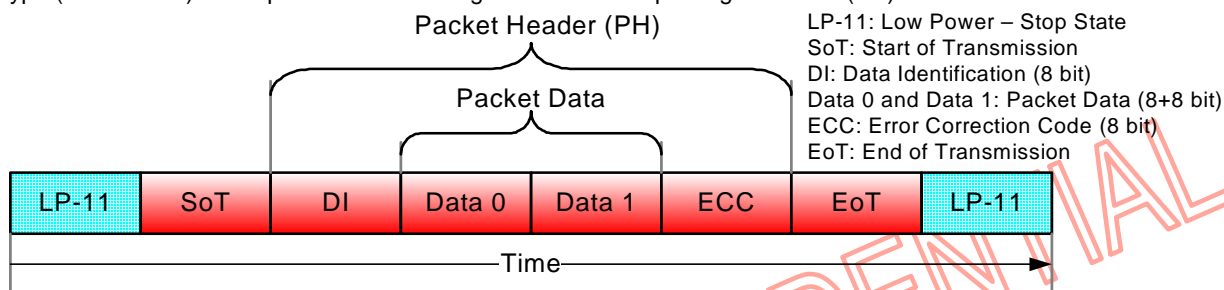
5.7.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

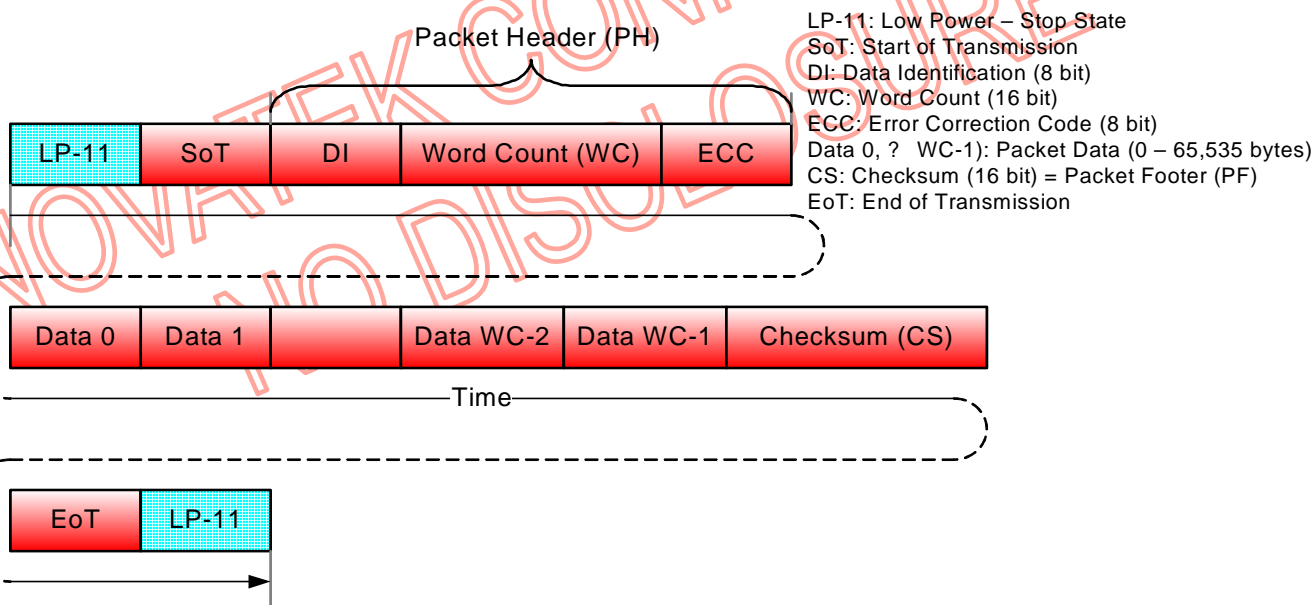
The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Short Packet (SPa) Structure



Long Packet (LPa) Structure

Note:

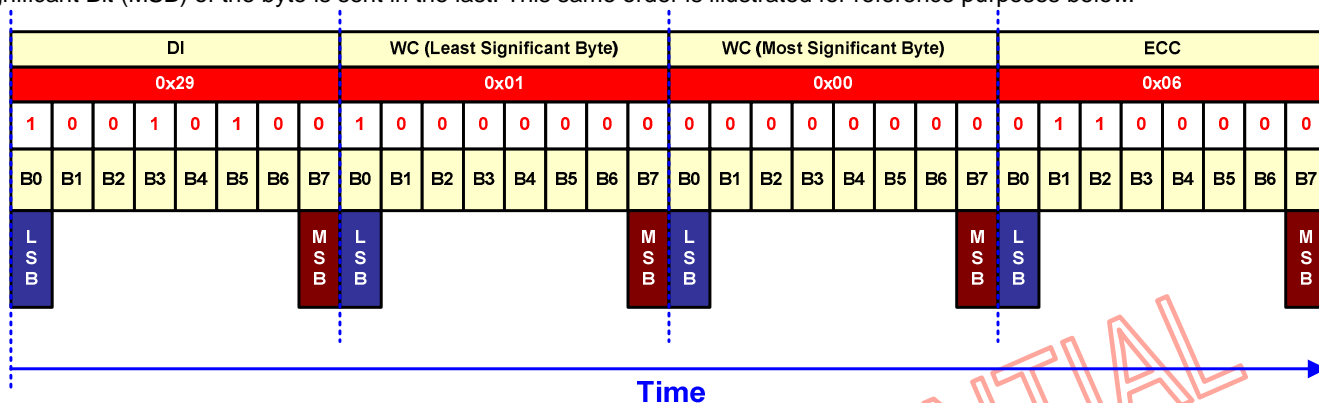
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- * LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- * LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- * LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.7.2.3.1.1 Bit Order of Byte on Packets

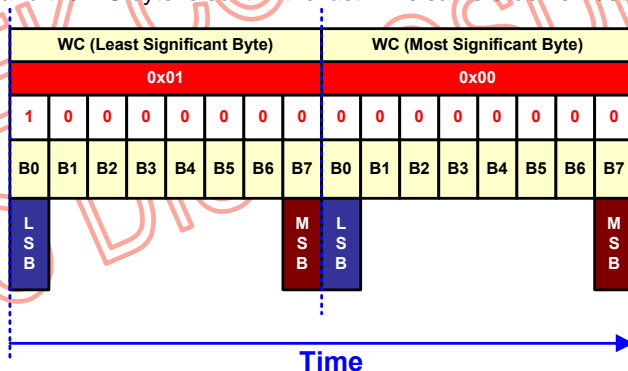
The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last. This same order is illustrated for reference purposes below.



Bit Order of the Byte on Packet

5.7.2.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last. This same order is illustrated for reference purposes below.



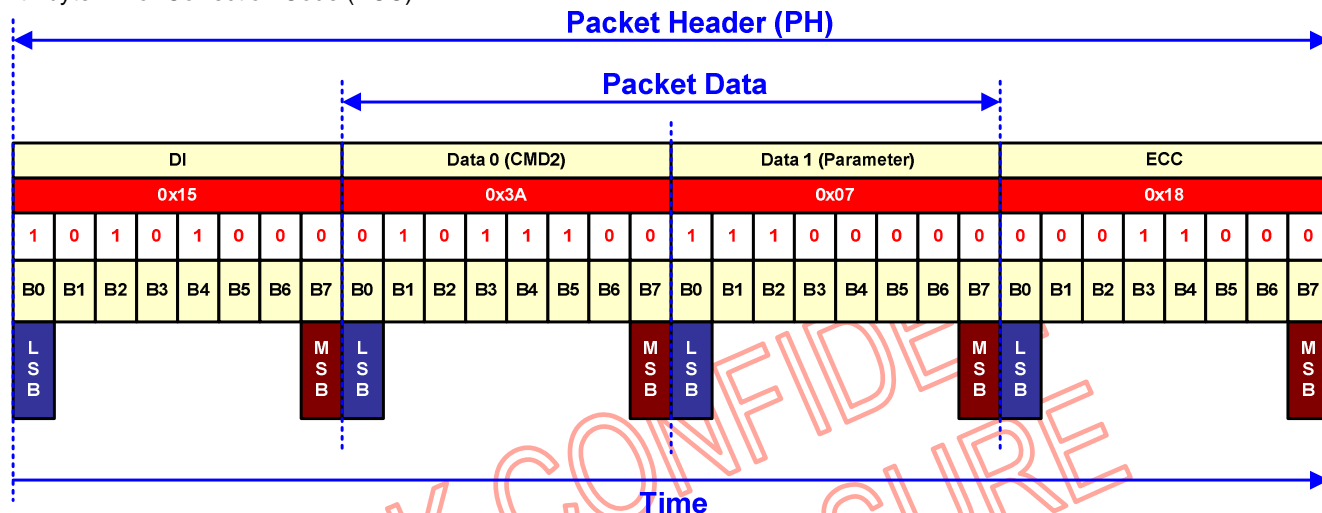
Byte Order of the Multiple Byte on Packet

5.7.2.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

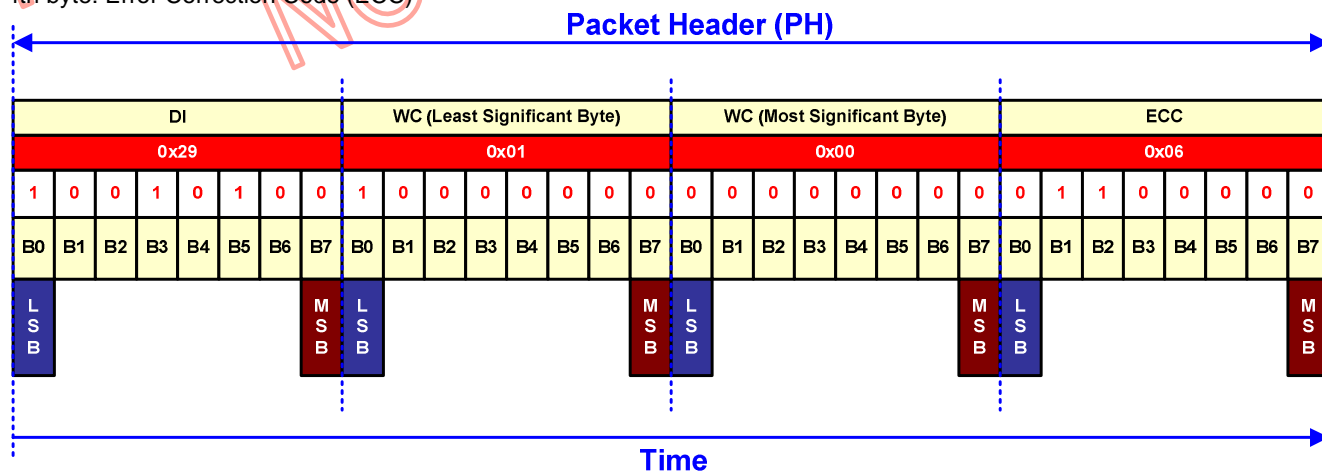
- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

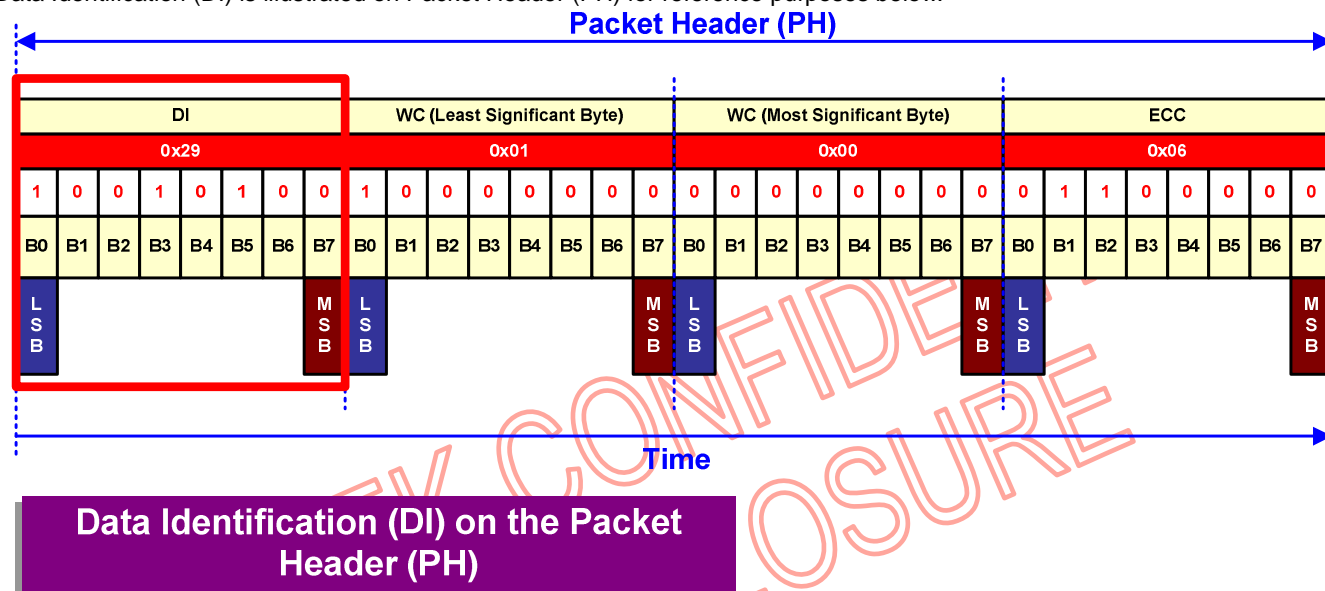
- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

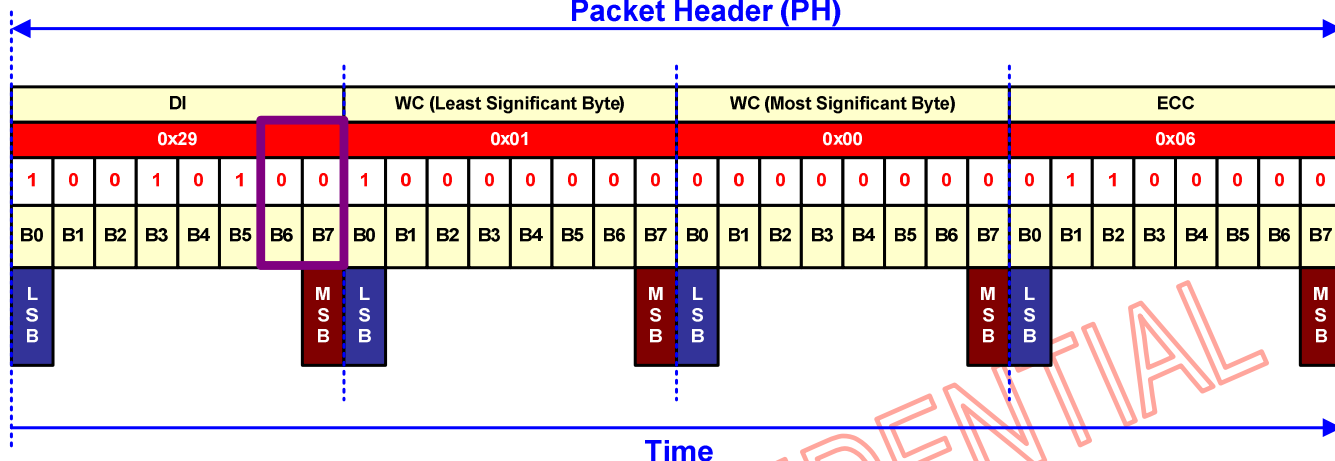
Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.



Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU. Bit of the Virtual Channel (VC) are illustrated for reference purposes below.

Packet Header (PH)

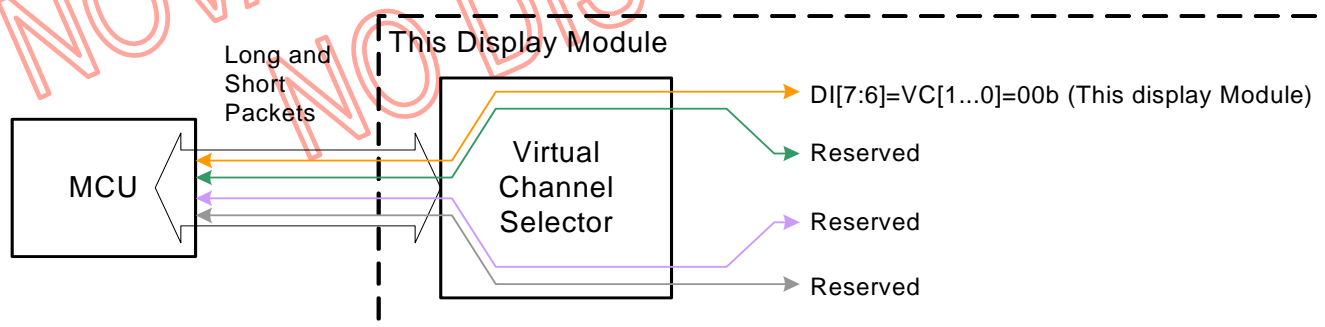


Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

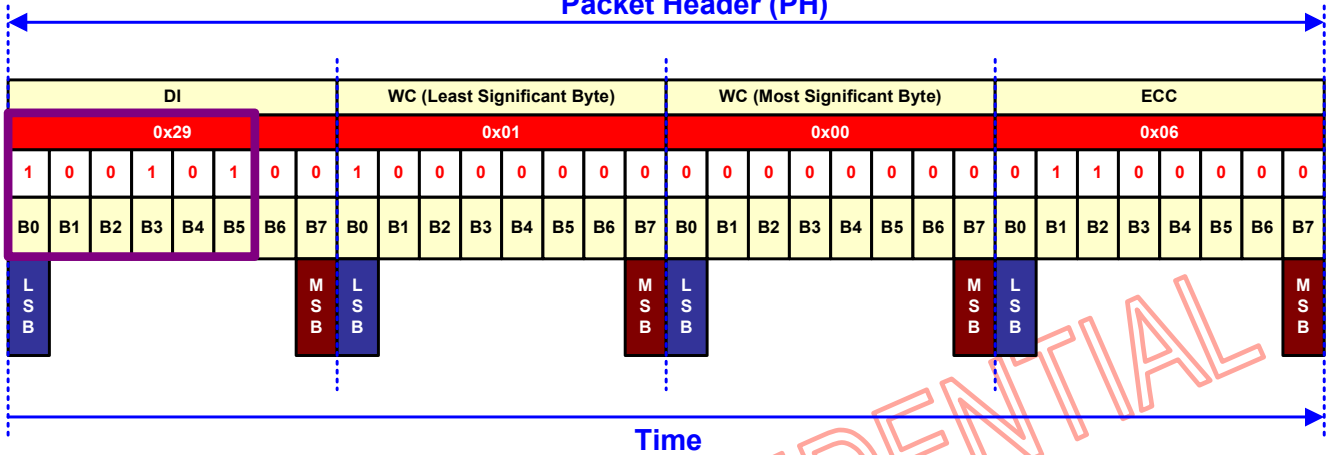


Virtual Channel (VC) Configuration

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet. Bit of the Data Type (DT) are illustrated for reference purposes below.

Packet Header (PH)



Data Type (DT) on the Packet Header (PH)

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This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type, hex	Data Type, binary	Description	Packet Size	Note
01h	00 0001	Sync Event, V Sync Start	Short	
11h	01 0001	Sync Event, V Sync End	Short	
21h	10 0001	Sync Event, H Sync Start	Short	
31h	11 0001	Sync Event, H Sync End	Short	
08h	00 1000	End of Transmission (EoT) packet	Short	
02h	00 0010	Color mode (CM) Off Command	Short	
12h	01 0010	Color mode (CM) On Command	Short	
22h	10 0010	Shut Down Peripheral Command	Short	
32h	11 0010	Turn On Peripheral Command	Short	
03h	00 0011	Generic Short Write, no parameter	Short	
13h	01 0011	Generic Short Write, 1 parameter	Short	1,2
23h	10 0011	Generic Short Write, 2 parameter	Short	1,3
29h	10 1001	Generic Long Write	Long	1
04h	00 0100	Generic Read, no parameter	Short	
14h	01 0100	Generic Read, 1 parameter	Short	1,2
24h	10 0100	Generic Read, 2 parameter	Short	1,3
05h	00 0101	DCS WRITE, no parameters	Short	
15h	01 0101	DCS WRITE, 1 parameter	Short	
06h	00 0110	DCS READ, no parameters	Short	
37h	11 0111	Set Maximum Return Packet Size	Short	
09h	00 1001	Null Packet, no data	Long	
19h	01 1001	Blanking Packet, no data	Long	
39h	11 1001	DCS Long Write/Write LUT Command Packet	Long	
0Eh	00 1110	Packed Pixel Stream, 16-bits RGB, 5-6-5 Format	Long	
1Eh	01 1110	Packed Pixel Stream, 18-bits RGB, 6-6-6 Format	Long	
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bits RGB, 6-6-6 Format	Long	
x0h and xFh unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved		

Note: 1. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).

2. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.

3. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.

4. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU									
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Short/Lng Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
08h	0	0	1	0	0	0	End of Transmission (EoT) packet	Short	EoT
1Ch	0	1	1	1	0	0	DCS Read Long Response	Long	DCSRR-L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1-S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2-S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response, 1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response, 2 byte returned	Short	GENRR2-S

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".

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Availability of MIPI Data Type for Instruction Code (User Command Set)

MIPI Data Type	03h (GENWN-S)	13h (GENW1-S)	23h (GENW2-S)	29h (GENW-L)	04h (GENRN-S)	14h (GENR1-S)	24h (GENR2-S)	05h (DCSWN-S)	15h (DCSW1-S)	39h (DCSW-L)	06h (DCSRN-S)
Instruction Code	Availability of MIPI Data Type										
00h (NOP)								Yes	Yes	Yes	
01h (SOFT_RESET)								Yes	Yes	Yes	
05h (RDNUMED)											Yes
0Ah (GET_POWER_MODE)											Yes
0Bh (GET_ADDRESS_MODE)											Yes
0Ch (GET_PIXEL_FORMAT)											Yes
0Dh (GET_DISPLAY_MODE)											Yes
0Eh (GET_SIGNAL_MODE)											Yes
0Fh (RDDSDR)											Yes
10h (ENTER_SLEEP_MODE)								Yes	Yes	Yes	
11h (EXIT_SLEEP_MODE)								Yes	Yes	Yes	
12h (ENTER_PARTIAL_MODE)								Yes	Yes	Yes	
13h (ENTER_NORMAL_MODE)								Yes	Yes	Yes	
20h (EXIT_INVERT_MODE)								Yes	Yes	Yes	
21h (ENTER_INVERT_MODE)								Yes	Yes	Yes	
22h (ALLPOFF)								Yes	Yes	Yes	
23h (ALLPON)								Yes	Yes	Yes	
26h (GMASET)									Yes	Yes	
28h (SET_DISPLAY_OFF)								Yes	Yes	Yes	
29h (SET_DISPLAY_ON)								Yes	Yes	Yes	
2Ah (SET_HORIZONTAL_ADDRESS)										Yes	
2Bh (SET_VERTICAL_ADDRESS)										Yes	
2Ch (WRITE_MEMORY_START)									Yes	Yes	
2Dh (SET_RAM_ADDRESS)										Yes	
2Eh (READ_MEMORY_START)											Yes
30h (SET_PARTIAL_AREA)										Yes	Yes
34h (SET_TEAR_OFF)								Yes	Yes	Yes	
35h (SET_TEAR_ON)									Yes	Yes	Yes
36h (SET_ADDRESS_MODE)									Yes	Yes	Yes
38h (EXIT_IDLE_MODE)								Yes	Yes	Yes	
39h (ENTER_IDLE_MODE)								Yes	Yes	Yes	
3Ah (SET_PIXEL_FORMAT)									Yes	Yes	Yes
3Bh (RGBCTRL)										Yes	Yes
3Ch (RAMWRC)									Yes	Yes	
3Eh (RAMRDC)											Yes
44h (SET_TEAR_SCANLINE)										Yes	Yes
45h (RDACL)											Yes
4Fh (ENTER_DSTB_MODE)									Yes	Yes	
51h (WRIDSBV)									Yes	Yes	Yes
52h (RDDISBV)											Yes
53h (WRCTRLD)									Yes	Yes	

MIPI Data Type	03h (GENWN-S)	13h (GENW1-S)	23h (GENW2-S)	29h (GENW-L)	04h (GENRN-S)	14h (GENR1-S)	24h (GENR2-S)	05h (DCSWN-S)	15h (DCSW1-S)	39h (DCSW-L)	06h (DCSRN-S)
Instruction Code	Availability of MIPI Data Type										
54h (RDCTRLD)											Yes
55h (WRCABC)									Yes	Yes	
56h (RDCABC)											Yes
5Eh (WRCABCMB)									Yes	Yes	
5Fh (RDCABCMB)											Yes
60h (WRPFK)										Yes	Yes
61h (WRKEYBV)									Yes	Yes	Yes
62h (RDKEYBV)											Yes
63h (WRCTRLK)									Yes	Yes	
64h (RDCTRLK)											Yes
65h (WRLSCC)										Yes	
66h (RDLSCCM)											Yes
67h (RDLSCCL)											Yes
70h (RDBWLB)											Yes
71h (RDBKX)											Yes
72h (RDBKY)											Yes
73h (RDWX)											Yes
74h (RDWY)											Yes
75h (RDRGLB)											Yes
76h (RDRX)											Yes
77h (RDRY)											Yes
78h (RDGX)											Yes
79h (RDGY)											Yes
7Ah (RDBALB)											Yes
7Bh (RDBX)											Yes
7Ch (RDBY)											Yes
7Dh (RDAX)											Yes
7Eh (RDAY)											Yes
A1h (RDDDBS)											Yes
A8h (RDDDBC)											Yes
AAh (RDFCS)											Yes
AEh (SET EDGE TIMING CTRL)									Yes	Yes	Yes
AFh (RDCCS)											Yes
DAh (RDID1)											Yes
DBh (RDID2)											Yes
DCh (RDID3)											Yes
E1h(IDLEMODE_BL_CTRL)									Yes	Yes	
E2h(IDLEMODE_BL_CTRL)											Yes
E3h(WRALS)									Yes	Yes	
E4h(RDALS)											Yes
EDh (CMD2UNLOCK)									Yes	Yes	
FFh(Page status)											Yes

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

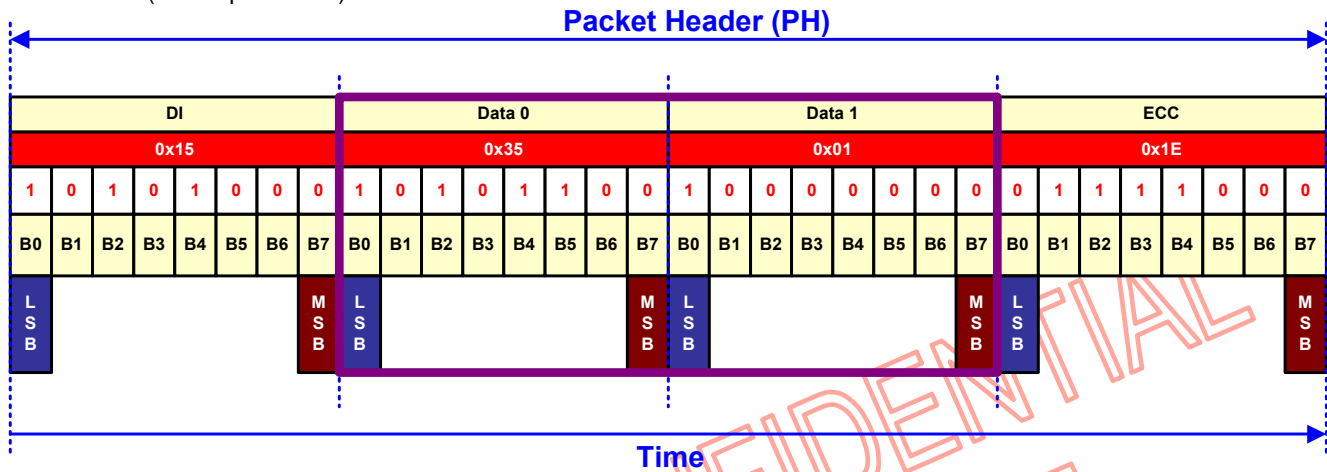
Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bit of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

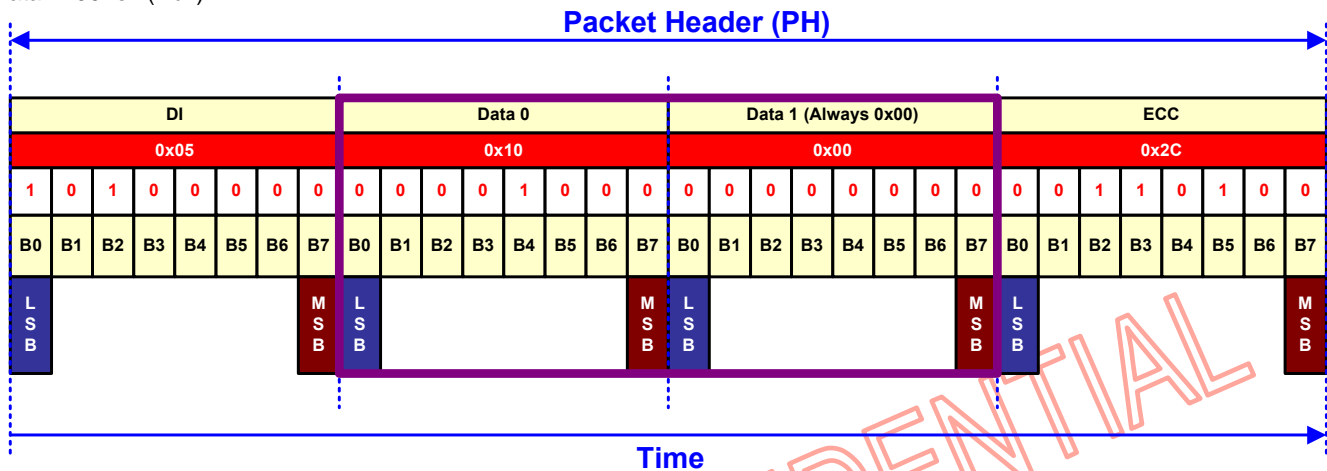


Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

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Packet Data (PD) Information:

- Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Byte Information

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Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

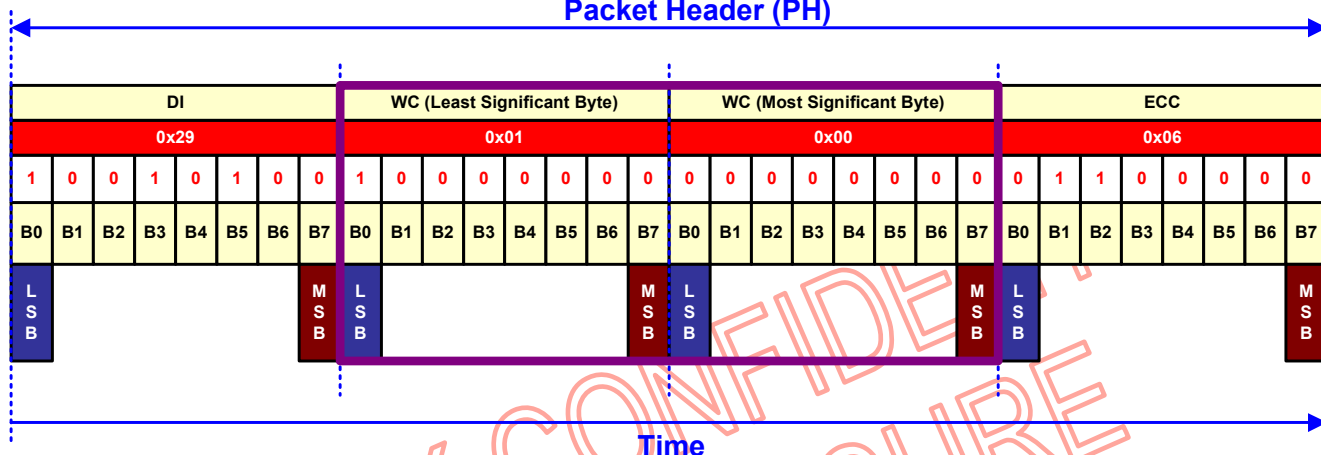
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

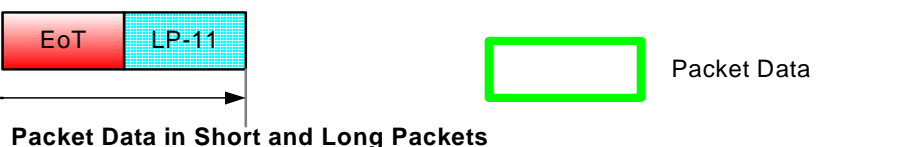
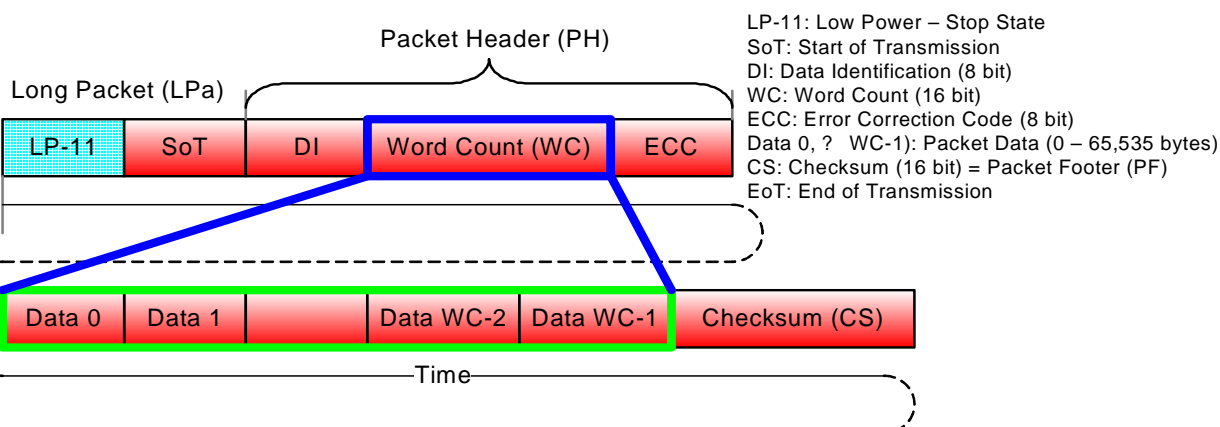
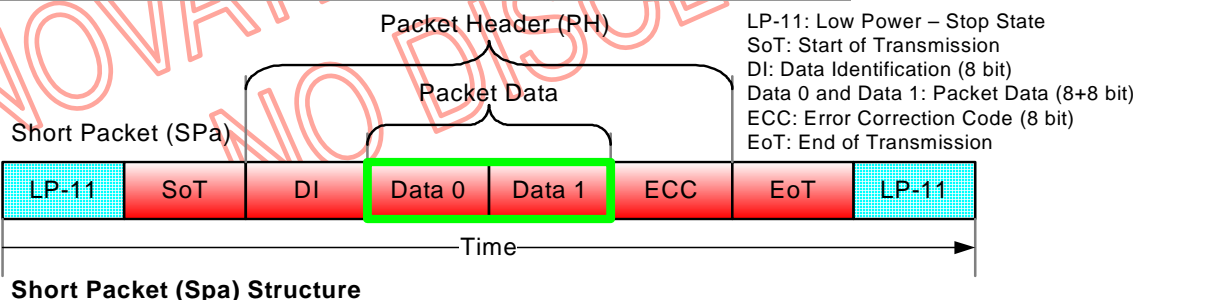
These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

Packet Header (PH)



Word Count (WC) on the Long Packet (LPa)

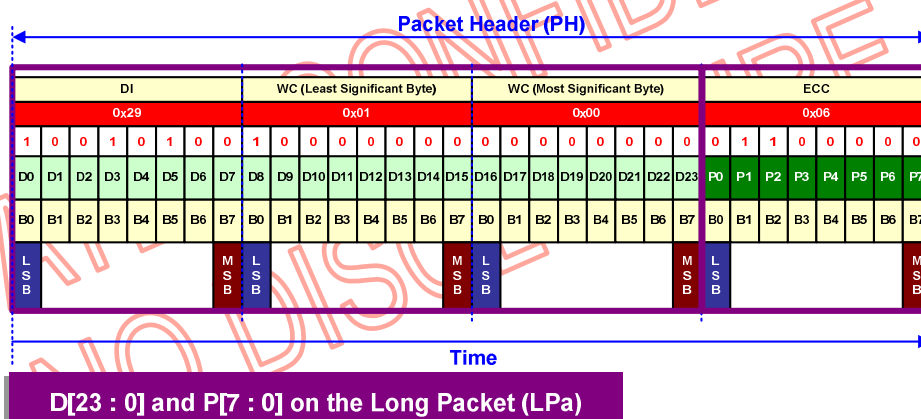
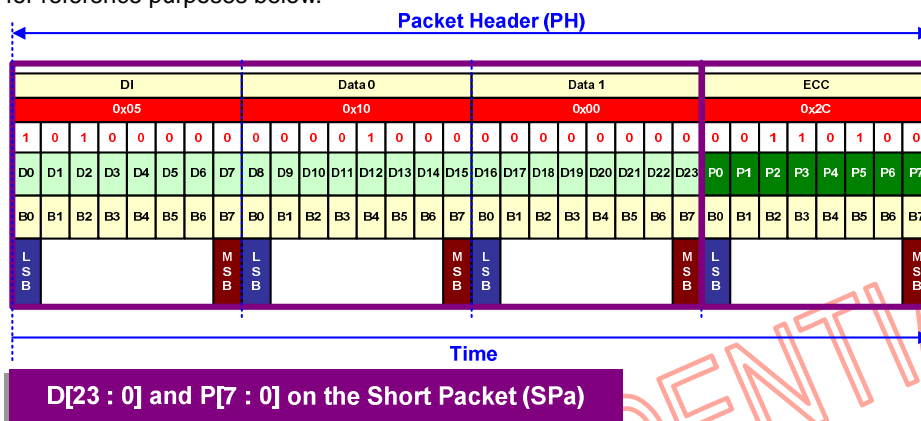


Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23...0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23...0])

D[23...0] is illustrated for reference purposes below.

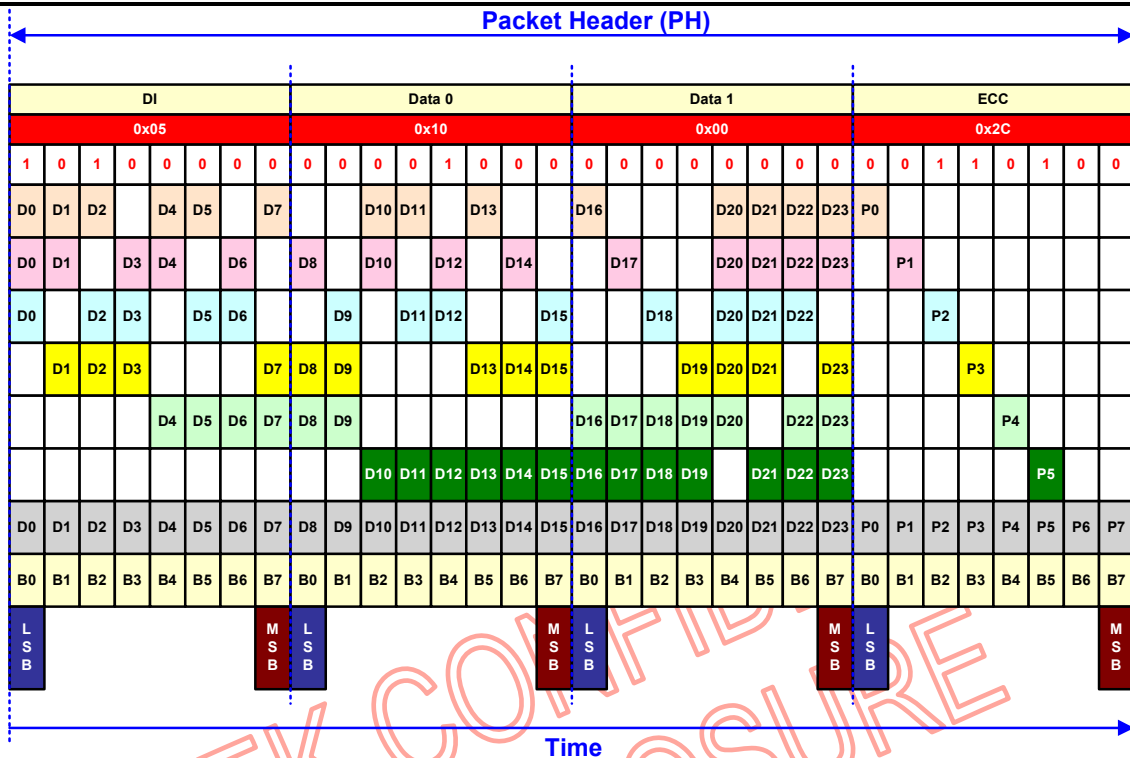


Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

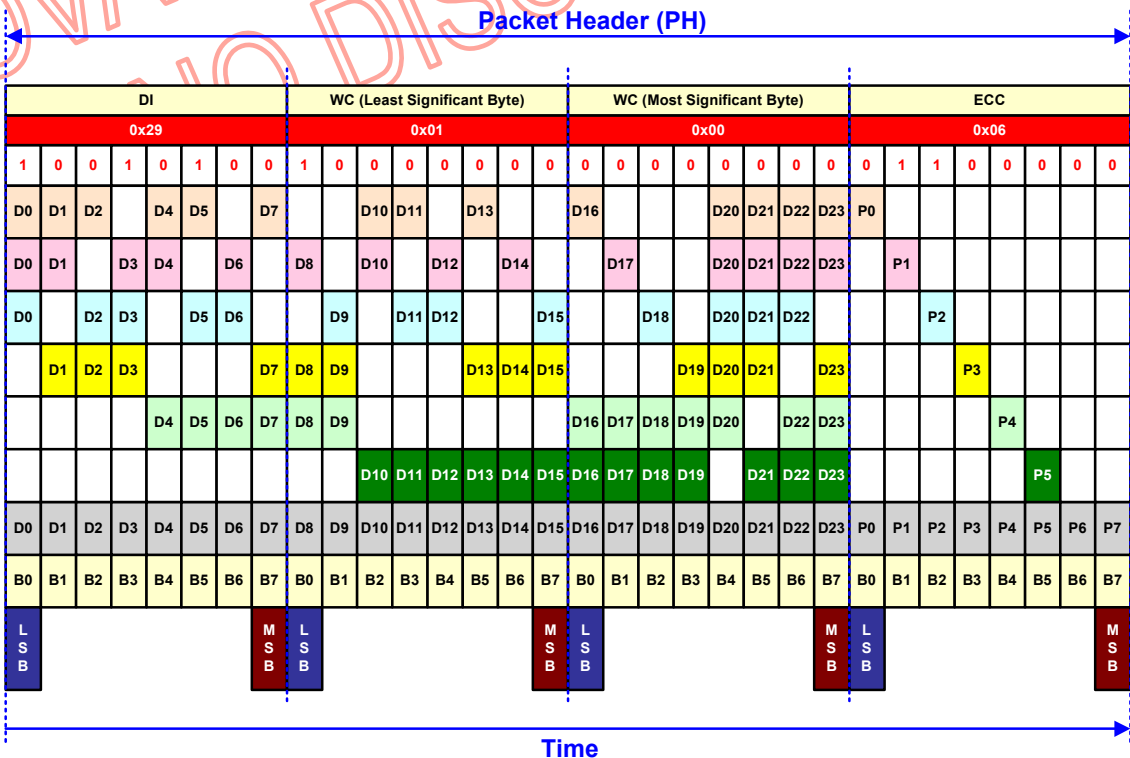
Bit (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bits value ([D63...0]), but this implementation is based on 24 bits value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).



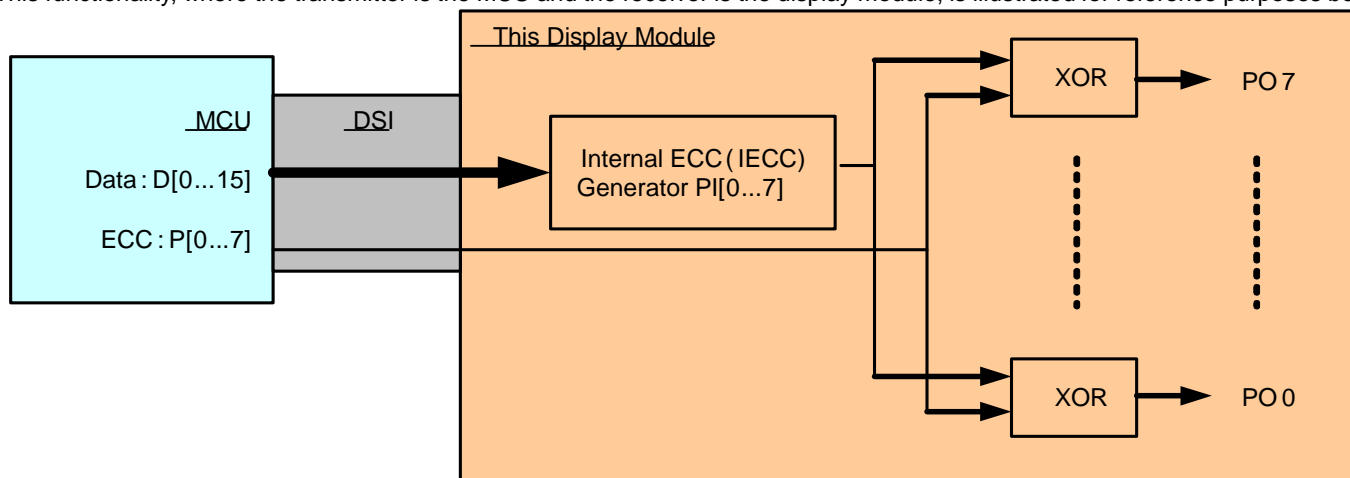
XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7...0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[15...0]) and ECC (P[7...0]) are received correctly, if a value of the PO[7...0] is 00h. The sent data bits (D[15...0]) and ECC (P[7...0]) are not received correctly, if a value of the PO[7...0] is not 00h.

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 0 0 0 0 0 0	03h
XOR(ECC,IECC) =>PO[7...0]	0 0 0 0 0 0 0 0	=00h => No Error
	L S B	M S B

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 1 1 0 0 0 0	0Fh
XOR(ECC,IECC) =>PO[7...0]	0 0 1 1 0 0 0 0	=0Ch => Error
	L S B	M S B

Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[15...0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to values on the following table.
One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7...0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7...0] = 0Ch.

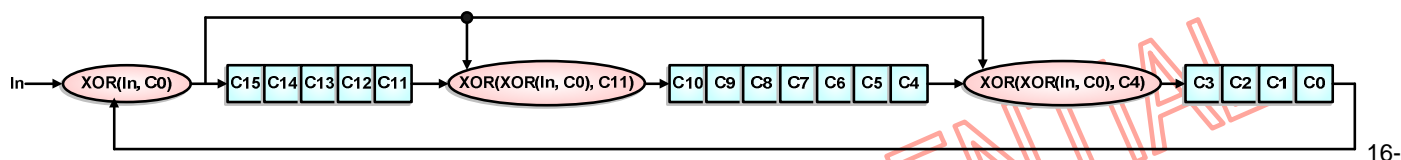
5.7.2.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet (LPa)".

5.7.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

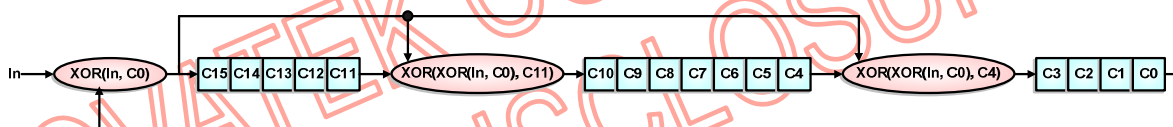
The checksum is using a 16-bits Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.



16-bit Cyclic Redundancy Check (CRC) Calculation

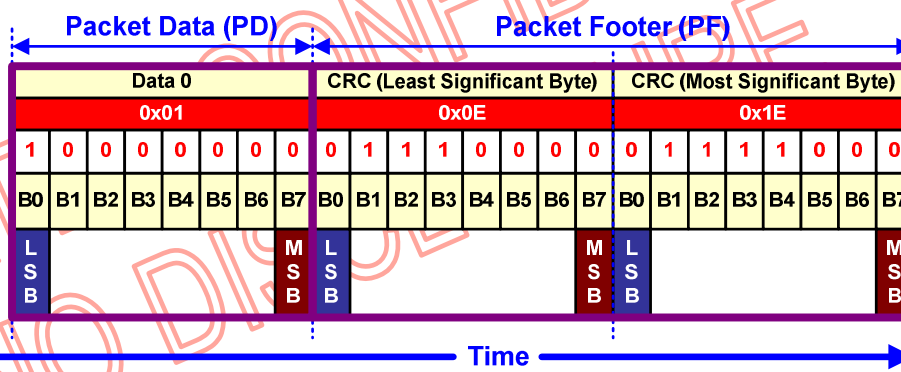
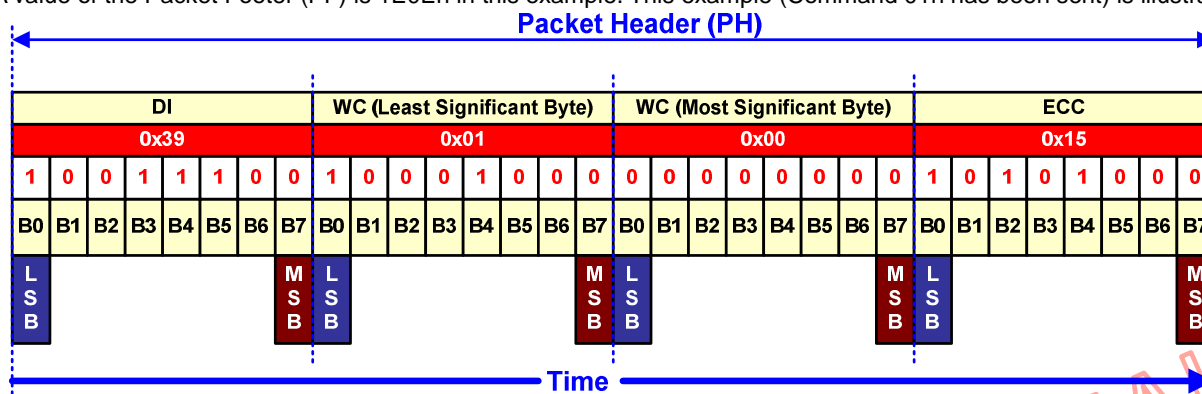
The 16-bits Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bits Cyclic Redundancy Check (CRC).

An example of the 16-bits Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In, C0)	C15	C14	C13	C12	C11	XOR(XOR(In, C0), C11(Step - 1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In, C0), C4(Step - 1))	C3	C2	C1	C0	C0	
0	x	x	1	1	1	1	1	x	1	1	1	1	1	1	1	x	1	1	1	1	x	
1	1 (LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1	
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	
5	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	
8	0 (MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	
1 Byte	CRC Result		0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0		
			MSB																			LSB

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

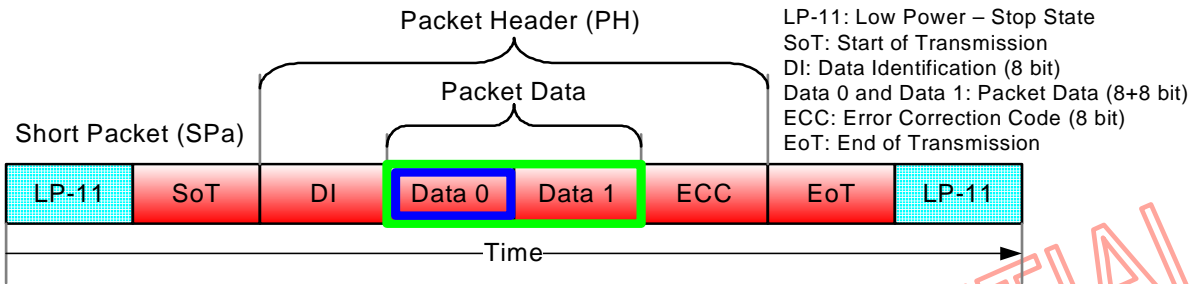
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.7.2.3.2 Packer Transmission

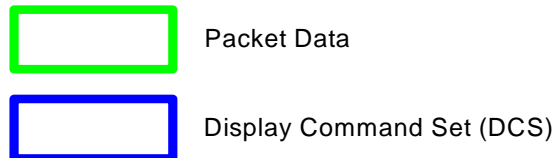
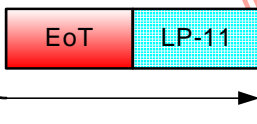
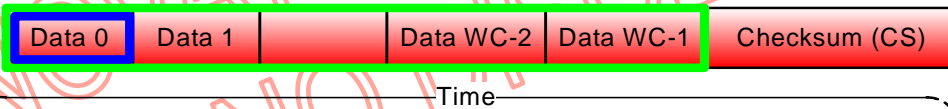
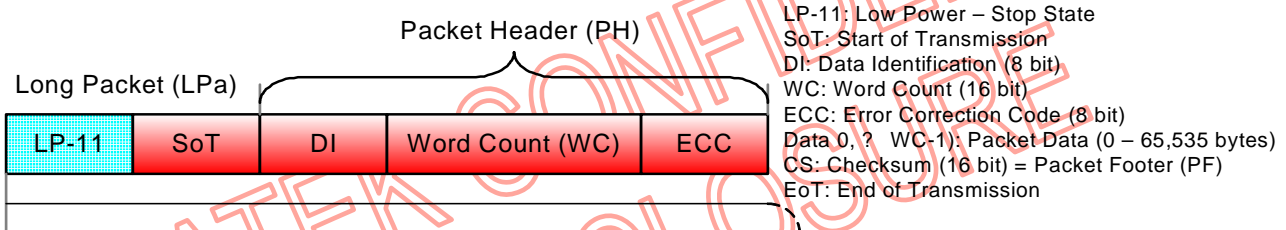
5.8.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter "Instruction Description", is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



Short Packet (SPa) Structure



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, no Parameter (GENW0-S), Data Type = 00 0011 (03h)
 This data type is useless in normal application.

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

“Generic Write, 1 Parameter” (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is “command” and 00h. “Generic Write, 1 Parameter” (GENW1-S) is used for Manufacture Command Set (CMD2, means panel function registers) writing only. Since all CMD2 registers are 1 “address” byte with 1 “parameter” byte. Therefore, this data type is useless in normal application.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

Data Type (DT, DI[5...0]): 01 0011b

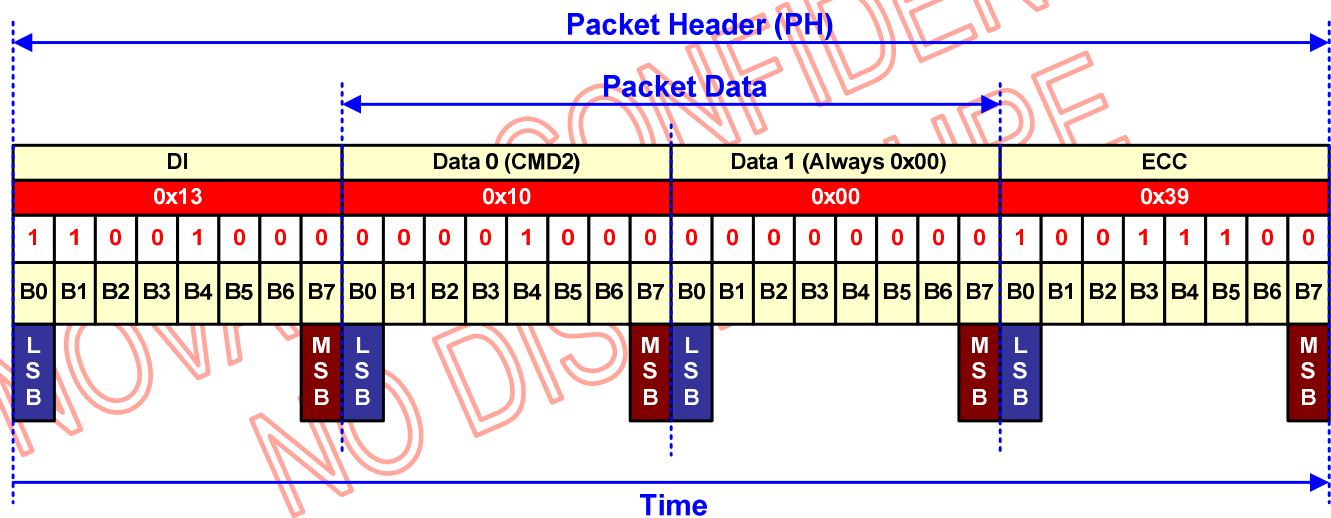
- Packet Data (PD)

Data 0: “POWER_CTRL15 (10h)”, the Power Control 15 in the page 0 of CMD2”

Data 1: Always 00hex

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 1 Parameter (GENW1-S) - Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes are "command" and "parameter". "Generic Write, 2 Parameter" (GENW2-S) is used for Manufacture Command Set (CMD2, means panel function registers) writing only.

Note : One Subpixel has been written.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b

Data Type (DT, DI[5...0]): 10 0011b

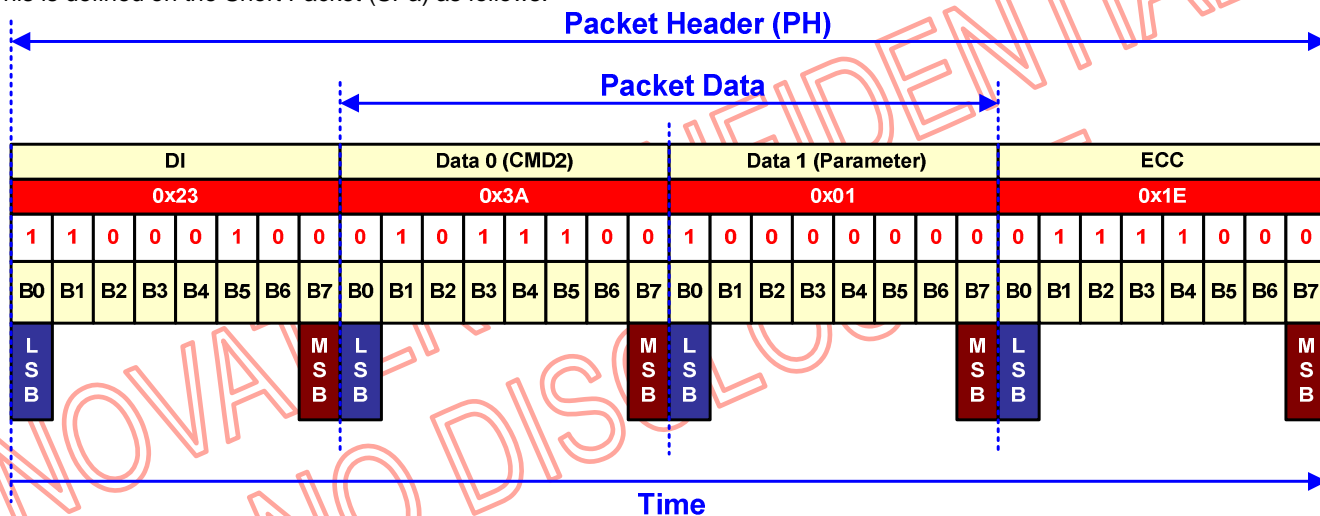
- Packet Data (PD)

Data 0: "3-GAMMA-R CTRL15 (3Ah)", the Red Gamma Control in page 0 of CMD2

Data 1: 01hex, the parameter of the CMD2

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) - Example

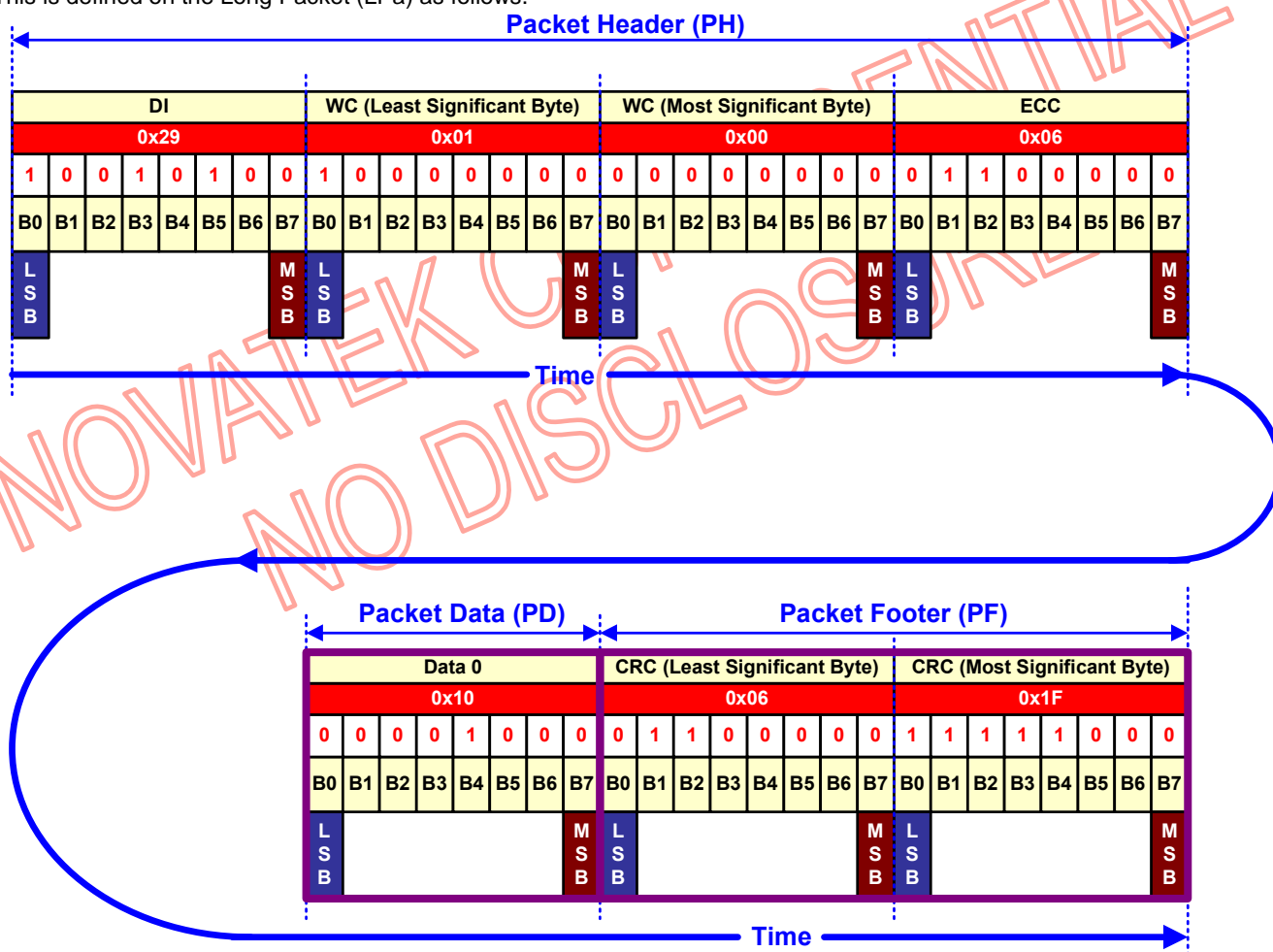
Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

“Generic Write Long” (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. The content of payload bytes are “command” with multiple “parameter”. “Generic Write Long” (GENW-L) is used for Manufacture Command Set (CMD2, means panel function registers) writing only.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
- Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



**Generic Write Long (GENW-L)
with CMD2 Only - Example**

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

Data Type (DT, DI[5...0]): 10 1001b

- Word Count (WC)

Word Count (WC): 0002h

- Error Correction Code (ECC)

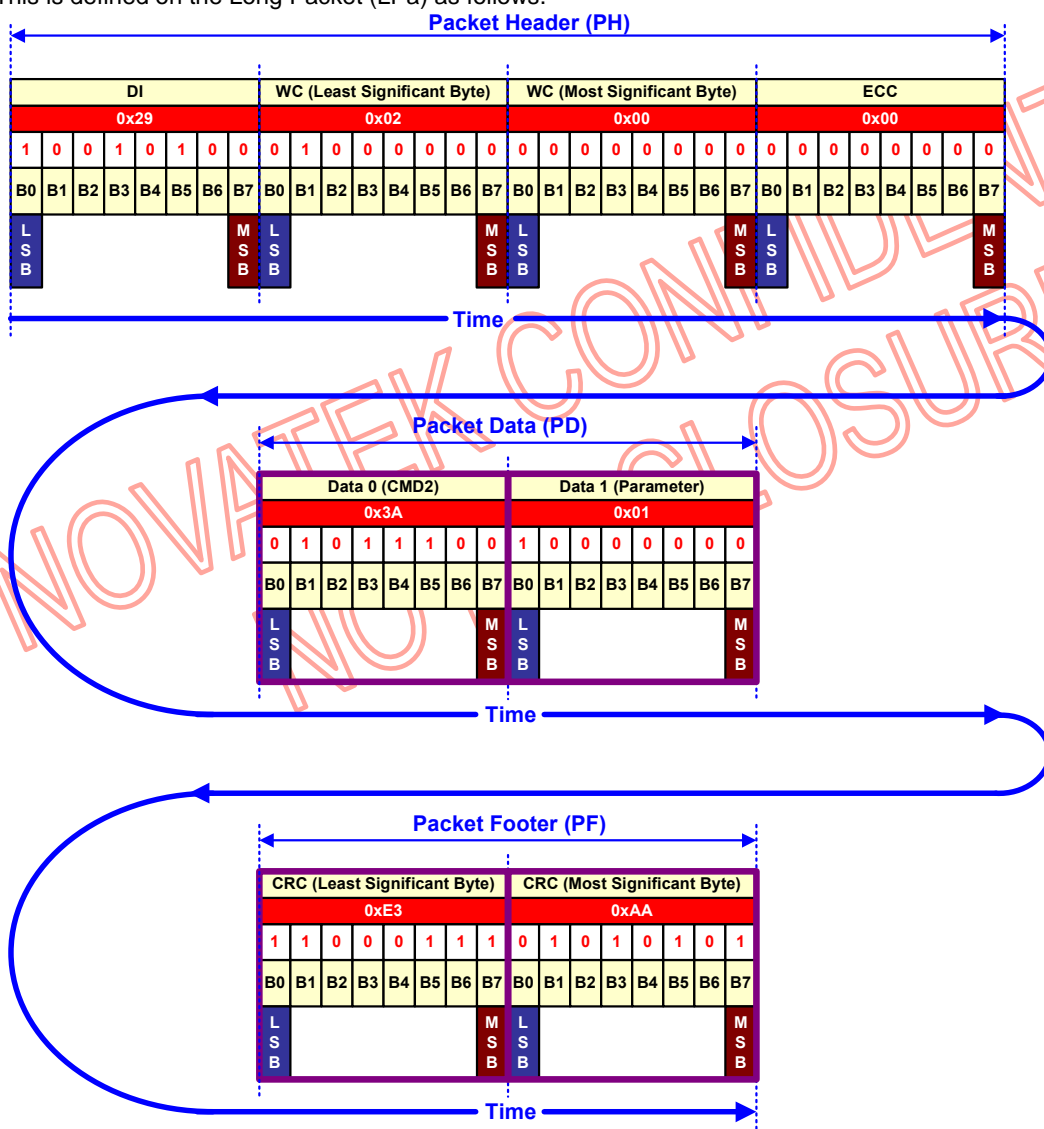
- Packet Data (PD):

Data 0: "3-GAMMA-R CTRL15 (3Ah)", the Red Gamma Control in page 0 of CMD2

Data 1: 01hex, Parameter of the CMD2

- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Generic Write Long with CMD2 and 1 Parameter - Example

Generic Read, No Parameter (GENR0-S), Data Type = 00 0100 (04h);
This data type is useless in normal application.

Generic Read, 1 Parameter (GENR1-S), Data Type = 01 0100 (14h); Generic Read, 2 Parameter (GENR2-S), Data Type = 10 0100 (24h)

"Generic Read, 1 Parameter / Generic Read, 2 Parameter" (GENR1-S / GENR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0100b) and Data Type (DT, 10 0100b), from the MCU to the display module. Generic read data type is used for Manufacture Command Set (CMD2, means panel function registers) reading only.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Generic Read, 1 Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

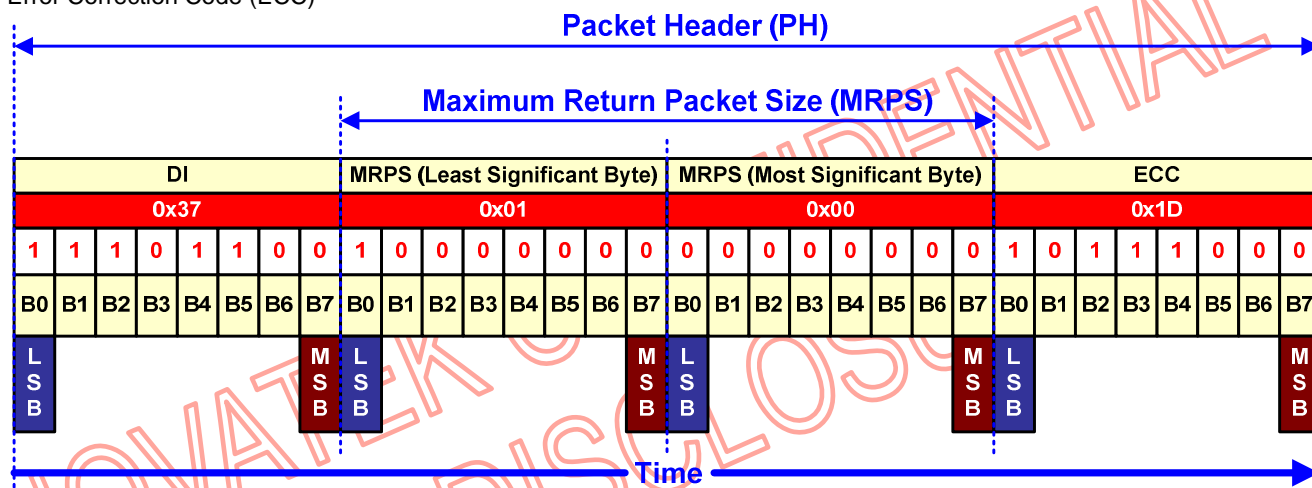
Data Type (DT, DI[5...0]): 11 0111b

- Maximum Return Packet Size (MRPS)

Data 0: 01hex

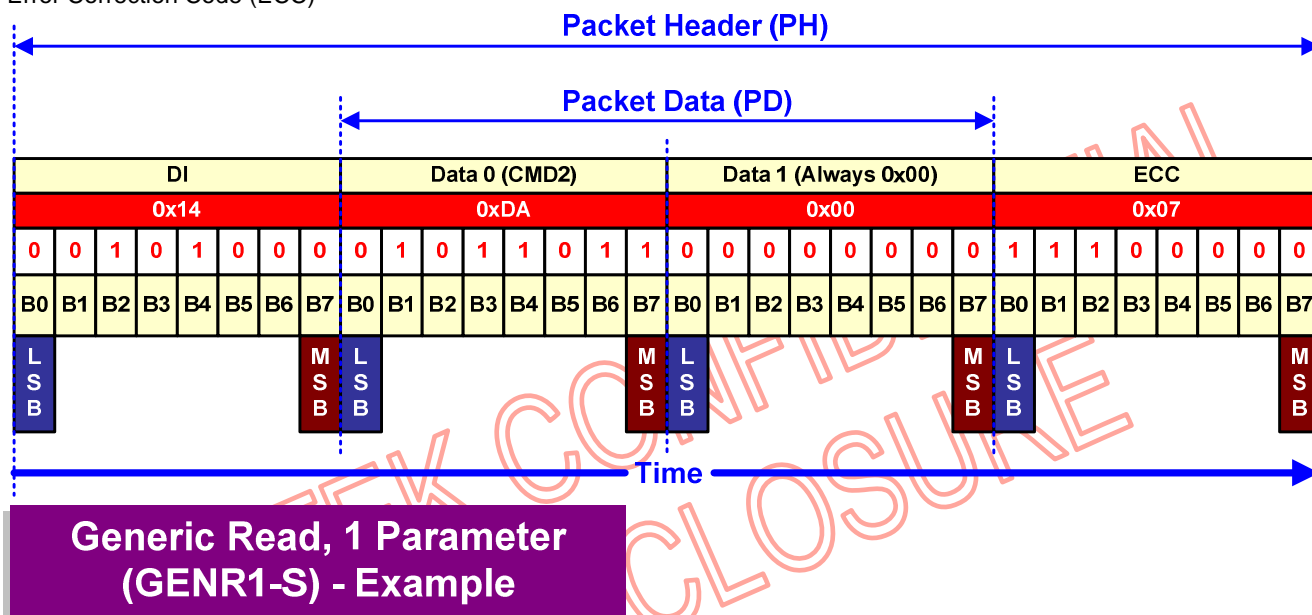
Data 1: 00hex

- Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

- Step 2:
- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Generic Read, 1 Parameter" to the display module
 - Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0100b
 - Packet Data (PD)
 - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
 - Data 1: Always 00hex
 - Error Correction Code (ECC)



- Step 3:
- The display module can send 2 different information to the MCU after Bus Turnaround (BTA)
- An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter "Acknowledge with Error Report (AwER)"
 - Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

“Display Command Set (DCS) Write, No Parameter” is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. The content of payload bytes are “command” with “00h”. “Display Command Set (DCS) Write, No Parameter” is used for User Command Set (CMD1) writing only.

Short Packet (SPa) is defined e.g.

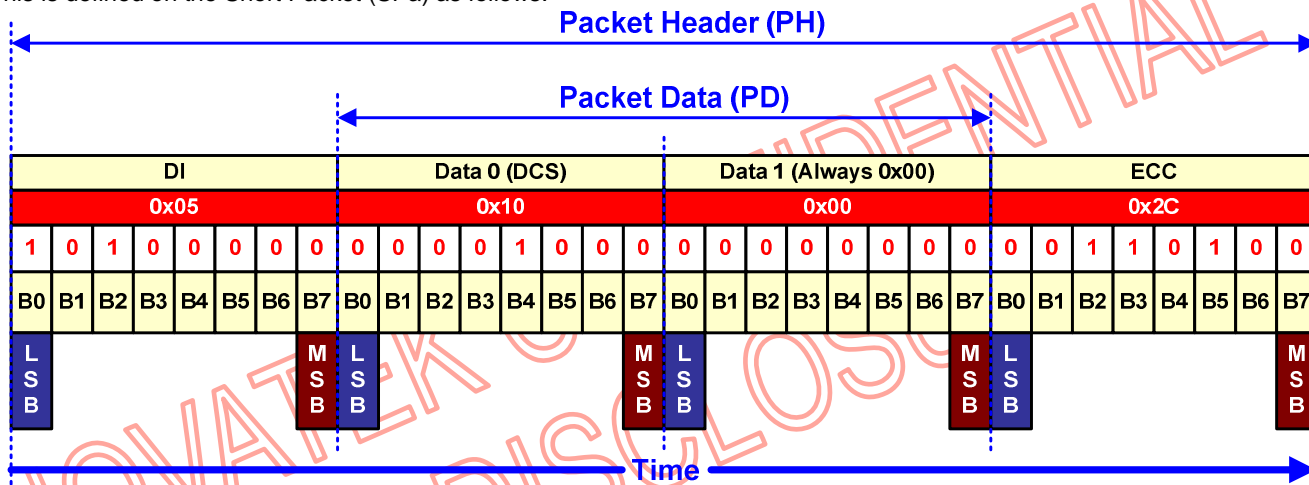
- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)

Data 0: “ENTER_SLEEP_MODE (10h)”, Display Command Set (DCS)

Data 1: Always 00hex

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. The content of payload bytes are “command” with one “parameter”. “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is used for User Command Set (CMD1) writing only.

Short Packet (SPa) is defined e.g.

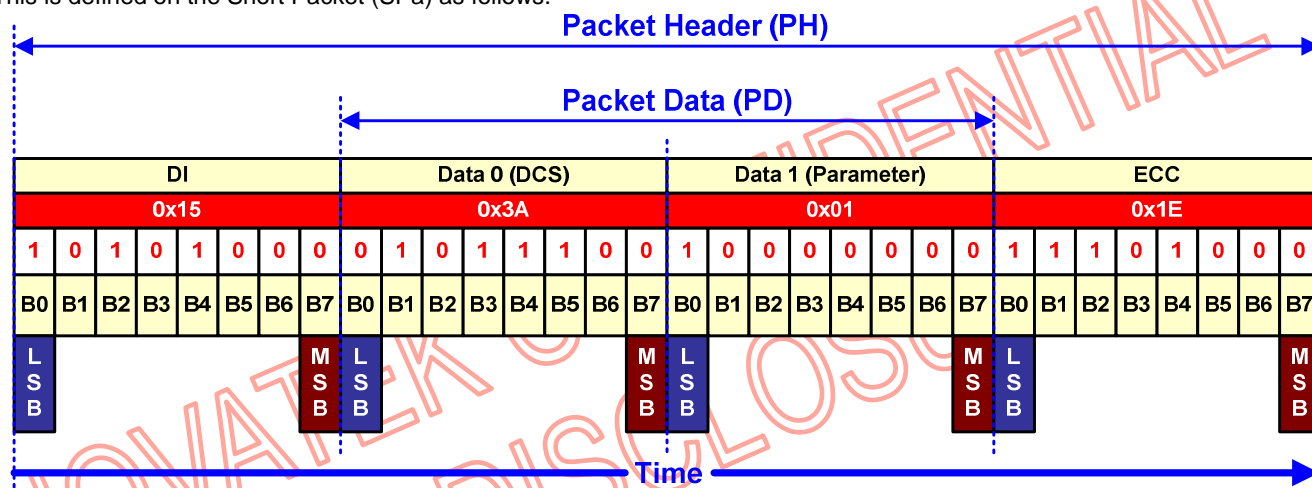
- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)

Data 0: “SET_PIXEL_FORMAT (3Ah)”, Display Command Set (DCS)

Data 1: 01hex, Parameter of the DCS

- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) - Example

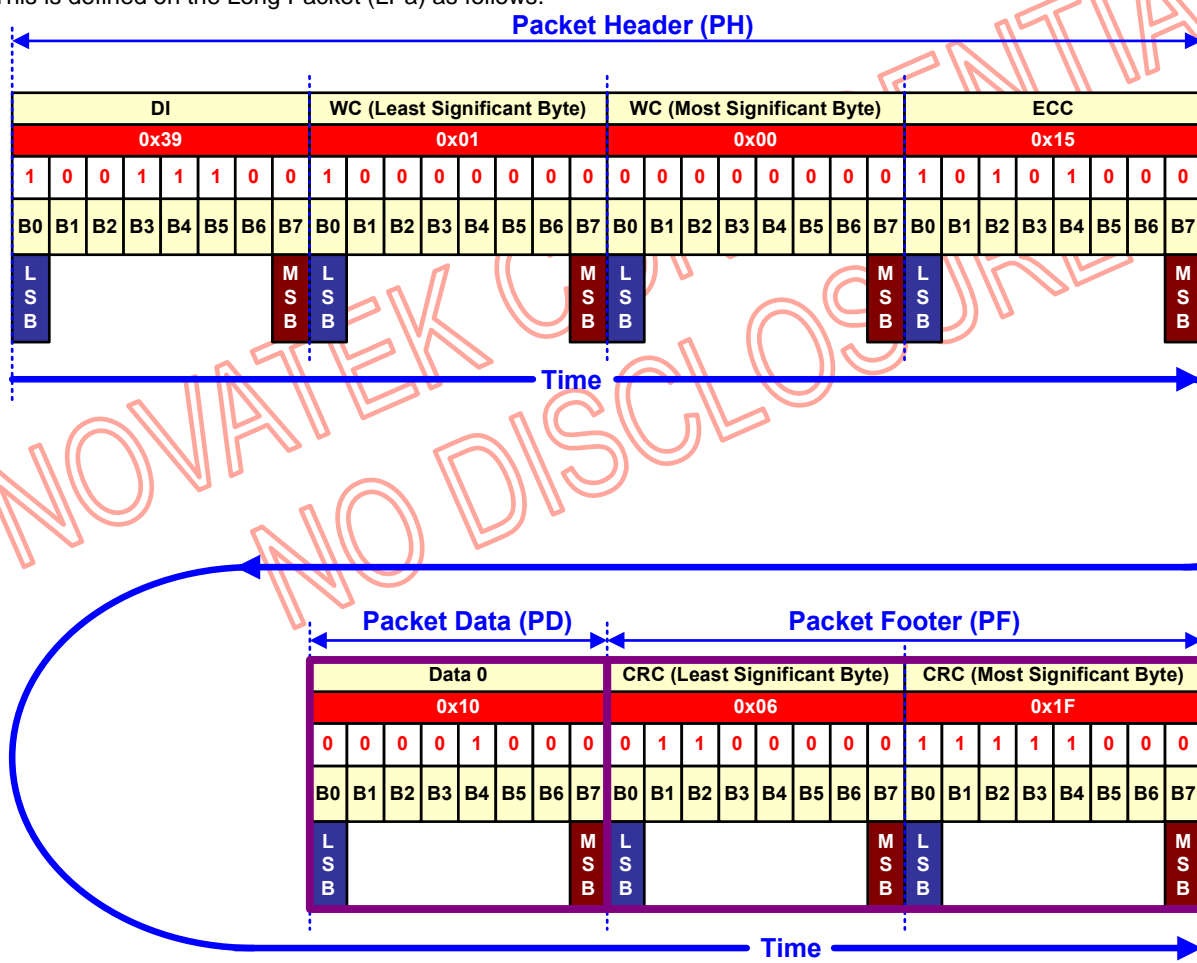
Display Command Set (DCS) Write Long (DCSW-L), Data Type = 11 1001 (39h)

“Display Command Set (DCS) Write Long” (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. The content of payload bytes are “command” with multiple parameter”. “Display command Set (DCS) Write Long” (DCSW-L) is used for User Command Set (CMD1) writing only.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
- Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “EXTER_SLEEP_MODE (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

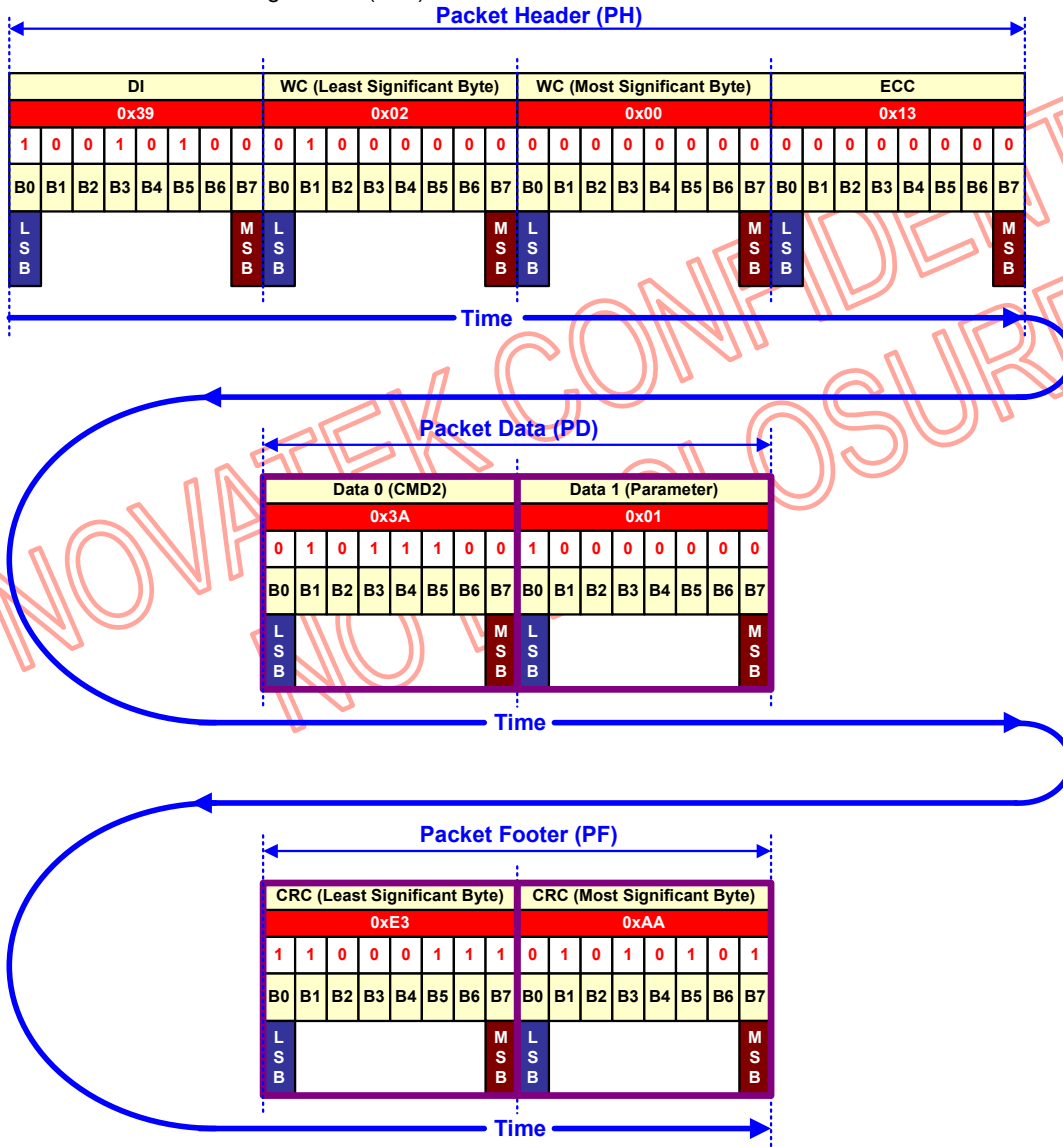


Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
- Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: "SET_PIXEL_FORMAT (3Ah)", Display Command Set (DCS)
- Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

Data Type (DT, DI[5...0]): 11 1001b

- Word Count (WC)

Word Count (WC): 0005h

- Error Correction Code (ECC)

- Packet Data (PD):

Data 0: "PARLINES (30h)", Display Command Set (DCS)

Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15...8]

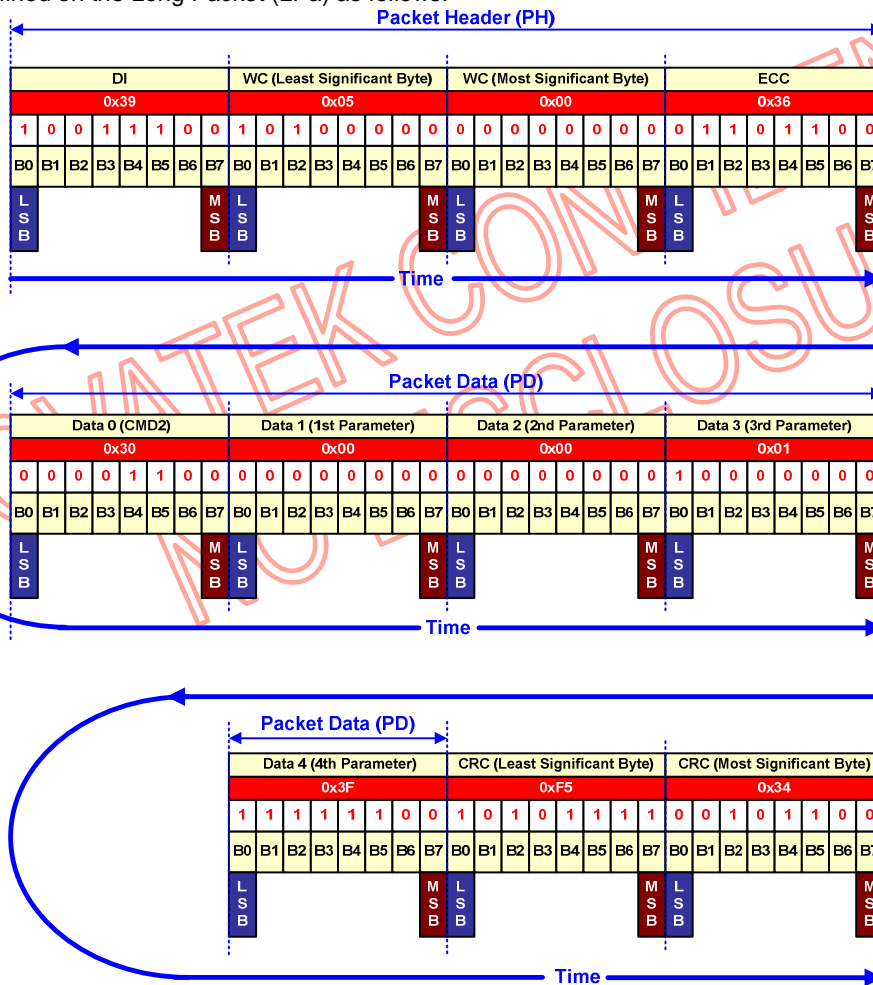
Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7...0]

Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15...8]

Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7...0]

- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S) , Data Type = 00 0110 (06h)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. The content of payload bytes are “command” with "00h". Display Command Set (DCS) Read, No Parameter (DCSRN-S) is used for User Command Set (CMD1) reading only.

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

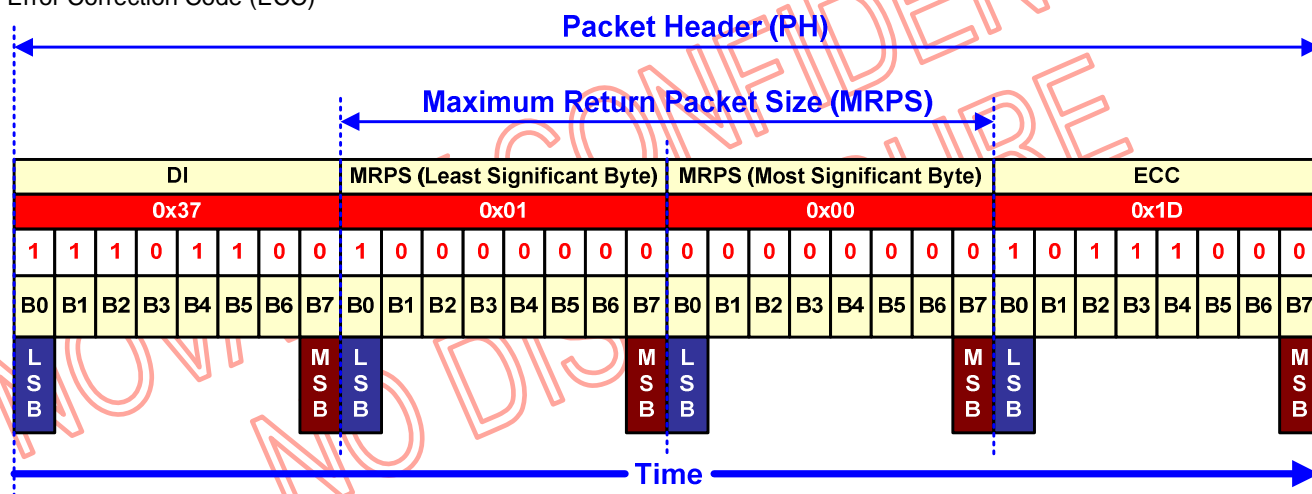
Data Type (DT, DI[5...0]): 11 0111b

- Maximum Return Packet Size (MRPS)

Data 0: 01hex

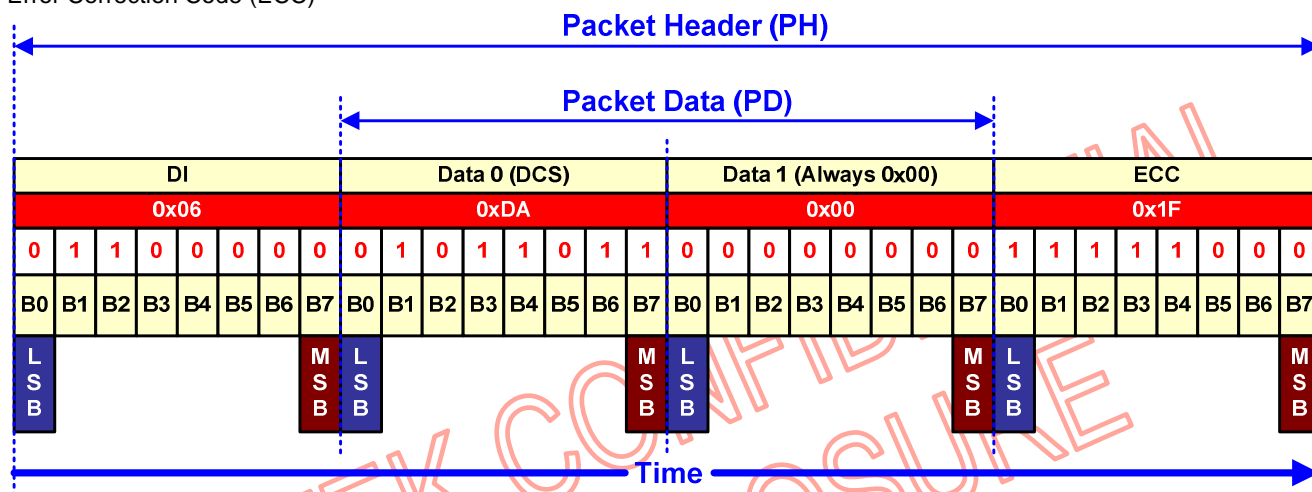
Data 1: 00hex

- Error Correction Code (ECC)



Set Maximum Return Packet Size (SMRPS-S) - Example

- Step 2:
- The MCU wants to receive a value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module
 - Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0110b
 - Packet Data (PD)
 - Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
 - Data 1: Always 00hex
 - Error Correction Code (ECC)



Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

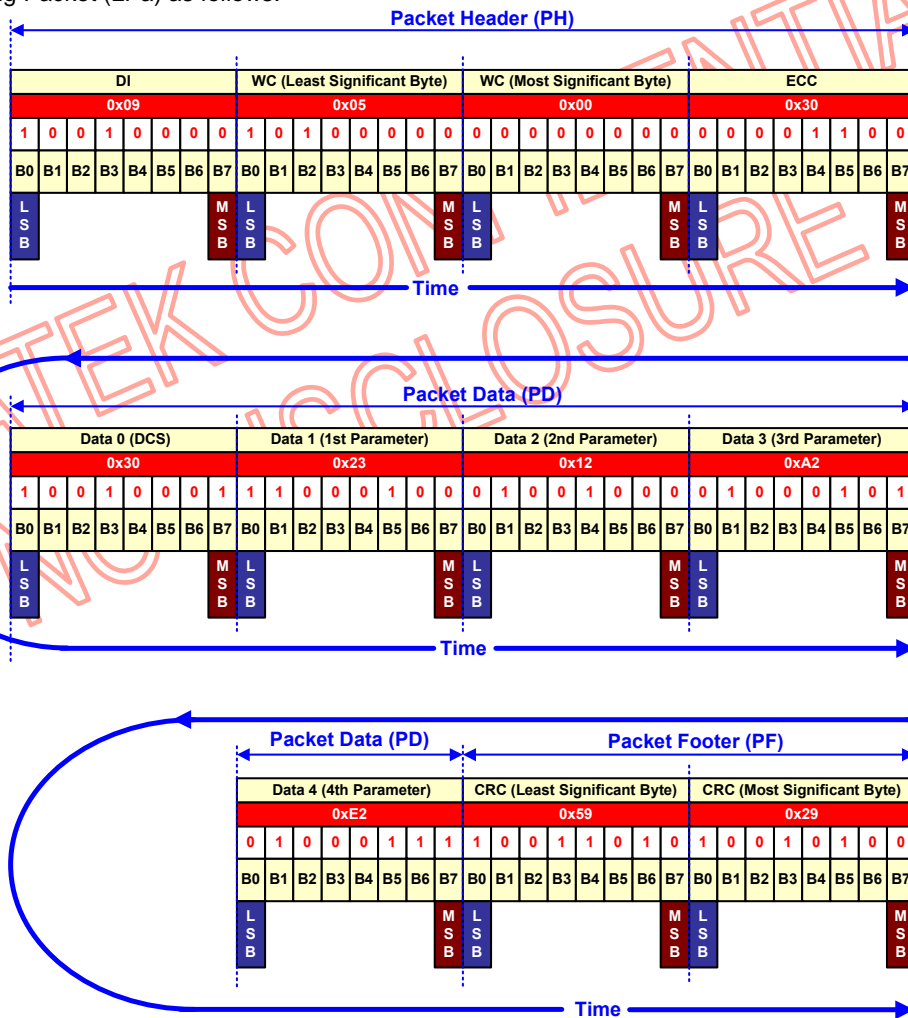
- Step 3:
- The display module can send 2 different information to the MCU after Bus Turnaround (BTA)
- An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter "Acknowledge with Error Report (AwER)"
 - Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending. Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
Virtual Channel (VC, DI[7...6]): 00b
Data Type (DT, DI[5...0]): 00 1001b
- Word Count (WC)
Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
Data 0: 89hex (Random data)
Data 1: 23hex (Random data)
Data 2: 12hex (Random data)
Data 3: A2hex (Random data)
Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Null Packet, No Data (NP-L) - Example

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

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EoT Packet, Data Type = 00 1000 (08h)

This new short packet is used for indicating the end of a HS transmission to the data link layer. As a result, detection of the end of HS transmission may be decoupled from physical layer characteristics. D-PHY defines an EoT sequence composed of a series of all 1's or 0's depending on the last bit of the last packet within a HS transmission. Due to potential errors, the EoT sequence could wrongly be interpreted as valid data types. Although EoT errors are not expected to happen frequently, the addition of this new packet will enhance overall system reliability.

Older devices compliant to earlier revisions of DSI specification do not support EoT packet generation or detection. All Hosts and Peripheral devices compliant to this revision of DSI specification, and going forward, shall incorporate capability of supporting EoT packet. They shall also provide means for enabling and disabling this capability – implementation specific – to ensure interoperability with older DSI devices not supporting EoT packet.

As mentioned earlier, the main objective of an EoT packet is to enhance overall robustness of the system during HS transmission mode. Therefore, DSI transmitters should not generate an EoT packet when transmitting in LP mode. The data link layer of DSI receivers shall detect and interpret arriving EoT packets regardless of transmission mode (HS or LP modes) in order to decouple itself from the PHY layer. Table below describes how DSI mandates EoT packet support for different transmission and reception modes.

EoT Support for Host and Peripheral

DSI Host (EoT capability enable)				DSI Peripheral (EoT capability enable)			
HS Mode		LP Mode		HS Mode		LP Mode	
Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit
Not Applicable	"Shall"	"Shall"	"Should not"	"Shall"	Not Applicable	"Shall"	"Should not"

Unlike other DSI packets, an EoT packet has a fixed format as follows:

- Data Type = DI [5:0] = 0b001000
- Virtual Channel = DI [7:6] = 0b00
- Payload Data [15:0] = 0x0F0F
- ECC [7:0] = 0x01

The virtual channel identifier associated with an EoT packet is fixed to 0, regardless of the number of different virtual channels present within the same transmission. For multi-Lane systems, the EoT packet bytes are distributed across multiple Lanes.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

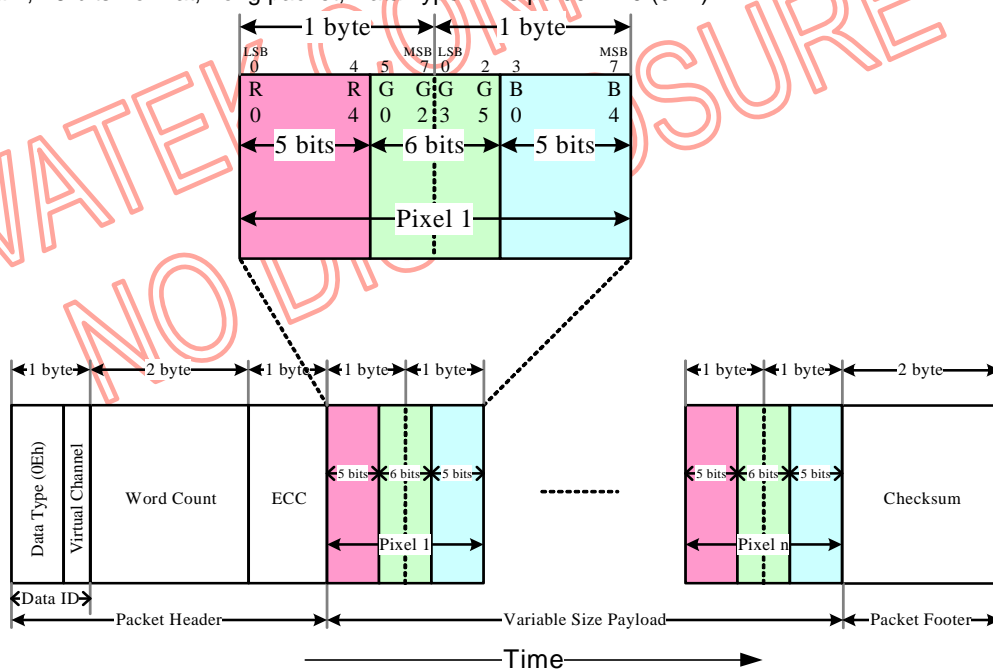
Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bits Format, Long packet, Data Type 1228 pe 00 1110 (0Eh)



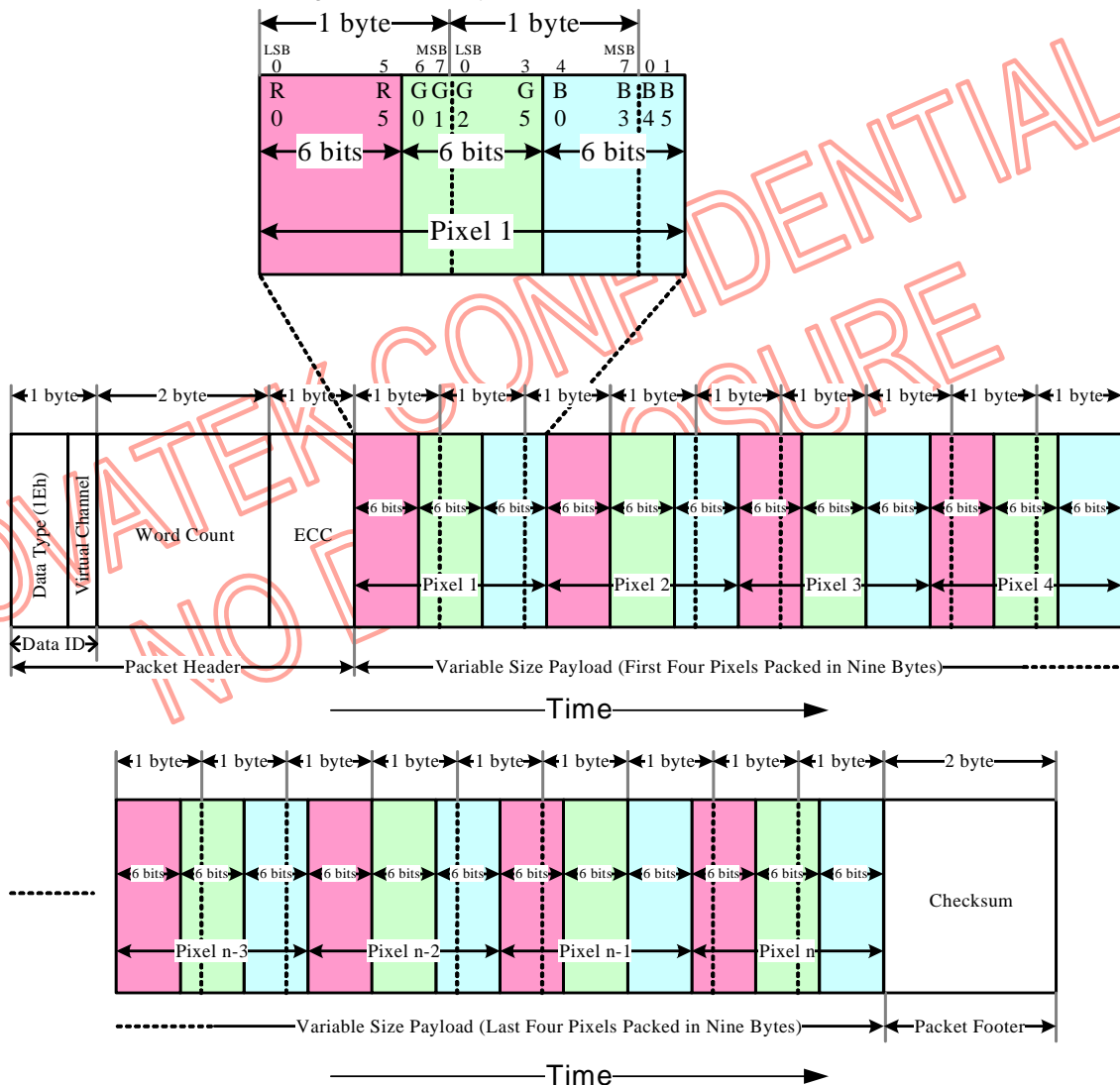
16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 16-Bits Format is a Long packet used to transmit image data formatted as 16-bits pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bit red, six bit green, five bit blue, in that order. Note that the "Green" component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bits Format, Long packet, Data type = 01 1110 (1Eh)



18-bit per Pixel (Packed)– RGB Color Format, Long packet

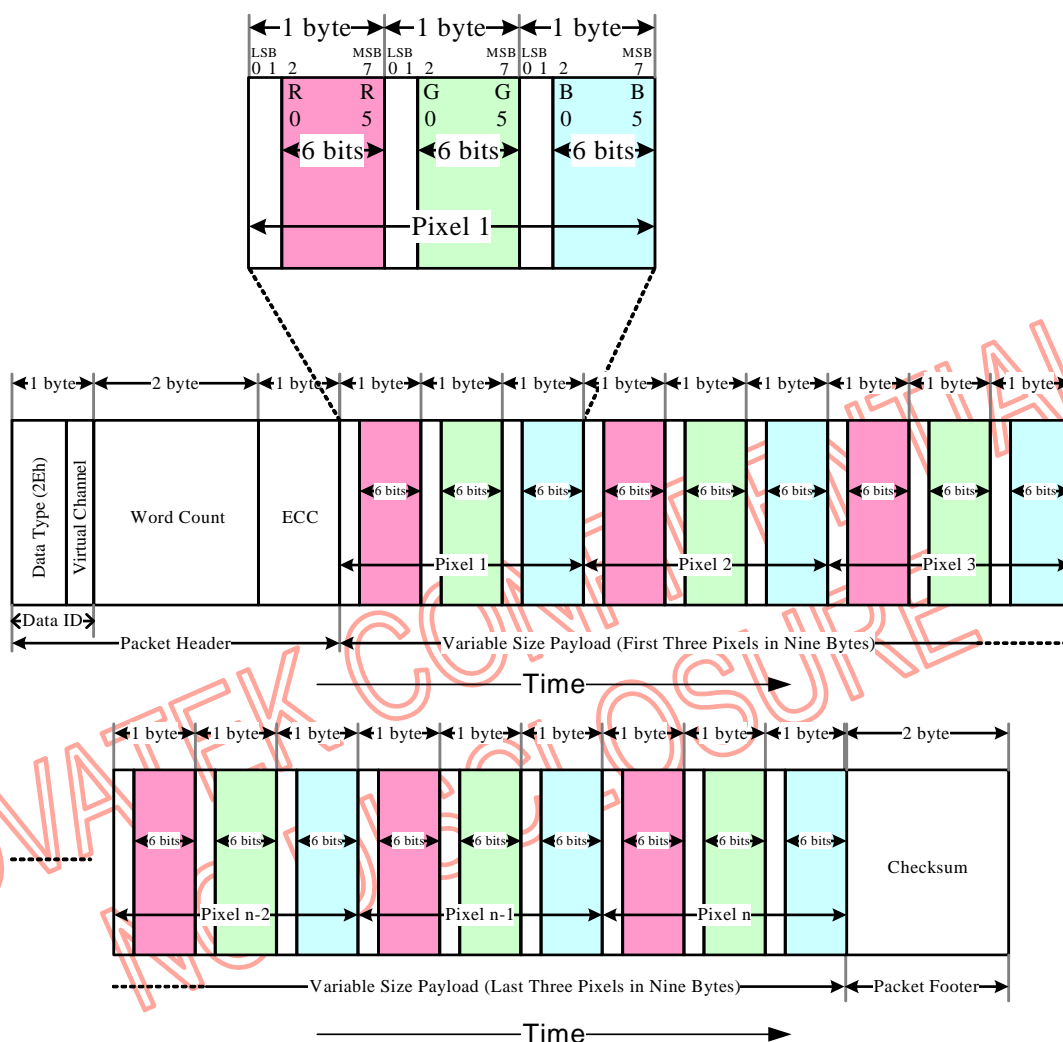
Packed Pixel Stream 18-Bits Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bits pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

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Pixel Stream, 18-bits Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



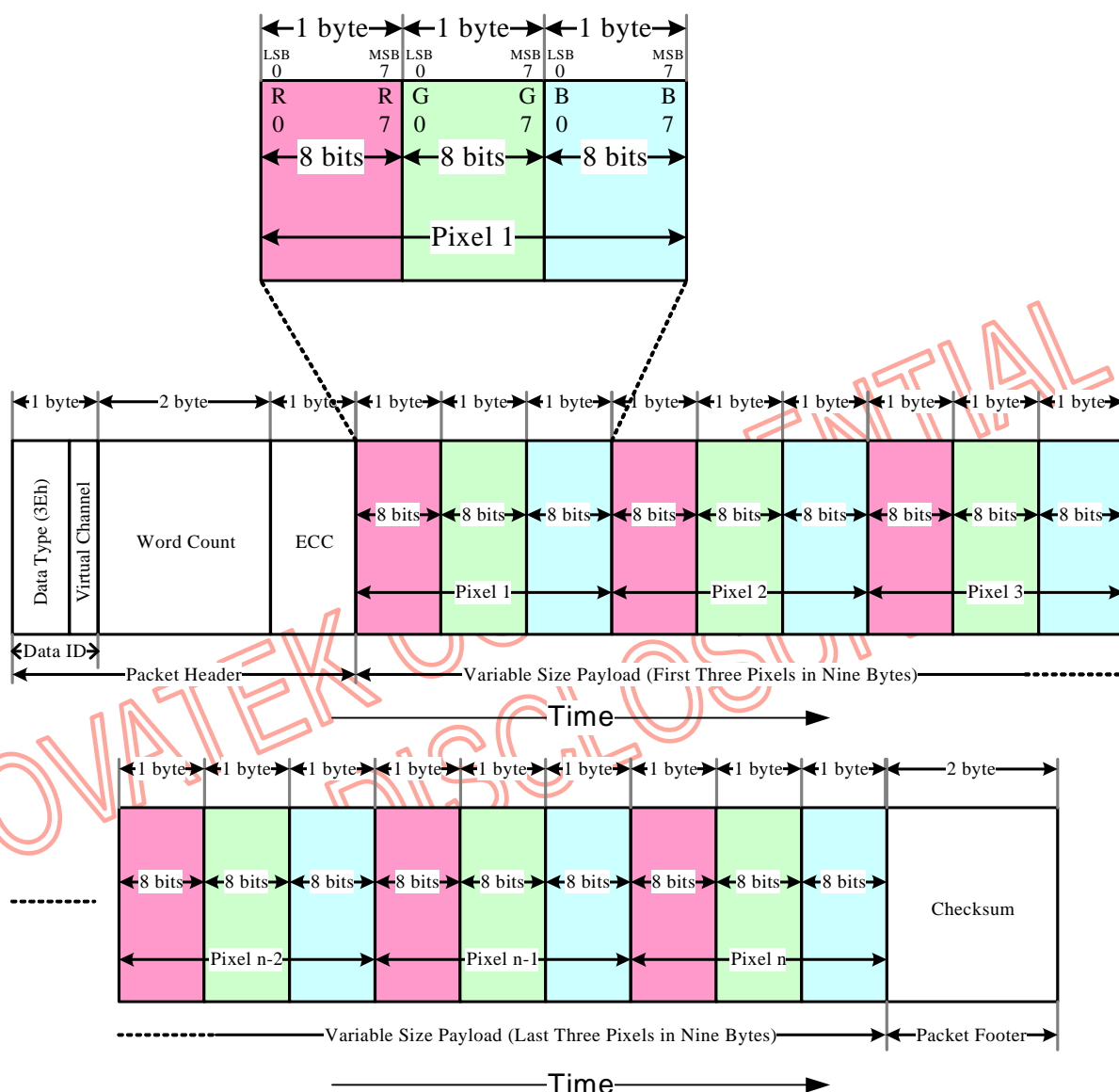
18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

In the 18-bits Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bits pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes. Packed Pixel Stream, 24-bits Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)



24-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Note:

NT35310 can accept MIPI DSI 8-8-8 pixel format packet in MIPI Command mode and Video mode. However, due to NT35310's RAM buffer is 18 bits depth per pixel, also the Source driver is 6 bits per channel, therefore only MSB 6 bits of each R/G/B sub-pixel can be stored in memory and displayed in LCD panel.

5.7.2.3.2.2 Packet from the Display Module to the MCU

Used Packet Types

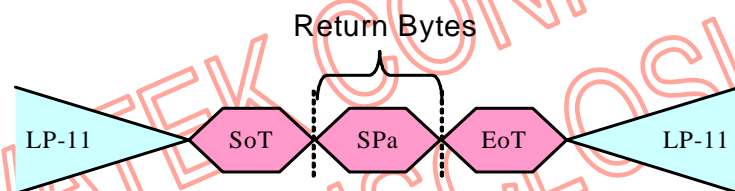
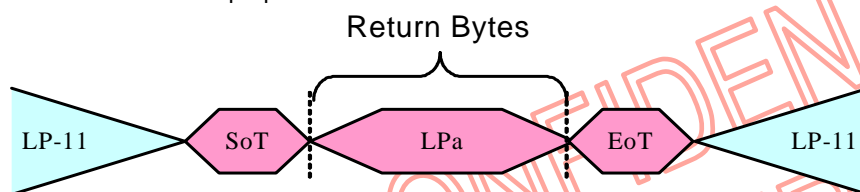
The display module is always using Short Packet (Spa) or Long Packet (Lpa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”.

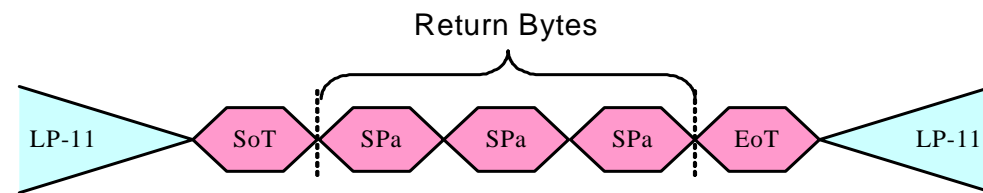
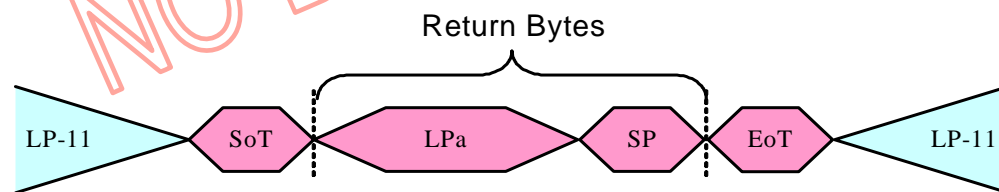
A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (Lpa) or Short Packet (Spa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is also possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.



Return Bytes on Single Packet



Return Bytes on Several Packets – Only for Reference Purposes

Data Types for Display Module-Sourced Packets

Data Type, (HEX)	Data Type, (BINARY)	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
08h	00 1000	EoT	End of Transmission (EoT) Packet	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	DCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	10 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Short Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Short Read Response, 2 Byte returned	Short

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bit, which are defining the current error, when a corresponding bits is set to ‘1’, as they are defined on the following table.

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)

Virtual Channel (VC, DI[7...6]): 00b

Data Type (DT, DI[5...0]): 00 0010b

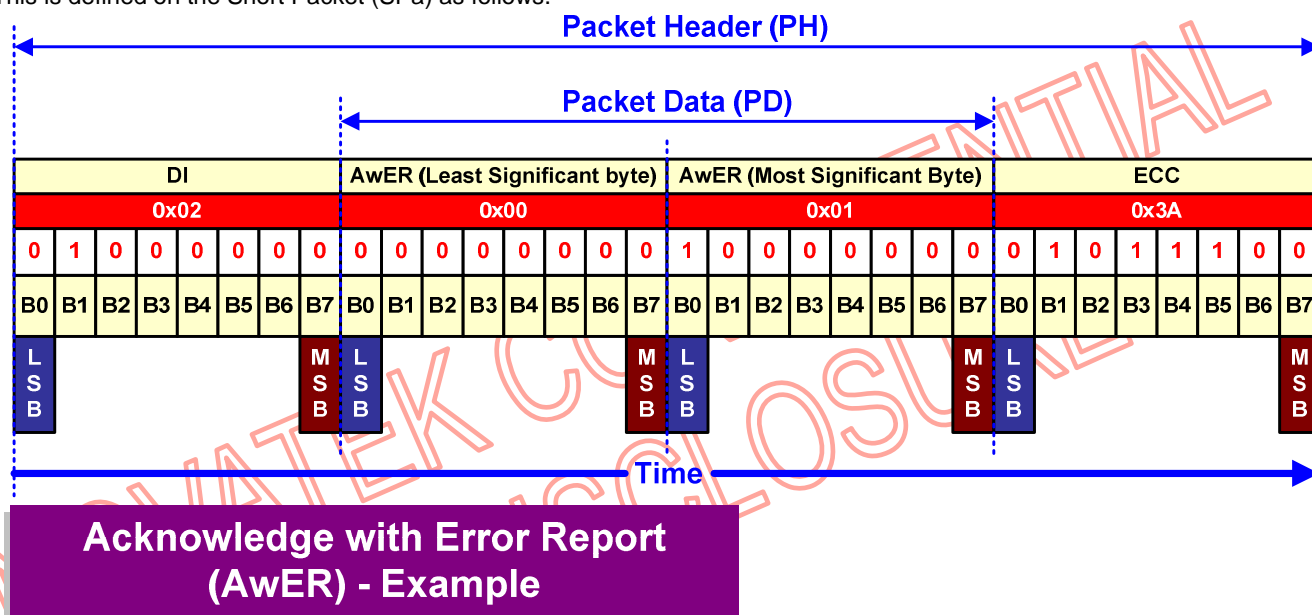
- Packet Data (PD)

Bit 8: ECC Error, single-bit (detected and corrected)

AwER: 0100h

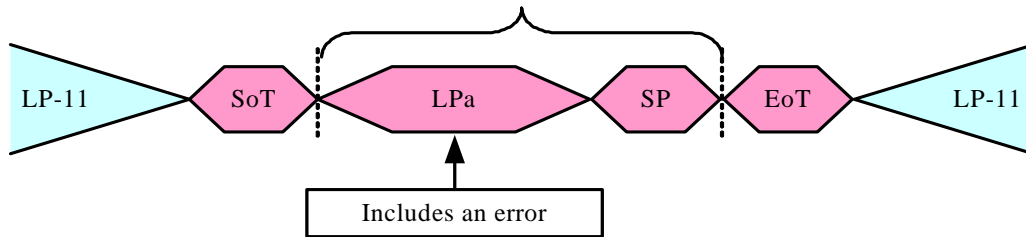
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

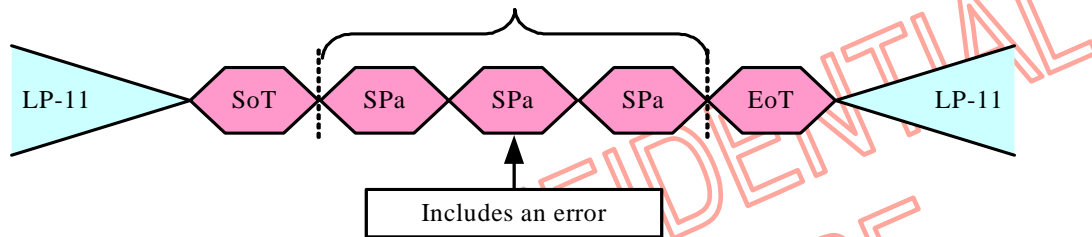


It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

Packets from the MCU



Packets from the MCU

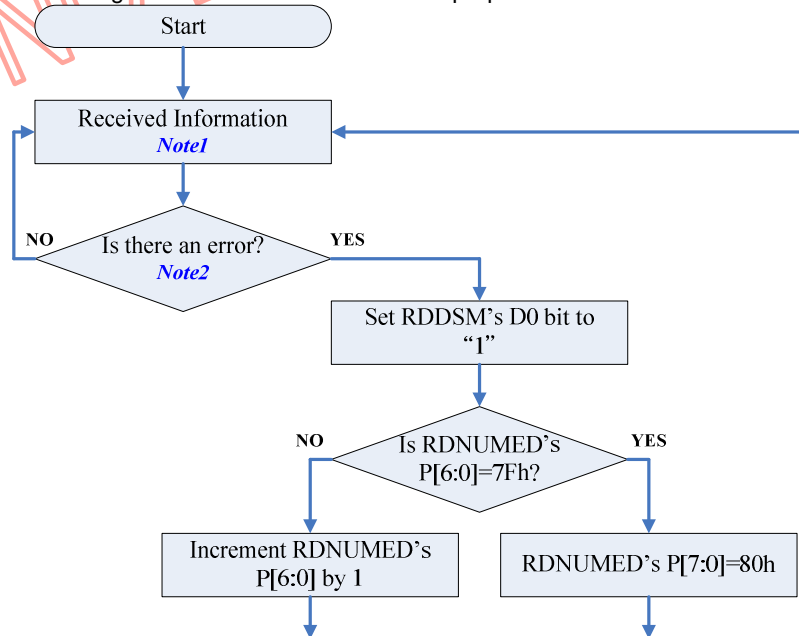


Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands.

The bit D0 of the "Read Display Signal Mode (0Eh)" command has been set to '1' if a received packet includes an error. The number of the packets, which are including an error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h as well as set the bits D0 of the "Read Display Signal Mode (0Eh)" command to '0' after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note1: This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.

Note2: CRC or ECC error.

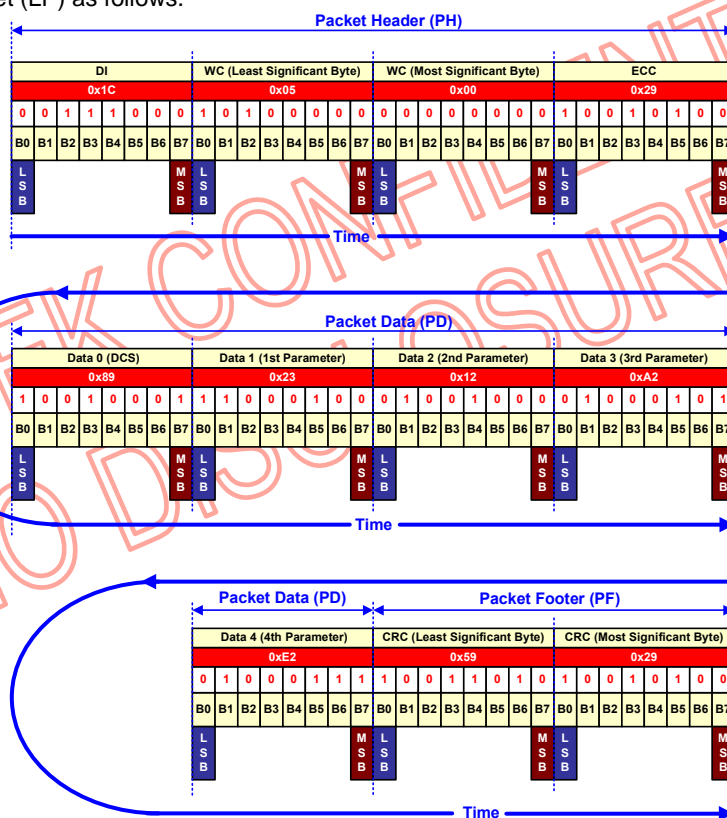
DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
- Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: 89hex
- Data 1: 23hex
- Data 2: 12hex
- Data 3: A2hex
- Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response (DCSRR-L) - Example

DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)
 "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

- Short Packet (SPa) is defined e.g.
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
 - Packet Data (PD)
 - Data 0: 45hex
 - Data 1: 00hex (Always)
 - Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

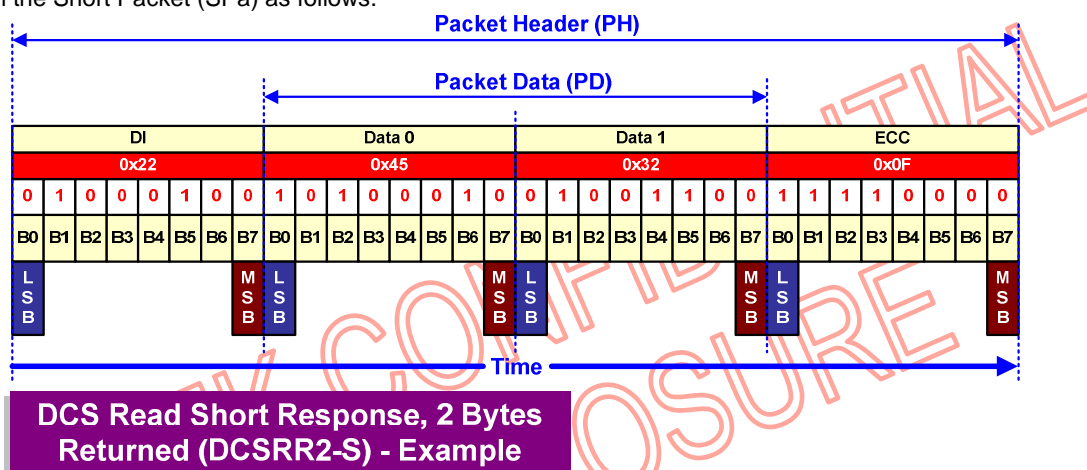
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)
 "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type

(DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



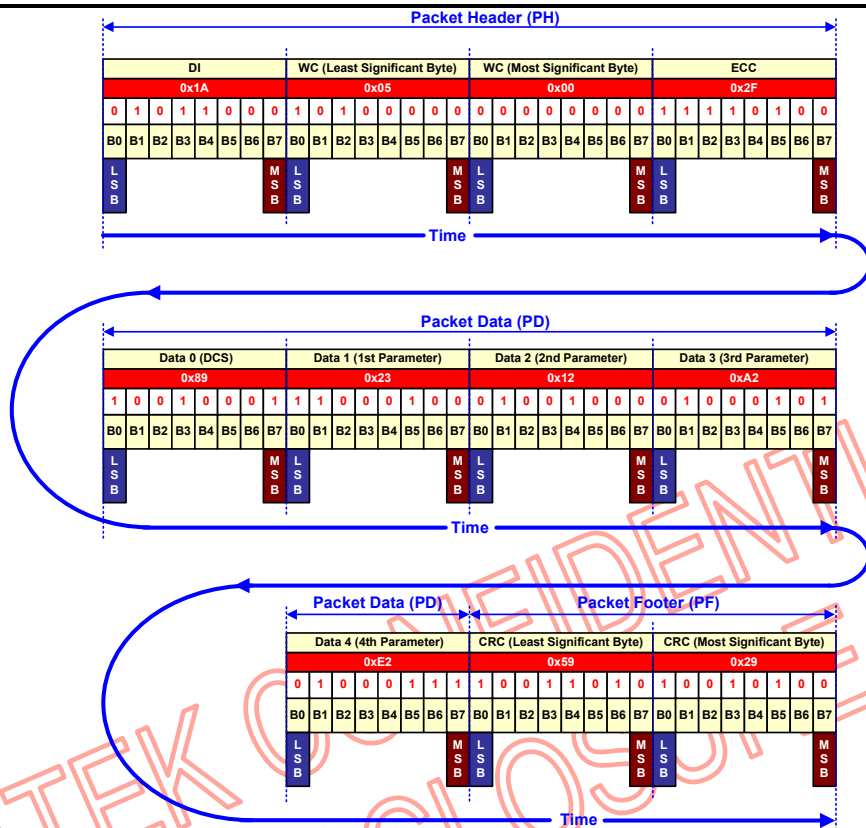
Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 01 1010b
- Word Count (WC)
- Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: 89hex
- Data 1: 23hex
- Data 2: 12hex
- Data 3: A2hex
- Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



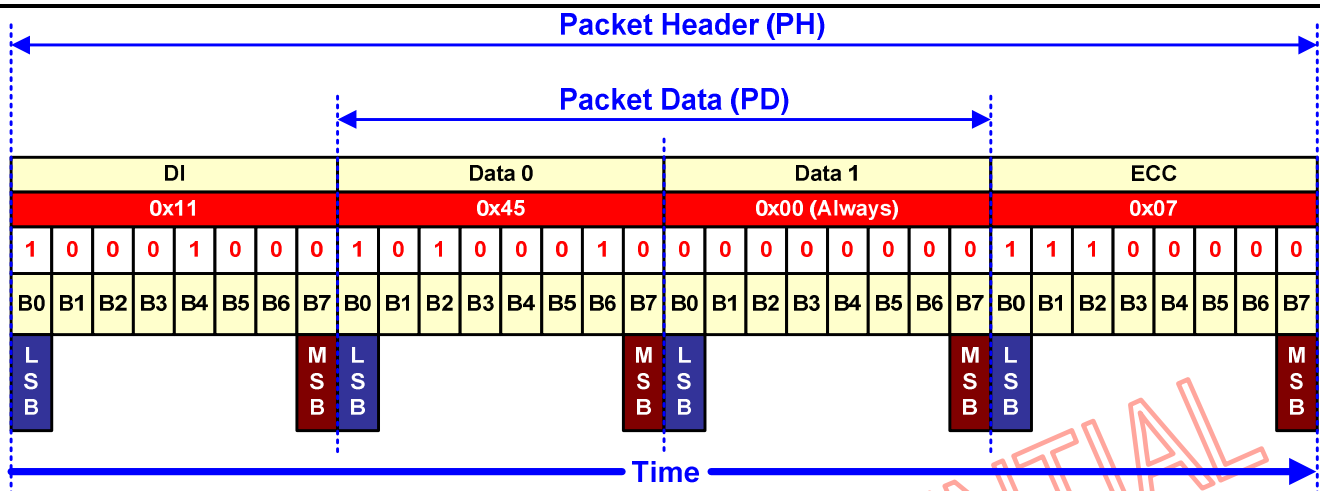
Generic Read Long Response (GENRR-L) - Example

Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

“Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. “Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

- Short Packet (SPa) is defined e.g.
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0001b
 - Packet Data (PD)
 - Data 0: 45hex
 - Data 1: 00hex (Always)
 - Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S) - Example

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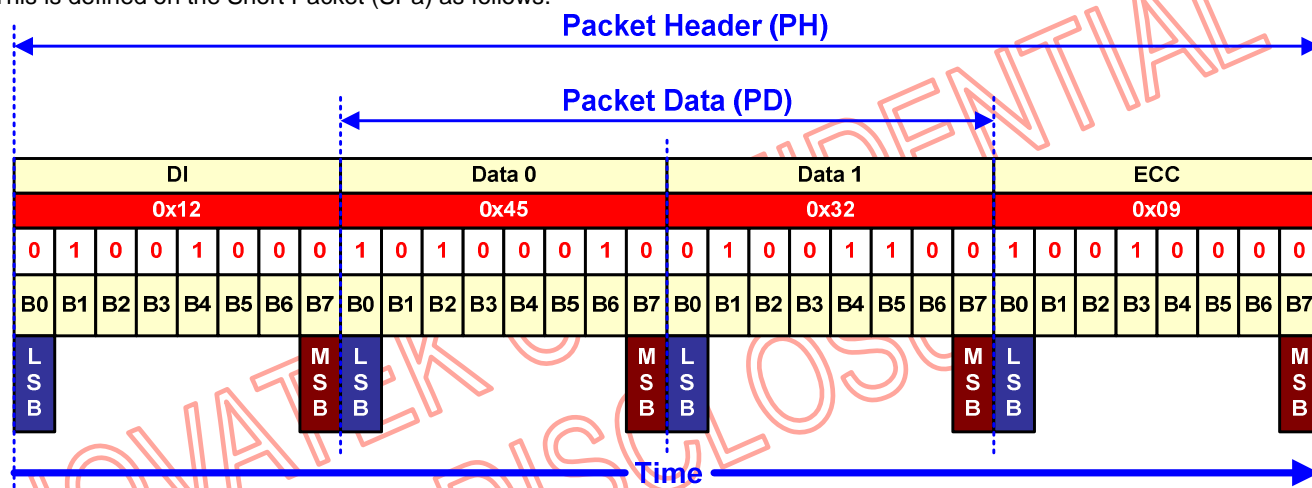
Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

“Generic Read Short Response, 2 Bytes Returned” (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. “Generic Read Short Response, 2 Bytes Returned” (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI[7...6]): 00b
- Data Type (DT, DI[5...0]): 01 0010b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Read Short Response, 2 Byte Returned (GENRR2-S) - Example

5.7.2.3.3 Communication Sequence

5.7.2.3.3.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters "Interface Level Communication" and "Packet Level Communication". This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.7.2.3.3.2 Sequences
DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
5	-	-	<=	LP-11	-	If no error => goto line 7 If error => goto line 12
6						
7	-	-	<=	ACK	-	No error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
10	-	LP-11	=>	-	-	End
11						
12	-	-	<=	LPDT	AwER	Error report
13	-	-	<=	LP-11	-	
14	-	BTA	<=>	BTA	-	
15	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Memory Write (2Ch)
3	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
4	DCSW-L	HSDT	=>	-	-	Memory Write Continue(3Ch)
5	DCSW1-S	HSDT	=>	-	-	Memory Write Continue(3Ch) with 1 parameter
6	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	LPDT	DCSRR1-S	Response 1 byte return
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	LPDT	DCSRR-L	Response 200 bytes return
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7						
8	-	-	<=	LPDT	DCSRR-L	Response 100 bytes return
9	-	-	<=	LPDT	DCSRR-L	Response 100 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7						
8	-	-	<=	LPDT	DCSRR-L	Response 199 bytes return
9	-	-	<=	LPDT	DCSRR1-L	Response 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence - Example 4

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read : 200 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response "Memory Read" (2Eh)
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 14
7	-	-	-	-	-	
8	-	-	<=	LPDT	DCSRR-L	Response 198 bytes return
9	-	-	<=	LPDT	DCSRR2-L	Response 2 bytes return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13	-	-	-	-	-	
14	-	-	<=	LPDT	AWER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	
17	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined on chapter "Null Packet, No Data (NP-L)" and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	-	LP-11	=>	-	-	End

5.7.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.7.2.4.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor

should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

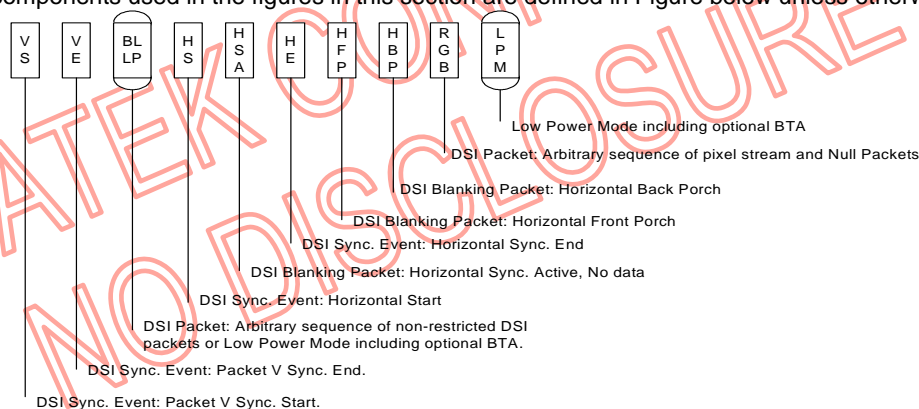
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scanline of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.

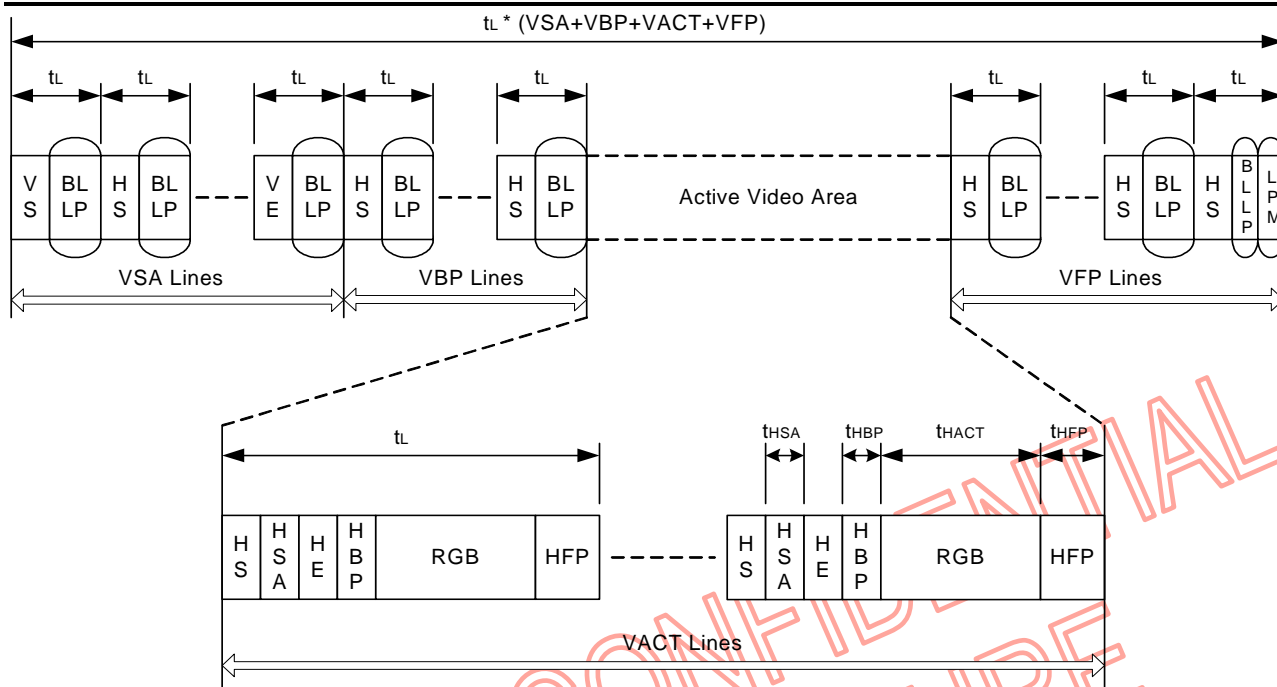


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.7.2.4.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

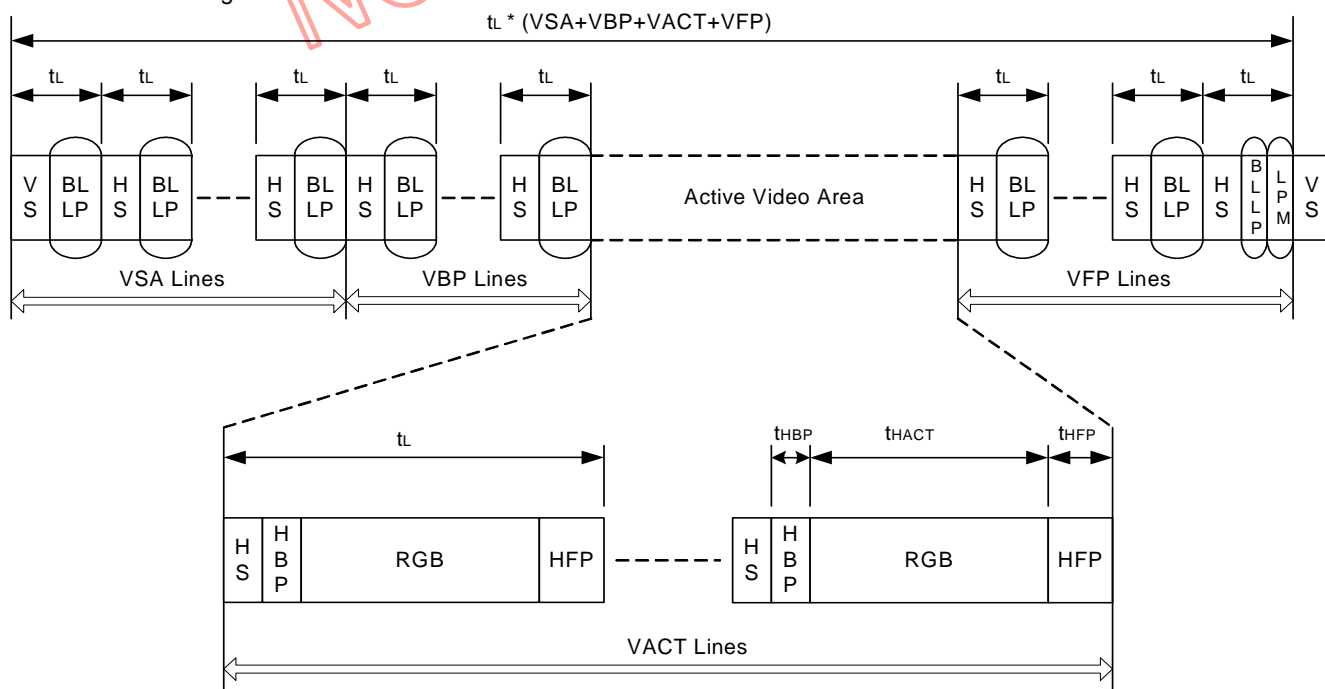


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.7.2.4.3 Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section 5.8.2.4.2 "Non-Burst Mode with Sync Pulse". Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

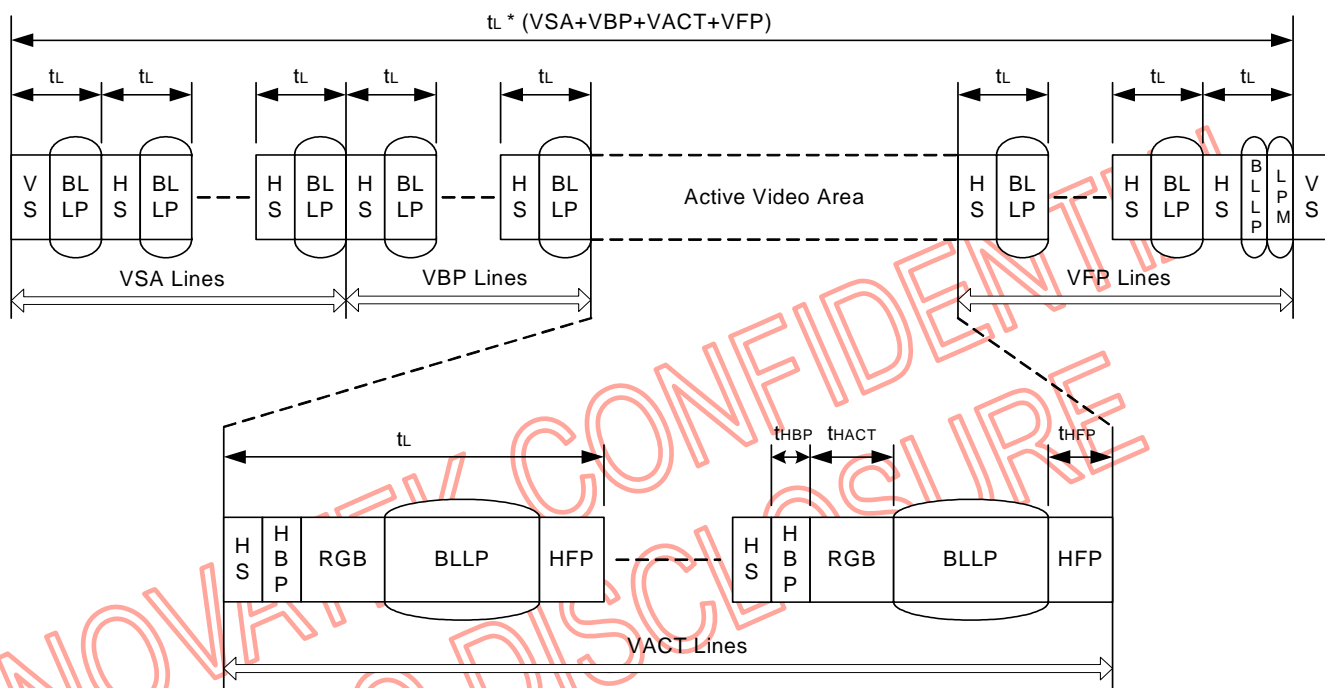


DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.7.2.4.4 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.7.2.4.5 Parameters

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

Required Peripheral Timing Parameters (Base on 320RGB x 480)

Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes	HVGA+ (320RGB x 480)	80	-	500	Mbps
tL	Line time	HVGA+ (320RGB x 480)	-	34 (Note 1)	-	us
tHBP	Horizontal back porch	HVGA+ (320RGB x 480)	1	-	-	us
tHACT	Time for image data	1 data lane	15	-	(Note 3)	us
HACT	Active pixels per line	HVGA+ (320RGB x 480)		320	-	pixels
tHFP	Horizontal front porch		1	-	-	us
VSA	Vertical sync active		1	-	-	H
VBP	Vertical back porch		TBD	-	-	H
VACT	Active lines per frame	HVGA+ (320RGB x 480)		480	-	H
VFP	Vertical front porch		TBD	-	-	H

Note 1: Frame rate (Typ) = 60Hz

Note 2: VBP (min) value can change by register.

Note 3: tHACT (max)= tL-tHFP- tHBP

5.7.2.4.6 Video mode ON/OFF sequence

In MIPI DSI interface, If host wants to enter/exit Video mode, please used the Bypass and DM commands and follow the flow as below.

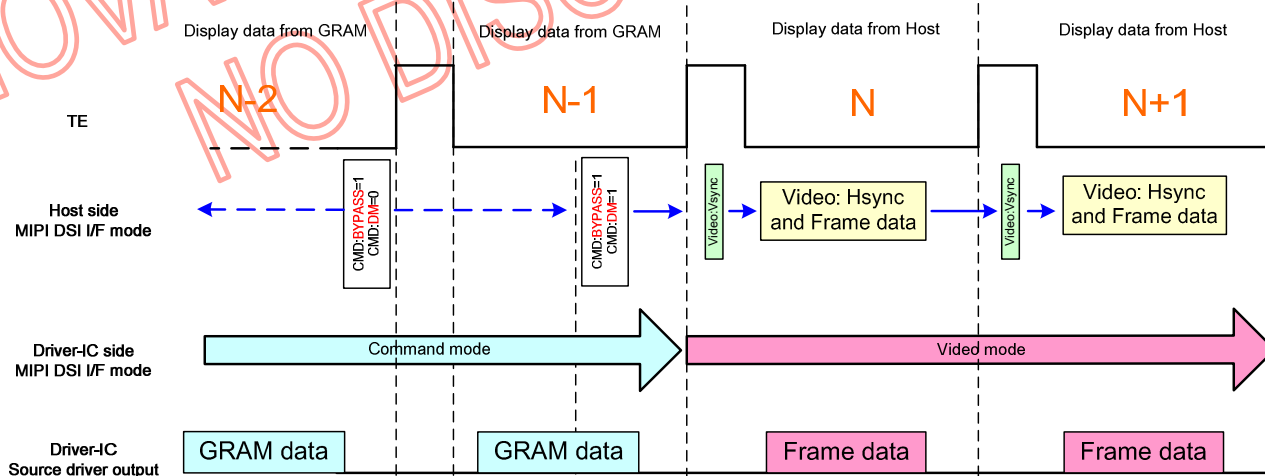


Figure 5.8.2.4.1 Turn on sequence in MIPI DSI Video mode

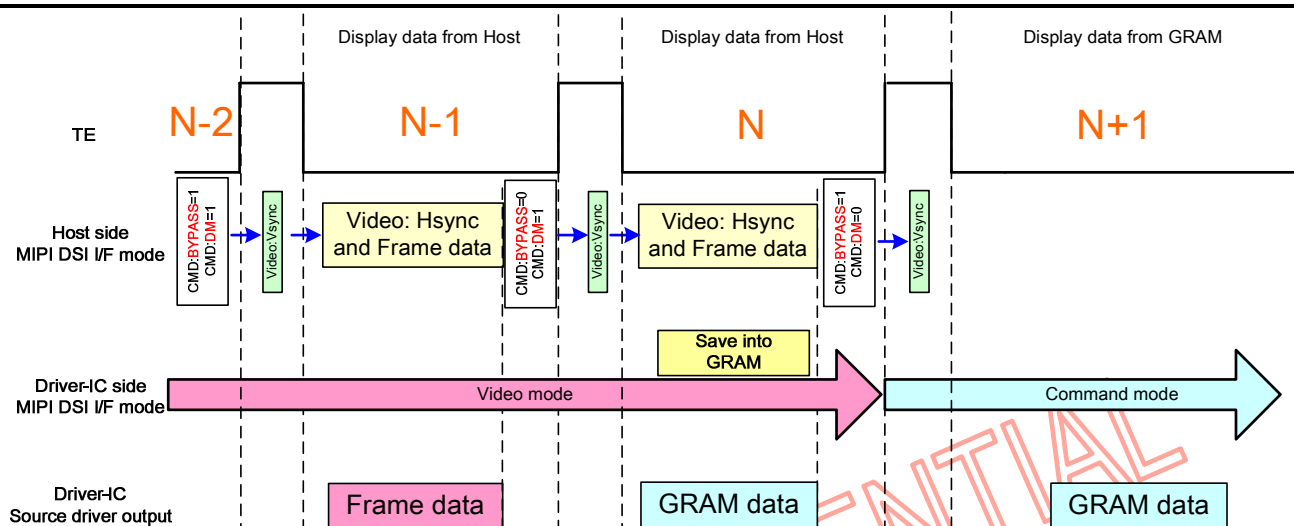


Figure 5.7.2.4.1 Shutdown sequence in MIPI DSI Video mode

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5.7.3 Memory access for DSI

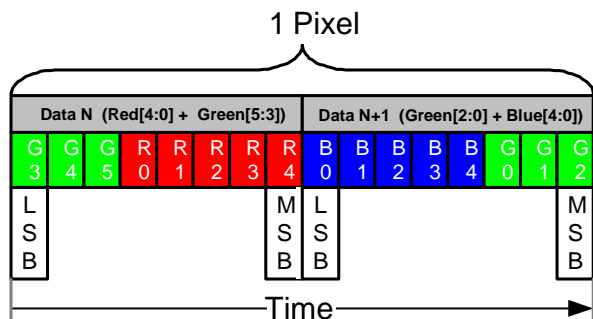
5.7.3.1 Memory write format

Different display data formats are available for three colors depth supported by the NT35310 listed below.

65k colors, RGB 5-6-5-bits input. Register command 3Ah="05h"

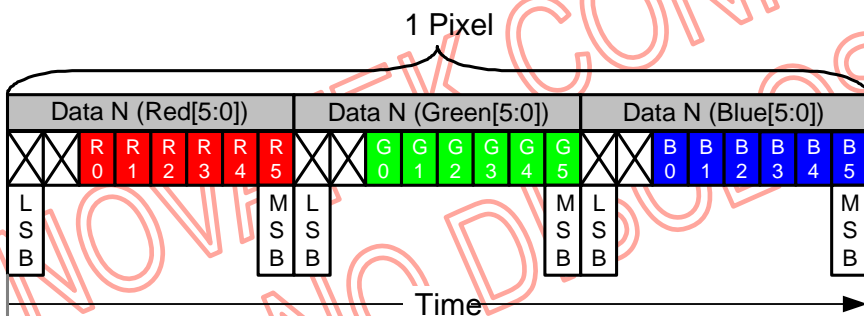
262k colors, RGB 6-6-6-bits input. Register command 3Ah="06h"

5-6-5-bits (65K colors)



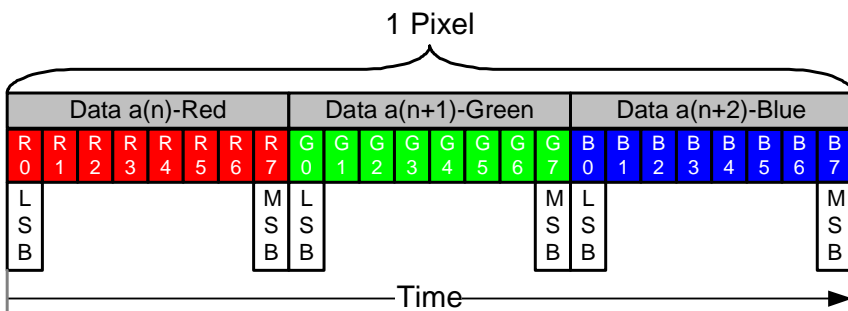
One Pixel Bit and Color Write Orders

6-6-6-bits (262K colors)



One Pixel Bit and Color Write Orders

8-8-8-bits (16.7M colors)



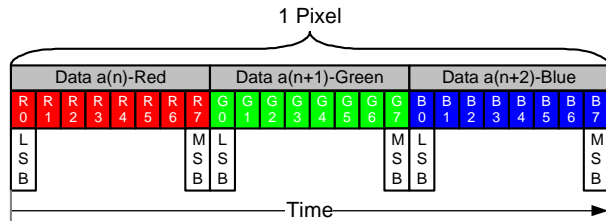
One Pixel Bit and Color Write Orders

Note:

NT35310 can accept MIPI DSI 8-8-8 pixel format packet in MIPI Command mode and Video mode. However, due to NT35310's RAM buffer is 18 bits depth per pixel, also the Source driver is 6 bits per channel, therefore only MSB 6 bits of each R/G/B sub-pixel can be stored in memory and displayed in LCD panel.

5.7.3.2 Memory writing/Reading

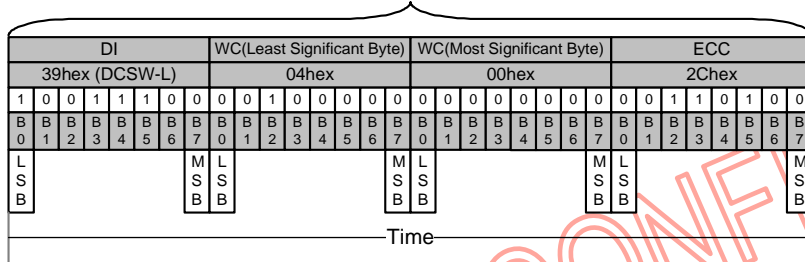
24 bit/pixel writing



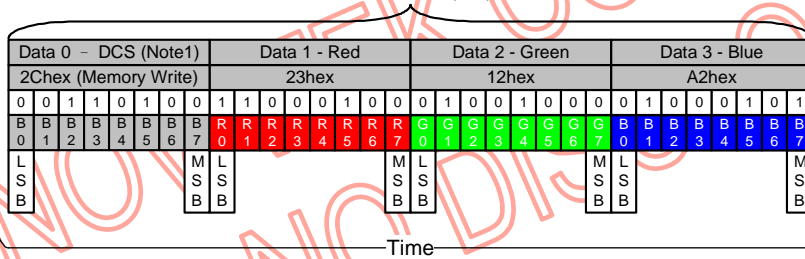
One Pixel Bit and Color Write Orders

The MCU can send to the display module a following packet

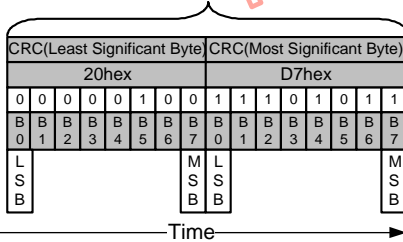
Packet Header (PH)



Packet Data (PD)



Packet Footer (PF)

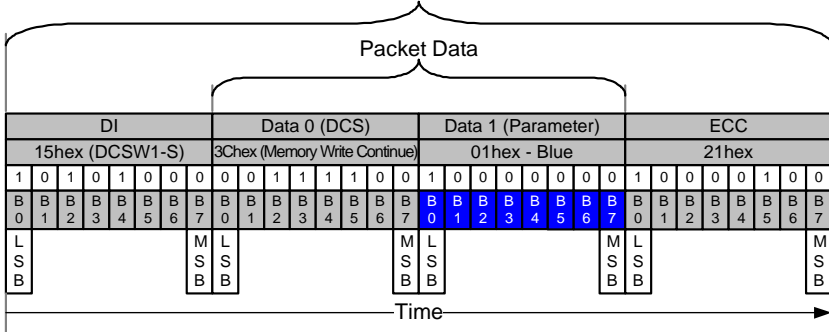


One Pixel Write (DCSW-L)

Notes:

- Memory Write (2Ch) or Memory Write Continue (3Ch)
- It is possible that one pixel information is split in two or three different packets which are ending and starting as follows:
 - R - GB (2 packets)
 - RG - B (2 packets)
 - R - G - B (3 packets)
- Packet can include several pixels (Not only one pixel as in this example)

Packet Header (PH)

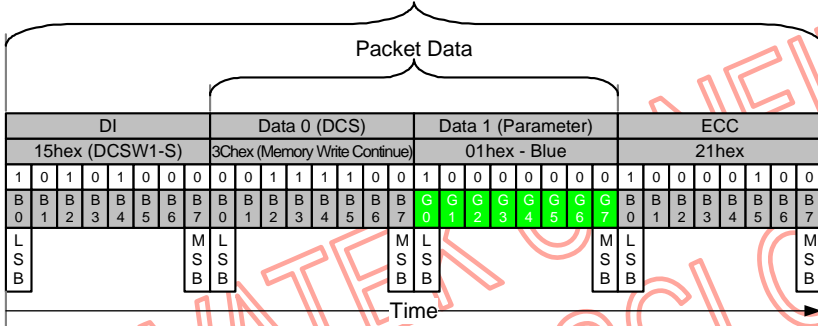


Blue Subpixel Write (DCSW1-S)

Notes:

- DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)
- Previous data byte was G[0:7]

Packet Header (PH)

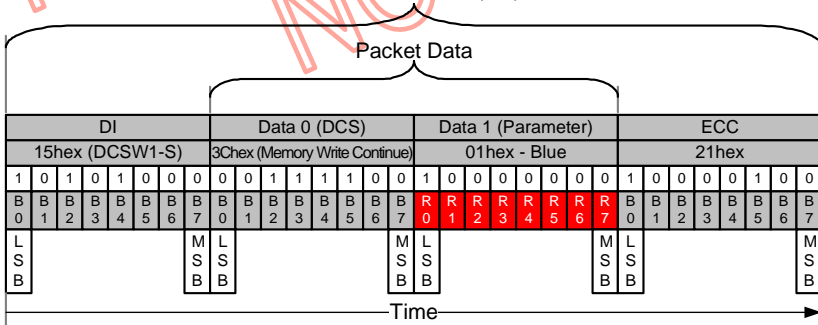


Green Subpixel Write (DCSW1-S)

Notes:

- DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)
- Previous data byte was R[0:7]

Packet Header (PH)



Red Subpixel Write (DCSW1-S)

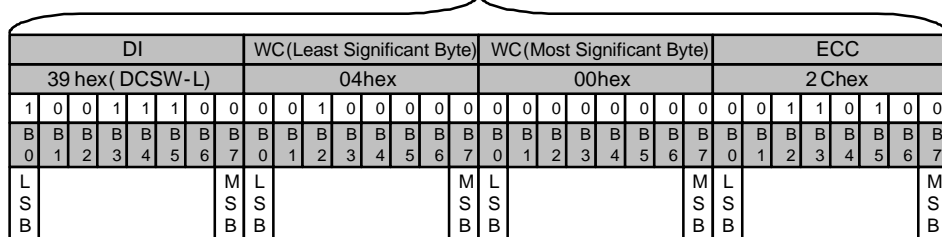
Note: DCS (Data 0) can also be "Memory Write Continue" (3Ch) command

18 bits/pixel writing

The MCU can send to the display module a following packet

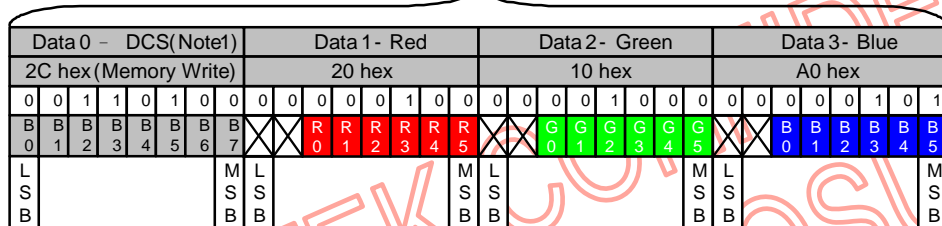
Example1: One pixel write

Packet Header (PH)



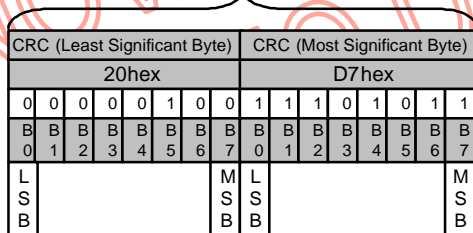
Time

Packet Data (PD)



Time

Packet Footer (PF)



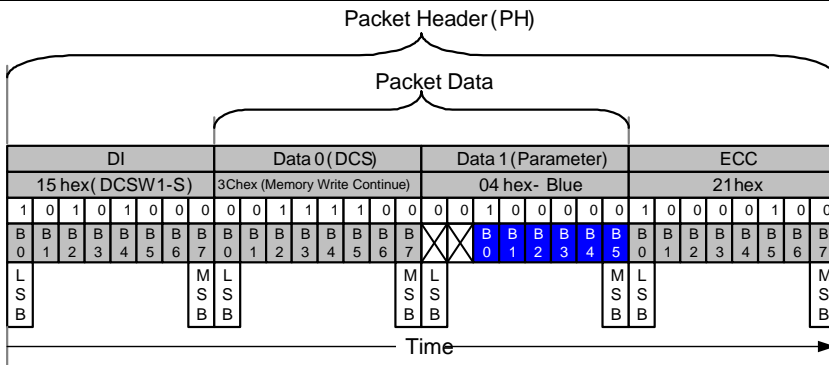
Time

One Pixel Write (DCSW-L)

Notes:

- Memory Write (2Ch) or Memory Write Continue (3Ch)
- It is possible that one pixel information is split in two or three different packets starting as follows:
 - R – GB (2 packets)
 - RG – B (2 packets)
 - R – G – B (3 packets)
- Packet can include several pixels (Not only one pixel as in this example)

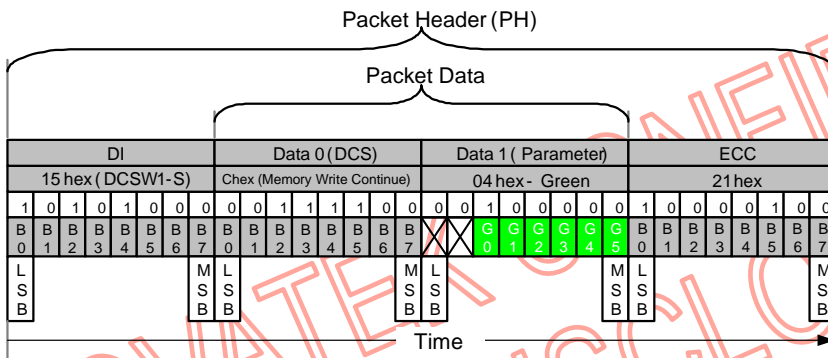
Example2: Blue sub-pixel write



Blue Subpixel Write (DCSW1-S)

Note: DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)

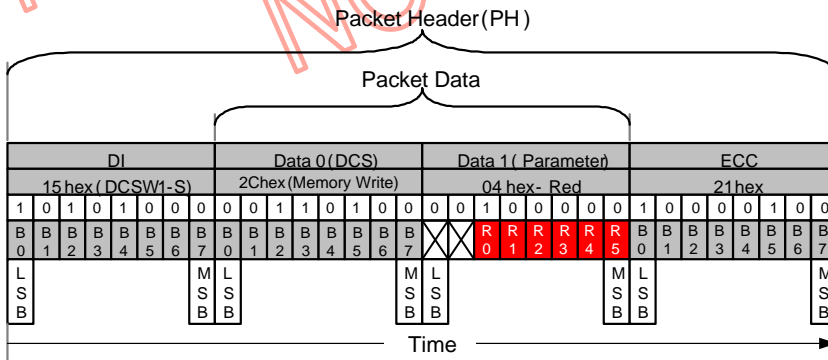
Example3: Green sub-pixel write



Green Subpixel Write (DCSW1-S)

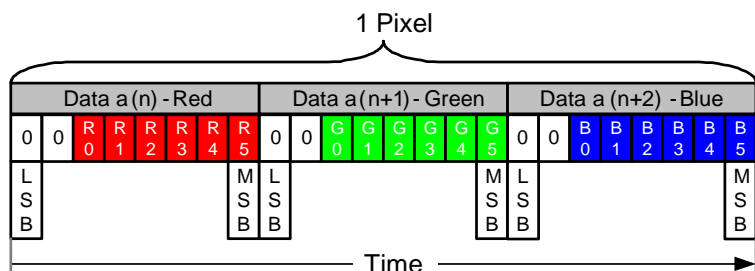
Note: DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)

Example4: Red sub-pixel write

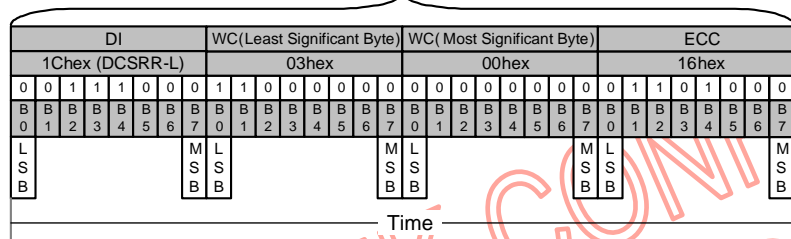
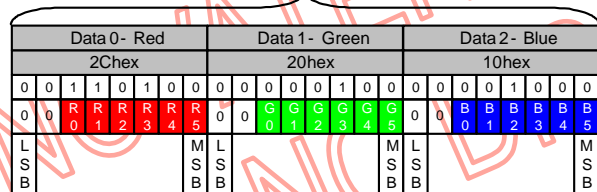
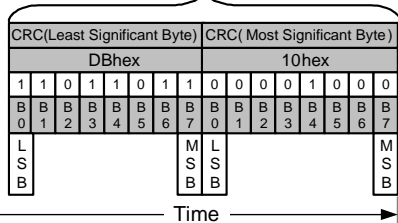


Red Subpixel Write (DCSW1-S)

Note: DCS (Data 0) can also be "Memory Write Continue" (3Ch) command

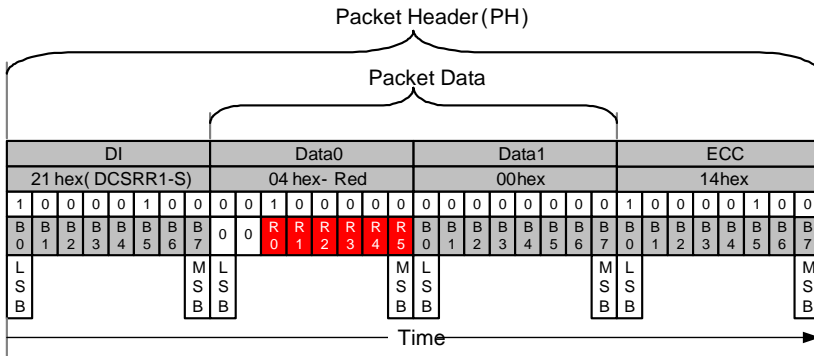
18 bits/pixel Reading

One Pixel Bit and Color Read Orders

The display module can send to the MCU following packets after the MCU has sent a read command "Memory Read (2Eh)" or "Memory Read Continue (3Eh)".

Packet Header (PH)

Packet Data (PD)

Packet Footer (PF)

One Pixel Read Response (DCSRR-L)

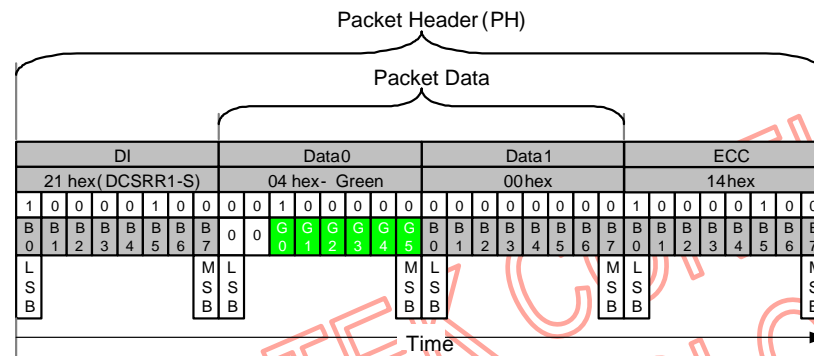
Note: It is possible that one pixel information is split in two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)



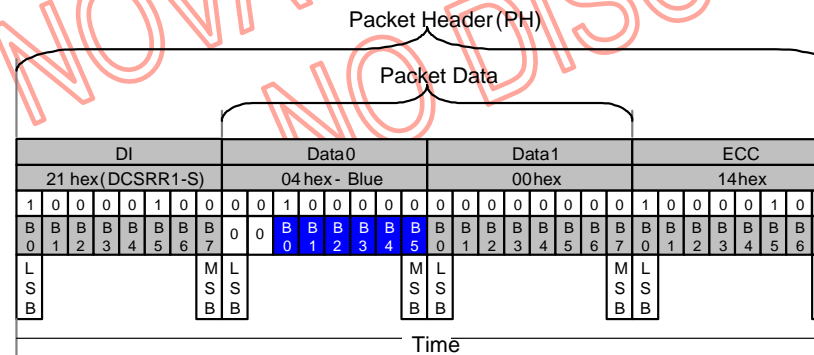
Red Subpixel Response (DCSRR1-S)

Note: Data 1 is always 00h



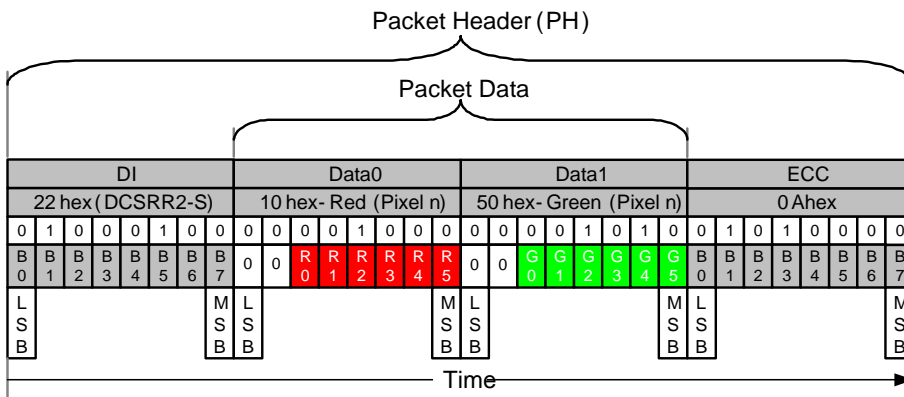
Green Subpixel Response (DCSRR1-S)

Note: Data 1 is always 00h

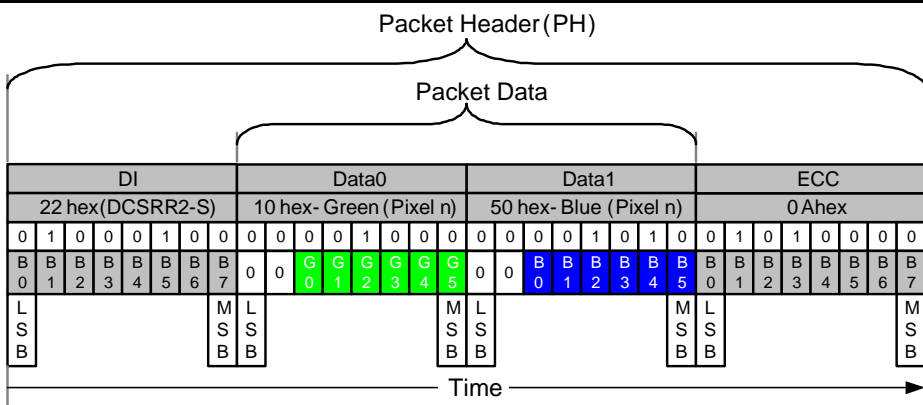
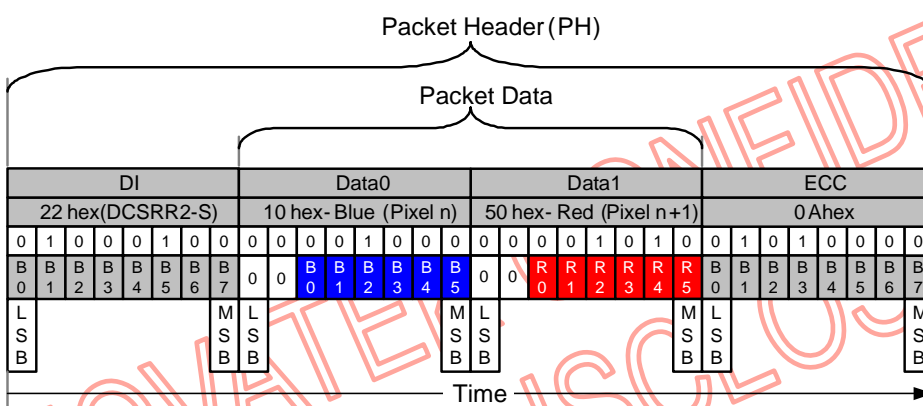


Blue Subpixel Response (DCSRR1-S)

Note: Data 1 is always 00h



Red and Green Subpixels Response (DCSRR2-S)


Green and Blue Subpixels Response (DCSRR2-S)

Blue and Red Subpixels Response (DCSRR2-S)

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5.8 Window Address Function

The window address function allows writing RAM data consecutively within the window address area which are determined by setting the horizontal address register (XSA and XEA) and vertical address register (YSA and YEA). The MV, MX and MY bit determine the transition direction of the RAM address (refer to register 36h).

The RAM address (XAD[8:0], YAD[8:0]) must be set within the window address area, and the window address must be made within the GRAM address map area.

For 360RGB x 480 resolution:

[Window address area setting range]

(Horizontal direction) → $0000h \leq XSA \leq XEA \leq 013Fh$

(Vertical direction) → $0000h \leq YSA \leq YEA \leq 01DFh$

[RAM Address setting range]

(RAM address) → $XSA \leq XAD[8:0] \leq XEA$

$YSA \leq YAD[8:0] \leq YEA$

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5.9 Reduced Power Consumption Drive Settings

The NT35310 supports various methods for reducing power consumption. Generally speaking, a balance will need to be found between reduced power consumption and display quality. In addition, the power consumption also depends on the characteristics of the panel. Review the various methods to determine which one will provide the optimal balance between reduced power consumption and display quality.

Frame Rate Setting

The NT35310 is able to change the liquid crystal polarity inversion cycle by setting the RTN bit to change the frame frequency. Setting a lower frequency in the partial display operation will reduce power consumption. For more information, refer to "Frame-Frequency Adjustment Frequency."

5.10 Frame-Frequency Adjustment Function

The NT35310 provides a function to adjust the frame frequency for driving liquid crystal by setting the RTN bits without changing the oscillation frequency.

Changing the frame frequency is permissible when a moving picture or still picture is displayed on the screen; a high oscillation frequency should be set in this case. By changing the RTN settings, the NT35310 can function at a low frame frequency to display a still picture (reducing power consumption), and at a high frame frequency when displaying a moving picture (which requires data to be rewritten at high speed).

Relationship between Liquid Crystal Drive Duty and the Frame Frequency

The formula below is used to calculate the relationship between the liquid crystal drive duty and the frame frequency. The frame frequency is determined by setting the 1H period adjustment (RTN) bit.

Equation for calculating frame frequency

$$\text{FrameFrequency} = \frac{13\text{MHz} / 3 (\pm 5\%)}{\text{RTN} * (\text{Lines} + \text{BP} + \text{FP})} \text{Hz}$$

RTN: Number of clocks per line.

Line: Display Line Number

FP: Number of lines for front porch.

BP: Number of lines for back porch.

5.11 GAMMA Function

The structure of grayscale amplifier is shown as below. The 18 voltage levels between GVDDP/GVDDN and VGSP/VGSN determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.

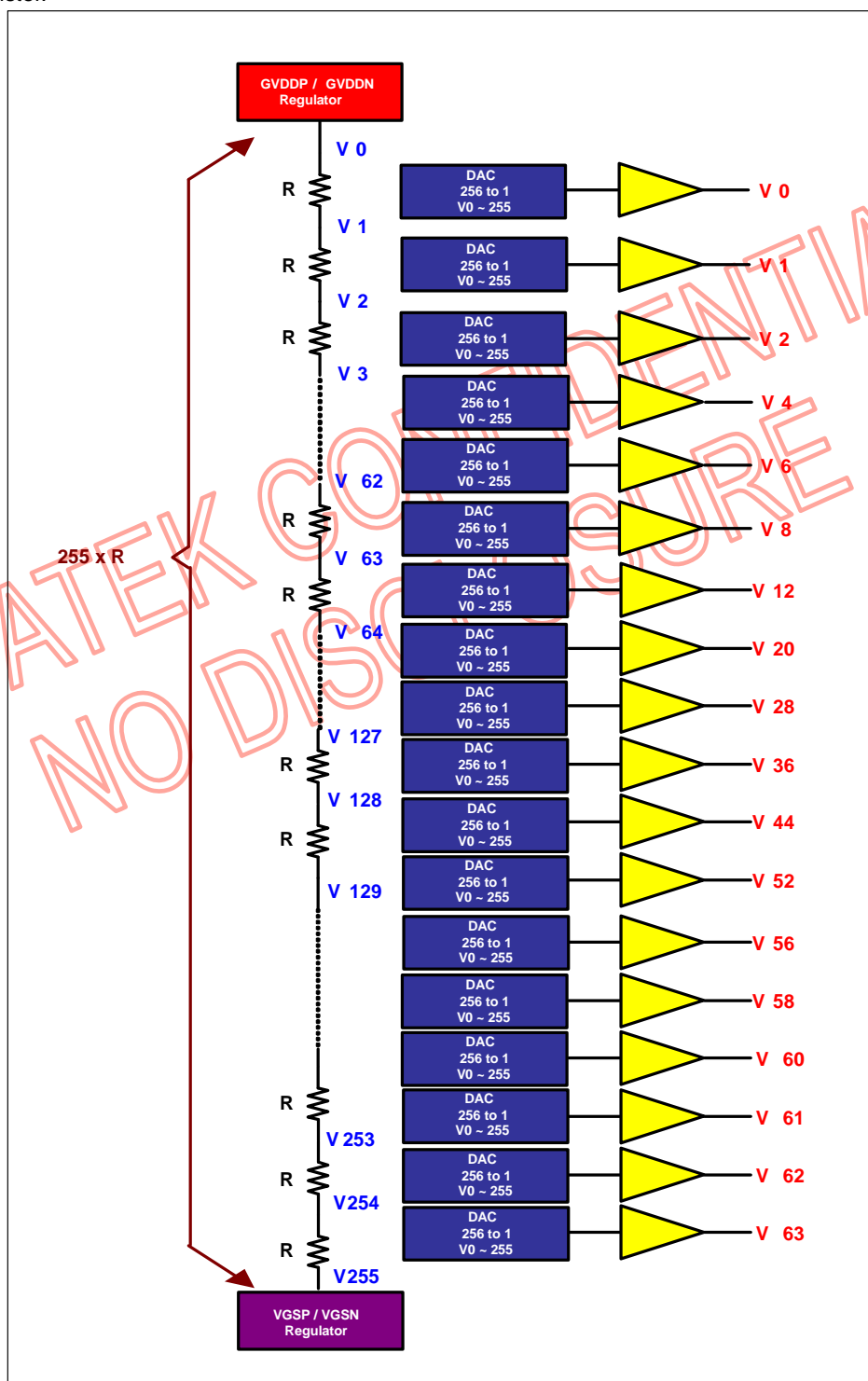


Figure 5.11.1 Gamma Architecture for NT35310

5.12 Reset Function

The RESET function of NT35310 is triggered by a RESX input. After reset function triggered, the NT35310 enter a reset period, and the duration of this period must be at least 1ms. During this period, the NT35310 and its power circuit is initialized. In the meanwhile, because the NT35310 will be in a busy state, neither instruction from MPU nor GRAM data access request are not acceptable. In addition, for power-on reset case, there will be a 20 ms period for oscillator to be stable. Therefore, any instructions or GRAM access request must be made after this 20 ms period is over.

Initial States of Output Pins.

The following table represent the output pins and its initial state

Output Pins	Initial State
Liquid crystal driver (Source driver output)	All output VSS
Liquid crystal driver (Gate driver output)	All output VSS
AVDD	VCI
AVEE	Disabled (VSS level output)
VCOM	Disabled (VSS level output)
GVDDP	Disabled (VSS level output)
GVDDN	Disabled (VSS level output)
VGH	VCI
VGL	VSS
VCL	VSS
VDD	VDD
VLPH	VDD
TE	Disabled (VSS level output)
SDO	Hi-Z
D17-0,SDI	Hi-Z

Initial States of Input / Output Pins

The following table represent the input/output pins and its initial state

Input/Output Pins	Initial State
C11P/M	Hi-Z
C12P/M	Hi-Z
C13P/M	Hi-Z
C21P/M	Hi-Z
C22P/M	Hi-Z

Note: The initial states of input/output pins listed above are proper under the condition that LCD module is connected as shown in the connection example.

Initial State of Instruction Set

The initial state of instruction set is listed in next chapter, and the default values are shown in the parenthesis of each instruction bit cell.

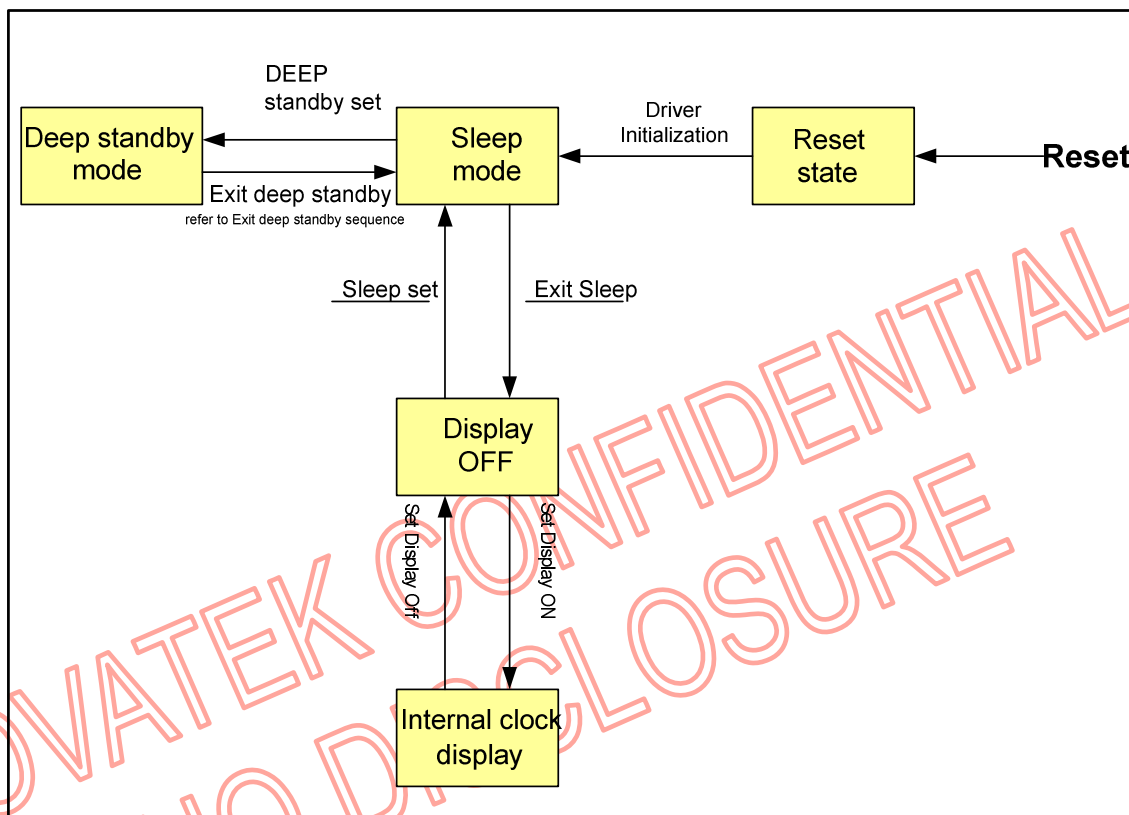
Initial State of RAM Data

The data in RAM is not automatically initialized in RESET period, and must be initialized by software before display-on instruction is made.

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5.13 Basic Operation Mode

The basic operation mode of NT35310 is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in the figure.


Figure 5.15.1

5.14 Power On/Off Sequence

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.

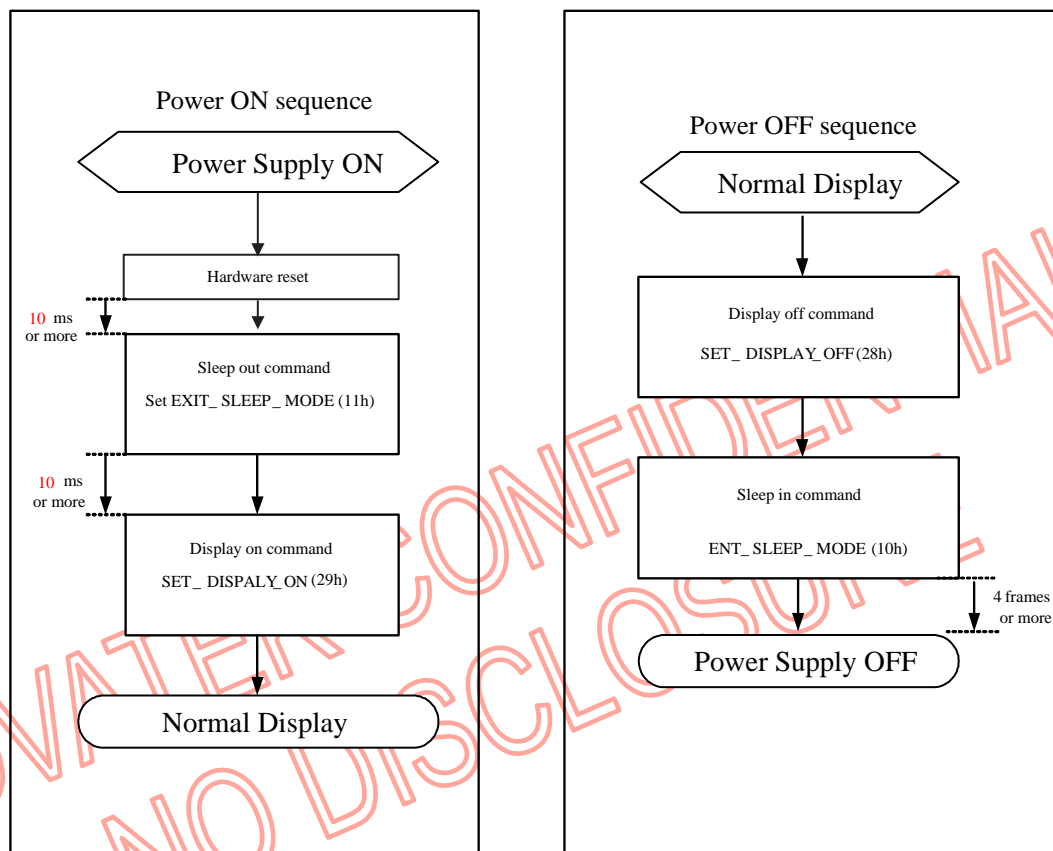


Figure 5.16.1 Power Supply Setting Sequence

5.15 Instruction Setting Sequence

When setting instruction to the NT35310, the sequences shown in below figures must be followed to complete the instruction setting.

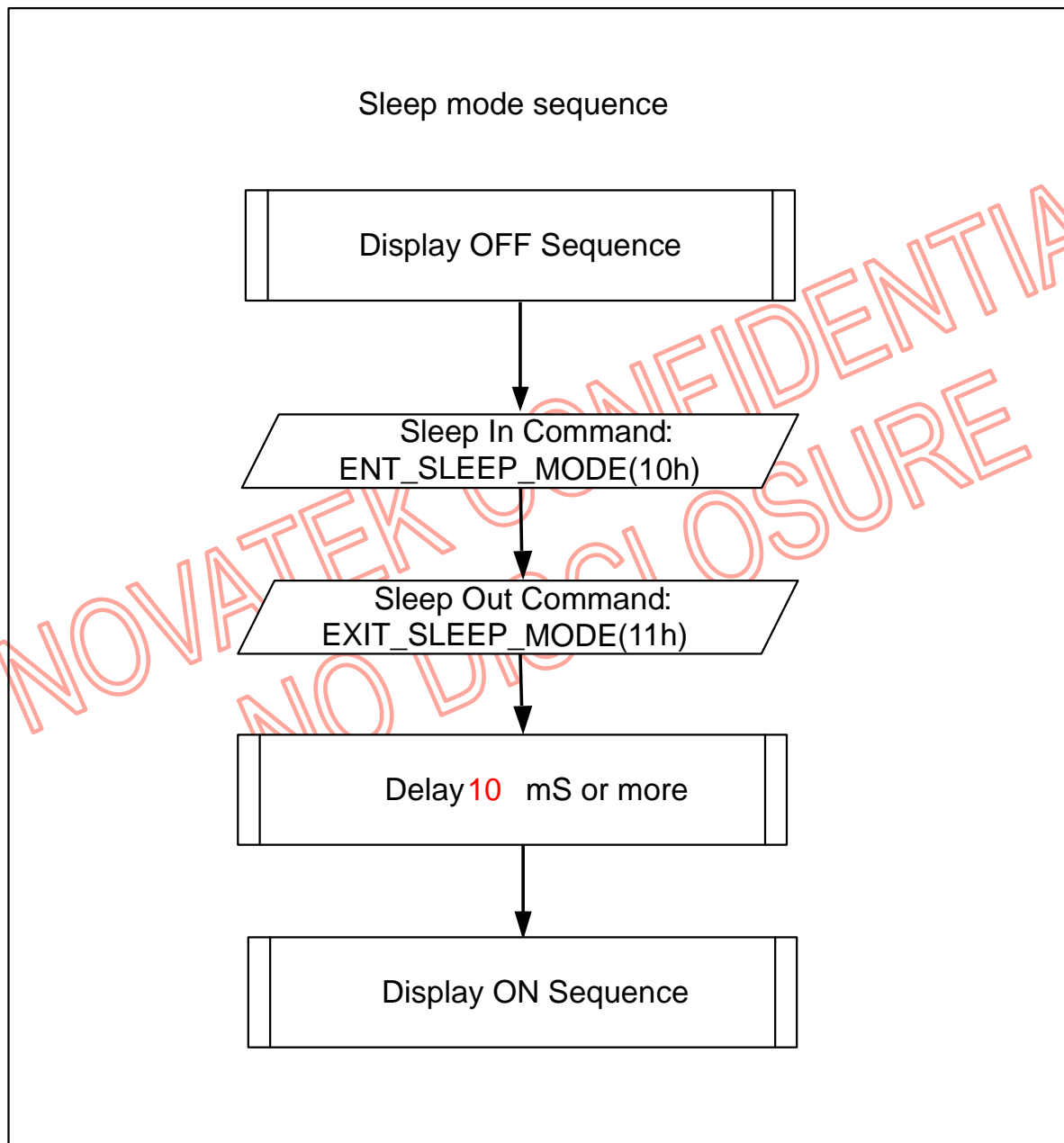
5.15.1 Sleep SET/EXIT Sequences


Figure 5.16.1 Sleep SET/EXIT Sequences

5.15.2 Deep Standby Mode ENTER/EXIT Sequences

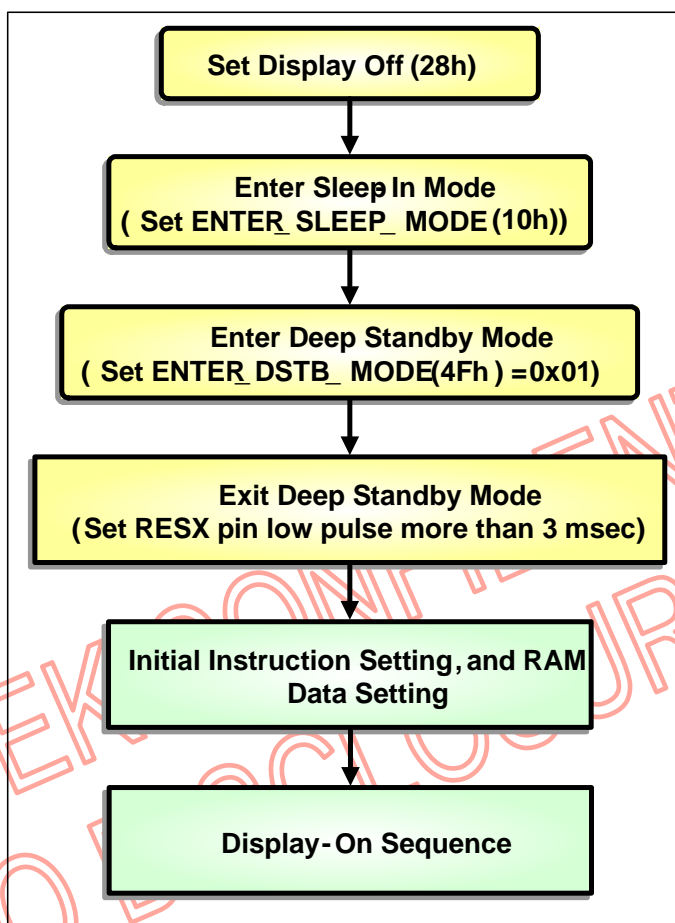


Figure 5.16.2 Deep Standby Mode ENTER/EXIT Sequences

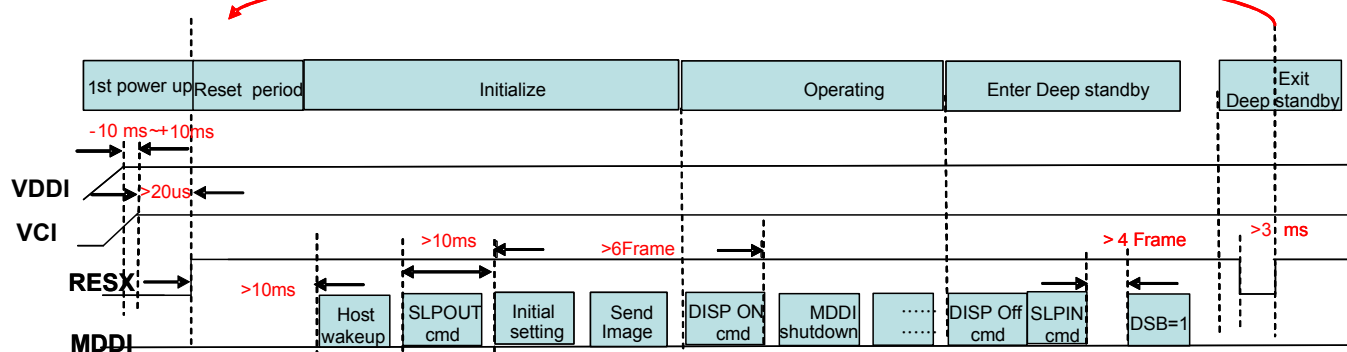


Figure 5.16.3 Enter/Exit Deep standby mode sequence.

5.16 MTP Write Sequence

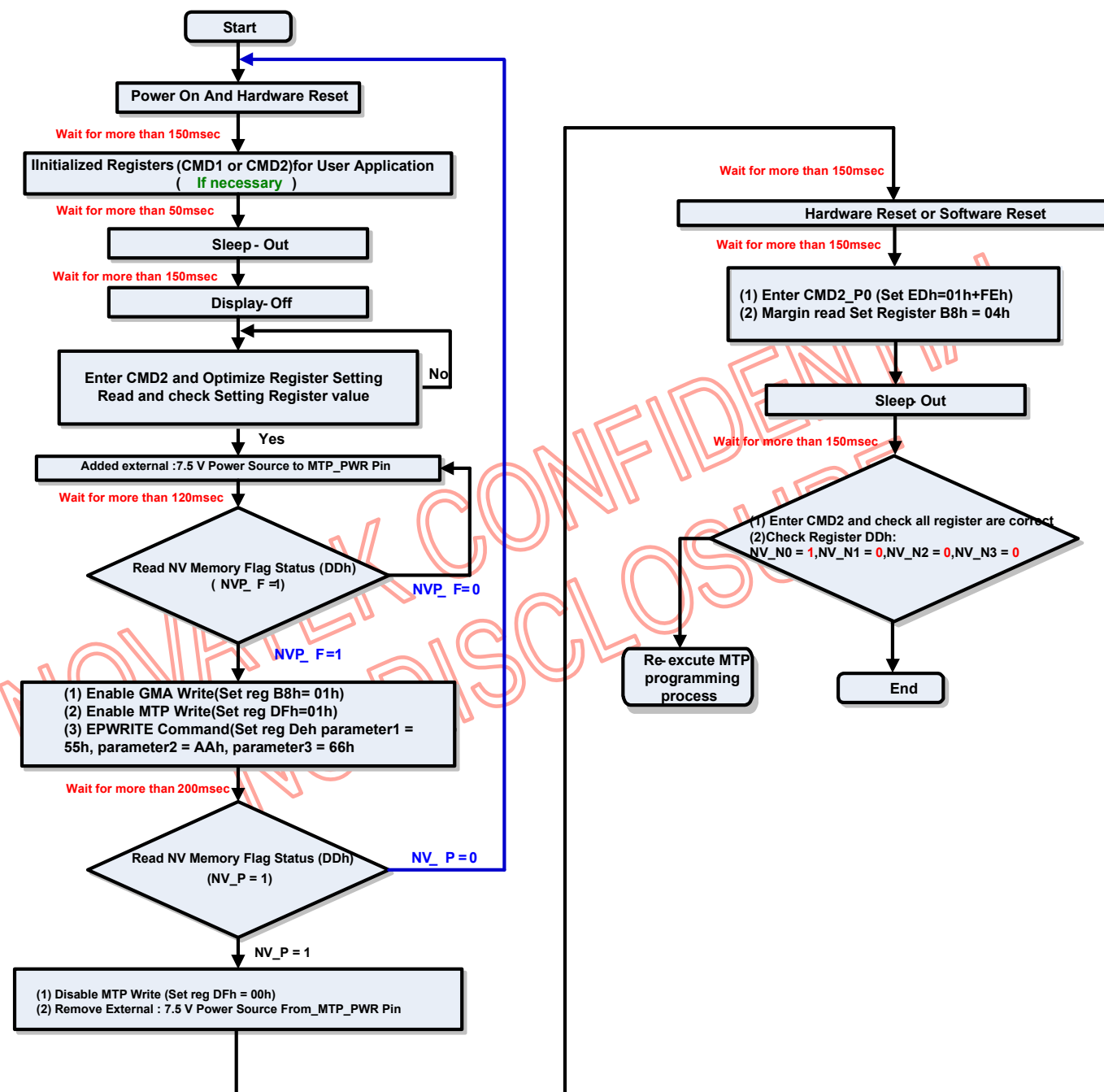
The NT35310 provides 1 time to store Power and gamma setting related register and DDB information. And 4 times MTP to store VCOM, ID1, ID2 and ID3 information. The table 5.18.1 shows what register setting could be stored in MTP for each MTP programming procedures.

Table 5.18.1 MTP Stored Contents

MTP Programming	MTP Storage Contents for Each Time MTP Programming
First Time MTP Programming	GAMMA,CABC,VCOM,ID1, ID2 and ID3,WRDDB,POWER_Control
Second Time MTP Programming	VCOM,ID1, ID2 and ID3,WRDDB,POWER_Control
Third Time MTP Programming	VCOM,ID1, ID2 and ID3,WRDDB
Forth Time MTP Programming	VCOM,ID1, ID2 and ID3,WRDDB

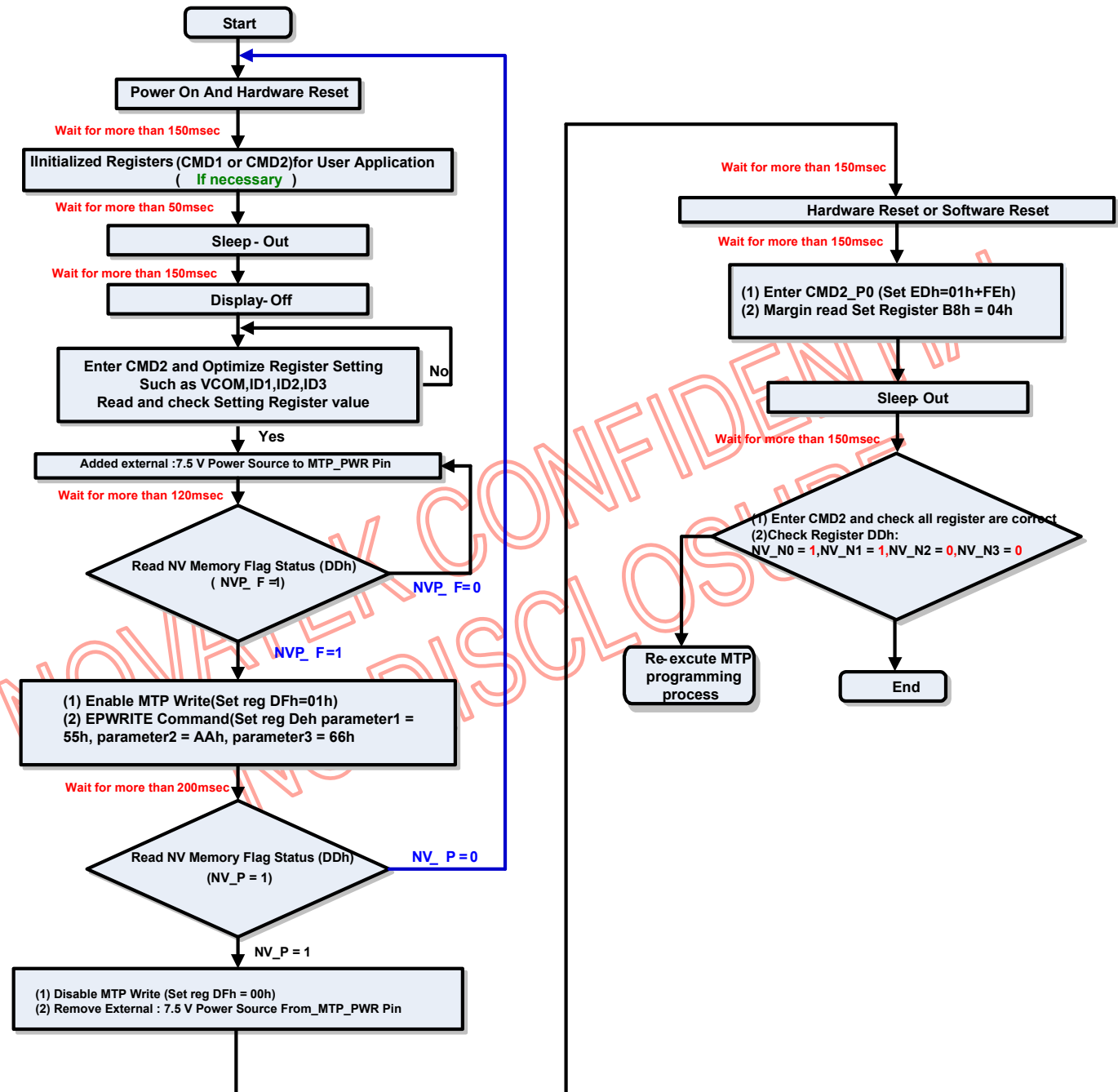
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5.16.1 First Time MTP Programming Sequence (for all MTP)

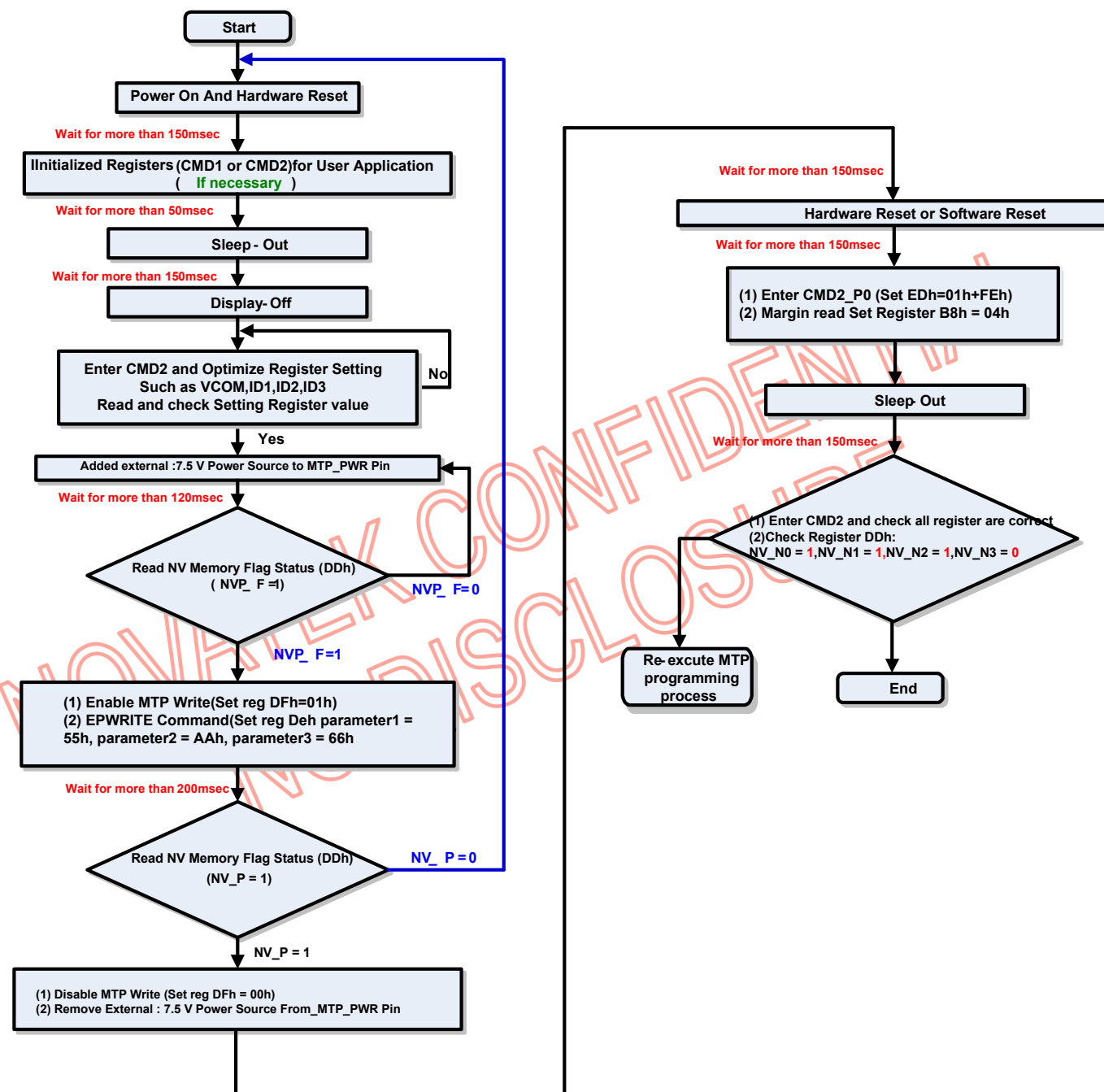


Note1: During this step, user have to ensure that all registers are optimal for display, because most registers “only” have one MTP programming chances.

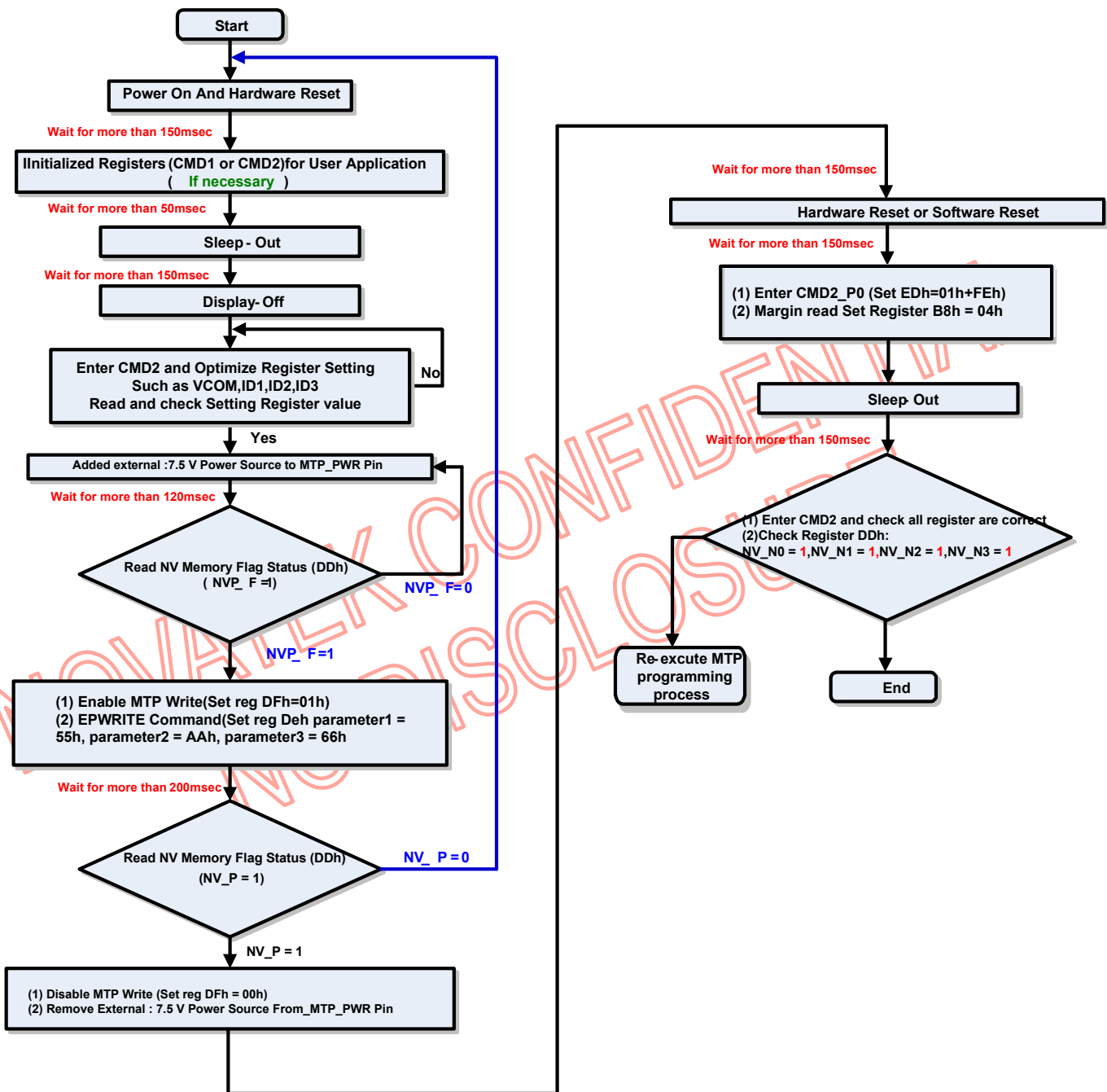
Note2: MTP GAMMA, please set B8h=01h before MTP Write.

5.16.2 Second Time MTP Programming Sequence


5.16.3 Third Time MTP Programming Sequence (Only for VCOM, ID and WRDDB)

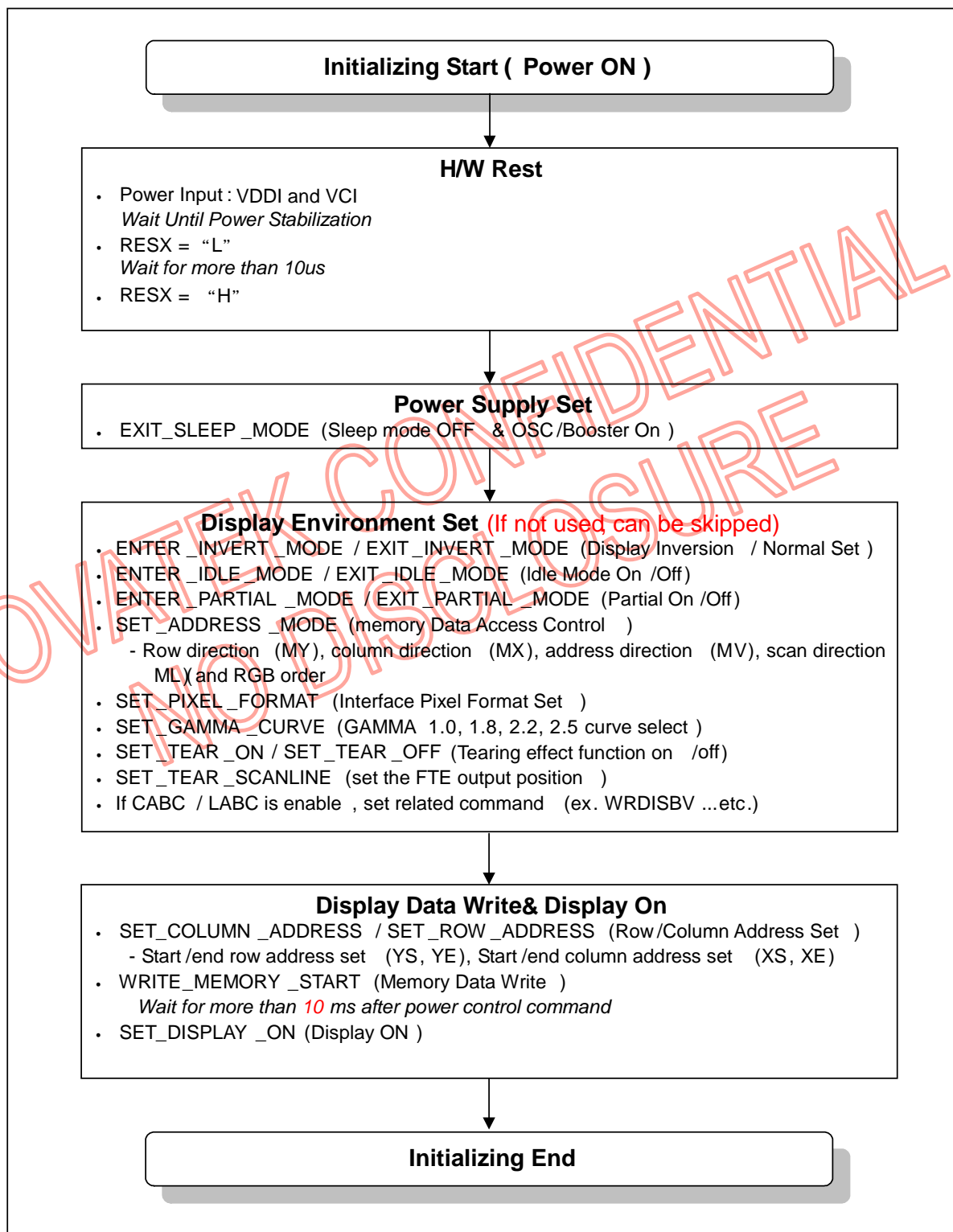


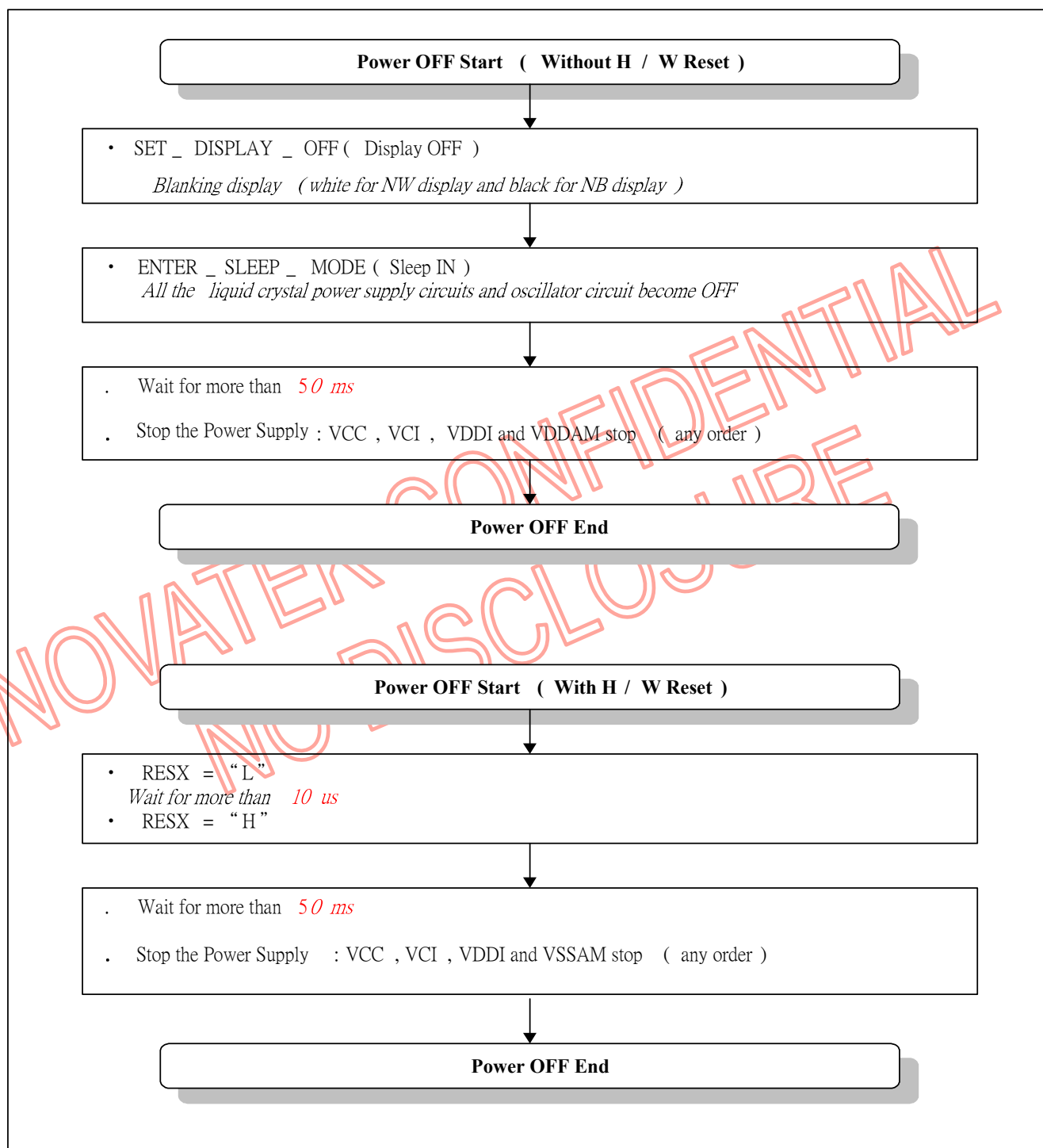
5.16.4 Fourth Time MTP Programming Sequence (Only for VCOM, ID and WRDDB)



5.17 Instruction Setup Flow

5.17.1 Initializing with the Build-in Power Supply Circuit



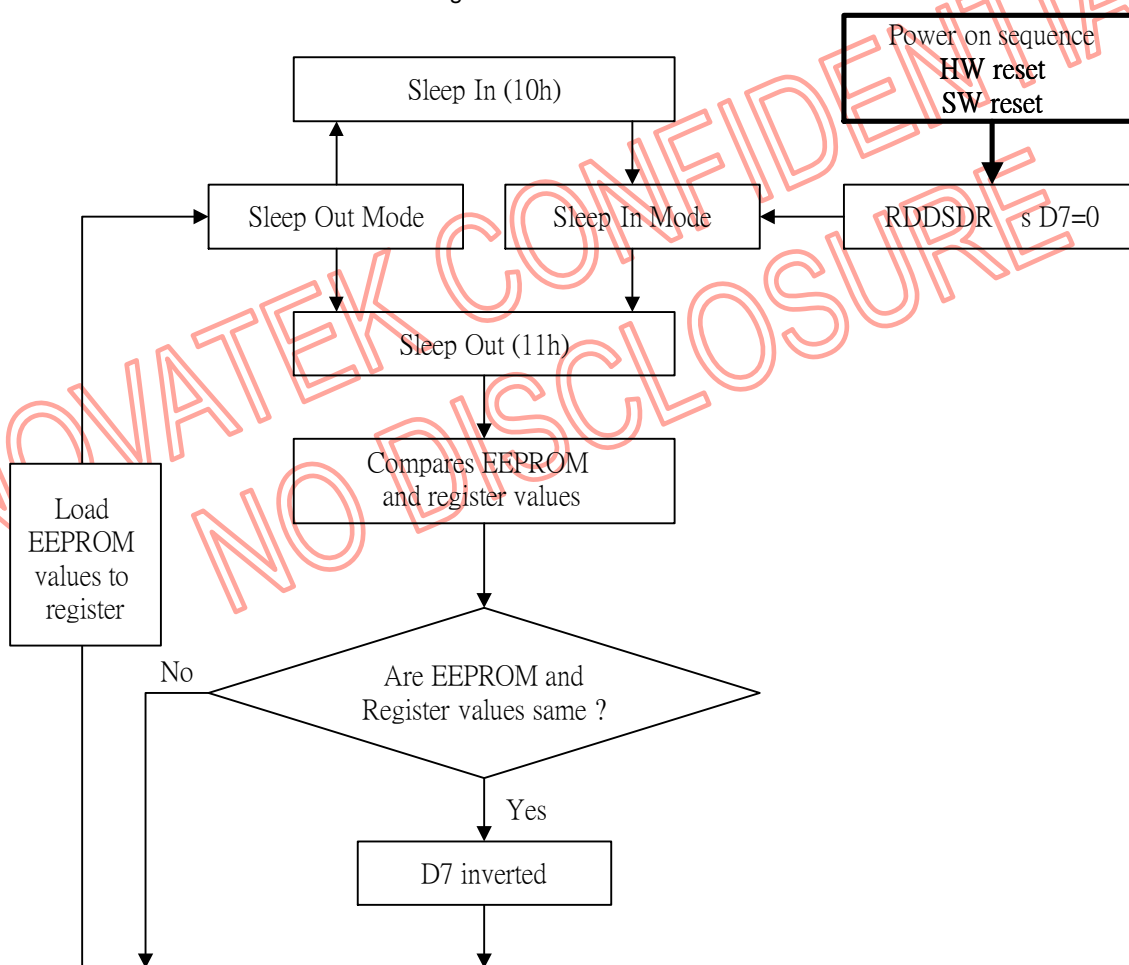
5.17.2 Power Off Sequence


5.18 SLEEP OUT-COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE
5.18.1 Register loading Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



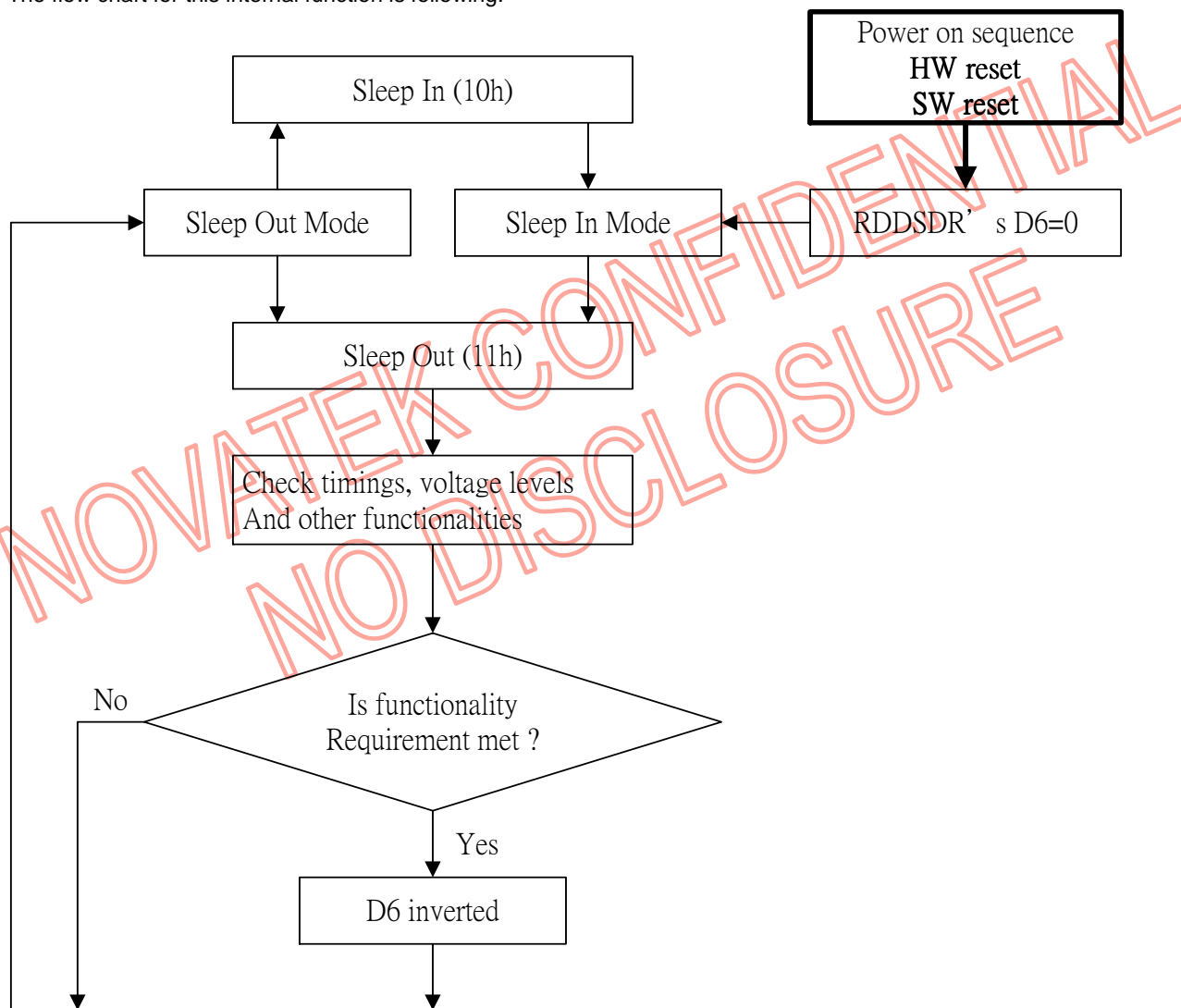
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

5.20.2 Functionality Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

6. Command Descriptions

For intergrating 2 High Speed Serial Interface, MIPI [8bits format] and MDDI [16Bits format], an algorithm of register mapping is implemented in NT35310. As for MIPI interface, the main difference for host to access these 2 groups of command sets is the Data type of the packets. The address mapping of registers for these 2 command sets is summarized as table below:

User Command Set (CMD1)					
Command Table	MIPI / CPU / SPI Interface			MDDI	
	MIPI Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	DCS WRT, No Parameter	Address	XXh	Address	XX00h
XXh + 1 Parameter	DCS WRT, 1 Parameter	Address	XXh	Address	XX00h
		Parameter	PA1h	Parameter	PA1h
XXh + 2 Parameters	DCS LONG WRT with 2 Parameters	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
				Parameter 2	PA2h
XXh + n Parameters (n > 2)	DCS LONG WRT with n Parameters	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
		Parameter 3	PA3h	Parameter2	PA2h
		Parameter 4	PA4h	Address	XX02h
		:	:	Parameter3	PA3h
		Parameter n-th	PAnh	Address	XX03h
				Parameter4	PA4h
				:	:
				Address	XXXnh
		Parameter n	PAnh		
CMD2 Unlock	DCS WRT, 1 Parameter	Address	EDh	Address	ED00h
		Parameter	01h	Parameter	0001h
		Parameter	FEh	Address	ED01h
				Parameter	00FEh

Manufacture Command Set (Register of CMD2)					
Command Table	MIPI / CPU / SPI Interface			MDDI	
	MIPI Type	Address	8-bits	Address	16-bits
		Parameter	8-bits	Parameter	16-bits
XXh	Generic Short Write	Address	XXh	Address	XX00h
XXh + 1 Parameter	Generic Short Write, 1 Parameter	Address	XXh	Address	XX00h
		Parameter	PA1h	Parameter	PA1h
XXh + 2 Parameters	Generic Short Write, 2 Parameter	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
				Parameter 2	PA2h
XXh + n Parameters (n > 2)	Generic Long Write n Parameters	Address	XXh	Address	XX00h
		Parameter 1	PA1h	Parameter 1	PA1h
		Parameter 2	PA2h	Address	XX01h
		Parameter 3	PA3h	Parameter2	PA2h
		Parameter 4	PA4h	Address	XX02h
		:	:	Parameter3	PA3h
		Parameter n-th	PAnh	Address	XX03h
				Parameter4	PA4h
				:	:
				:	:
				Address	XXXnh
		Parameter n	PAnh		

6.1 User Command Set (Command 1)

Other Interface		MDDI I/F Address	Instruction	MDDI D[15 : 8]	D7	D6	D5	D4	D3	D2	D1	D0	MTP	CTS		
CMD	Parameter													0	1	
00h	-	0000h	NOP		No Argument										O	O
01h	-	0100h	SOFT_REST		No Argument										O	O
04h	1 st Parameter	0400h	RDID1	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	O	O	NOP	
	2 nd Parameter	0401h	RDID2	00h	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	O	O	NOP	
	3 rd Parameter	0402h	RDID3	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	O	O	NOP	
05h	1 st Parameter	0500h	RDNUMED	00h	P7	P6	P5	P4	P3	P2	P1	P0		O	O	
0Ah	1 st Parameter	0A00h	GET_POWER_MODE	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
0Bh	1 st Parameter	0B00h	GET_ADDRESS_MODE	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
0Ch	1 st Parameter	0C00h	GET_PIXEL_FORMAT	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
0Dh	1 st Parameter	0D00h	GET_DISPLAY_MODE	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
0Eh	1 st Parameter	0E00h	GET_SIGNAL_MODE	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
0Fh	1 st Parameter	0F00h	RDDSDR	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
10h	-	1000h	ENTER_SLEEP_MODE		No Argument										O	O
11h	-	1100h	EXIT_SLEEP_MODE		No Argument										O	O
12h	-	1200h	ENTER_PARTIAL_MODE		No Argument										O	O
13h	-	1300h	ENTER_NORMAL_MODE		No Argument										O	O
20h	-	2000h	EXIT_INVERT_MODE		No Argument										O	NOP
21h	-	2100h	ENTER_INVERT_MODE		No Argument										O	NOP
22h	-	2200h	ALLPOFF		No Argument										O	O
23h	-	2300h	ALLPON		No Argument										O	O
26h	1 st Parameter	2600h	GAMSET		GC[7:0]										O	O
28h	-	2800h	SET_DISPLAY_OFF		No Argument										O	O
29h	-	2900h	SET_DISPLAY_ON		No Argument										O	O
2Ah	1 st Parameter	2A00h	SET_HORIZONTAL_ADDRESS	00h	0	0	0	0	0	0	0	XSA8		O	O	
	2 nd Parameter	2A01h		00h	XSA7	XSA6	XSA5	XSA4	XSA3	XSA2	XSA1	XSA0		O	O	
	3 rd Parameter	2A02h		00h	0	0	0	0	0	0	0	XEA8		O	O	
	4 th Parameter	2A03h		00h	XEA7	XEA6	XEA5	XEA4	XEA3	XEA2	XEA1	XEA0		O	O	
2Bh	1 st Parameter	2B00h	SET_VERTICAL_ADDRESS	00h	0	0	0	0	0	0	0	YSA8		O	O	
	2 nd Parameter	2B01h		00h	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0		O	O	
	3 rd Parameter	2B02h		00h	0	0	0	0	0	0	0	YEA8		O	O	
	4 th Parameter	2B03h		00h	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0		O	O	
2Ch	-	2C00h	WRITE_MEMORY_START	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
2Dh	1 st Parameter	2D00h	SET_MDDI_RAM_READ_ADDRESS	00h	0	0	0	0	0	0	0	XAD8		O	NOP	
	2 nd Parameter	2D01h		00h	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0		O	NOP	
	3 rd Parameter	2D02h		00h	0	0	0	0	0	0	0	YAD8		O	NOP	
	4 th Parameter	2D03h		00h	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0		O	NOP	
2Eh	-	2E00h	READ_MEMORY_START	00h	D7	D6	D5	D4	D3	D2	D1	D0		O	O	
30h	1 st Parameter	3000h	SET_PARTIAL_AREA	00h	0	0	0	0	0	0	0	PSL8		O	O	
	2 nd Parameter	3001h		00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		O	O	
	3 rd Parameter	3002h		00h	0	0	0	0	0	0	0	PEL8		O	O	
	4 th Parameter	3003h		00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		O	O	
33h	1 st Parameter	3300h	SCRLAR	00h	0	0	0	0	0	0	0	TFA8		O	NOP	
	2 nd Parameter	3301h		00h	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		O	NOP	
	3 rd Parameter	3302h		00h	0	0	0	0	0	0	0	VSA8		O	NOP	
	4 th Parameter	3303h		00h	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		O	NOP	
	5 th Parameter	3304h		00h	0	0	0	0	0	0	0	BFA8		O	NOP	
	6 th Parameter	3305h		00h	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		O	NOP	
34h	-	3400h	SET_TEAR_OFF		No Argument										O	O
35h	1 st Parameter	3500h	SET_TEAR_ON	00h	TEW3	TEW2	TEW1	TEW0	0	0	TEP	M		O	O	
36h	1 st Parameter	3600h	SET_ADDRESS_MODE	00h	MY	MX	MV	ML	RGB	MH	0	0		O	O	
37h	1 st Parameter	3700h	VSCSAD	00h	0	0	0	0	0	0	0	SSA8		O	NOP	
	2 nd Parameter	3701h		00h	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		O	NOP	
38h	-	3800h	EXIT_IDLE_MODE		No Argument										O	O

Other Interface		MDDI I/F Address	Instruction	MDDI D[15 : 8]	D7	D6	D5	D4	D3	D2	D1	D0	MTP	CTS			
CMD	Parameter													0	1		
39h	-	3900h	ENTER_IDLE_MODE		No Argument											O	O
3Ah	1 st Parameter	3A00h	SET_PIXEL_FORMAT	00h	0	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0			O	O	
3Bh	1 st Parameter	3B00h	RGBCTRL	00h	0	CRCM	0	0	DP	EP	HSP	VSP			O	NOP	
	2 nd Parameter	3B01h	RGBPRCTR	00h	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0			O	NOP	
	3 rd Parameter	3B02h	RGBPRCTR	00h	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0			O	NOP	
	4 th Parameter	3B03h	RGBPRCTR	00h	0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0			O	NOP	
	5 th Parameter	3B04h	RGBPRCTR	00h	0	HFP6	HFP5	HFP4	HFP3	HFP2	HFP1	HFP0			O	NOP	
3Ch	-	3C00h	RAMWRC	00h	D7	D6	D5	D4	D3	D2	D1	D0			O	O	
3Eh	-	3E00h	RAMRDC	00h	D7	D6	D5	D4	D3	D2	D1	D0			O	O	
44h	1 st Parameter	4400h	SET_TEAR_SCANLINE	00h	0	0	0	0	0	0	0	N8			O	O	
	2 nd Parameter	4401h		00h	N7	N6	N5	N4	N3	N2	N1	N0			O	O	
45h	1 st Parameter	4500h	RDSCL	00h	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8			O	O	
	2 nd Parameter	4501h		00h	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0			O	O	
4Fh	1 st Parameter	4F00h	ENTER_DSTB_MODE	00h	0	0	0	0	0	0	0	DSTB			O	NOP	
51h	1 st Parameter	5100h	WRDISBV	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0			O	O	
52h	1 st Parameter	5200h	RDDISBV	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0			O	O	
53h	1 st Parameter	5300h	WRCTRLD	00h	0	0	BCTRL	0	DD	BL	0	0			O	O	
54h	1 st Parameter	5400h	RDCTRLD	00h	0	0	BCTRL	0	DD	BL	0	0			O	O	
55h	1 st parameter	5500h	WRCABC	00h	IMAGE_ENHANCEMENT [3:0]			0	0	CABC_COND [1:0]					O	O	
56h	1 st parameter	5600h	RDCABC	00h	IMAGE_ENHANCEMENT [3:0]			0	0	CABC_COND [1:0]					O	O	
5Eh	1 st Parameter	5E00h	WRCABCMB	00h	CMB[7 : 0]											O	O
5Fh	1 st Parameter	5F00h	RDCABCMB	00h	CMB[7 : 0]											O	O
68h	1 st Parameter	6800h	RDDSDR	00h	D7	D6	D5	D4	D3	D2	D1	D0			O	O	
8Fh	1st Parameter	8F00h	SET_MIPI_MDDI	00h	0	0	0	0	0	0	0	MDDI_I	O		O	NOP	
A1h	1st Parameter	A100h	RDDDBS	00h	SID[7 : 0]: LS Byte of Supplier ID											O	O
	2nd Parameter	A101h		00h	SID[15 : 8]: MS Byte of Supplier ID											O	O
	3rd Parameter	A102h		00h	MRID[7 : 0]: LS Byte of Model Number ID											O	O
	4th Parameter	A103h		00h	MRID[15 : 8]: MS Byte of Model Number ID											O	O
	5th Parameter	A104h		00h	1	1	1	1	1	1	1	1	1	1			O
A8h	1st Parameter	A800h	RDDDDB	00h	SID[7 : 0]: LS Byte of Supplier ID											O	O
	2nd Parameter	A801h		00h	SID[15 : 8]: MS Byte of Supplier ID											O	O
	3rd Parameter	A802h		00h	MRID[7 : 0]: LS Byte of Model Number ID											O	O
	4th Parameter	A803h		00h	MRID[15 : 8]: MS Byte of Model Number ID											O	O
	5th Parameter	A804h		00h	1	1	1	1	1	1	1	1	1	1			O
AAh	1st Parameter	AA00h	RDFCS	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0			O	O	
Aeh	1st Parameter	AE00h	STB_EDGE_TIMING_CTRL	00h	STB_EDGE_SEL[7:0]											O	O
AFh	1st Parameter	AF00h	RDCCS	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0			O	O	
DAh	1st Parameter	DA00h	RDID1	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10			O	O	
DBh	1st Parameter	DB00h	RDID2	00h	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20			O	O	
DCh	1st Parameter	DC00h	RDID3	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30			O	O	
E1h	1st Parameter	E100h	IDLEMODE_BL_Control	00h	0	0	0	0	0	0	IDLE_O N_SIGN AL_EN	IDLE_MO DE_BL_E N			O	O	
E2h	1st Parameter	E200h	IDLEMODE_BL_Control	00h	0	0	0	0	0	0	IDLE_O N_SIGN AL_EN	IDLE_MO DE_BL_E N			O	O	
FFh	1st Parameter	-	RD_CMDSTATUS	00h	0	0	0	0	0	CMD2_ P1	CMD2_ P0	CMD1			O	O	
EDh	1st Parameter	ED00h	CMD2UNLOCK	00h	0	0	0	0	0	0	0	1			O	O	
	2nd Parameter	ED01h		00h	1	1	1	1	1	1	1	1	0			O	O

Note: CTS bits is located at CMD2 register(B7h bit[3]).

NOP (00h): No Operation

Address (MDDI I/F)		0000h					Access Attribute			W
Address (Other I/F)		00h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	No Argument									N/A

Description	- This command performs no operation and is ignored by the device.									
Restriction	-									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Partial Mode On, Idle Mode Off, Sleep Out					Yes				
	Partial Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In					Yes				
Default Value	N/A									

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SOFT_RESET (01h): Software Reset

Address (MDDI I/F)		0100h					Access Attribute			W
Address (Other I/F)		01h					Number of Parameter(s)			N/A
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	No Argument									N/A

Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their SW Reset register values and all source & gate outputs are set to GND (display off).												
Restriction	(1) It will be necessary to wait 20msec before sending new command following software reset. (2) The display module loads all display supplier's factory default values to the registers during 5 msec. (3) If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120 msec before sending Sleep Out command. (4) Software Reset command cannot be sent during Sleep Out sequence.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	N/A												

RDID (04h): Read Display ID

Address (MDDI I/F)		0400h					Access Attribute				R
Address (Other I/F)		04h					Number of Parameter(s) via MIPI I/F				1
MDDI I/F	Other I/F	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
0400h	Parameter 1	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	N/A
0401h	Parameter 2	00h	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	N/A
0402h	Parameter 3	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	N/A

Description	<p>- This read byte returns display identification information.</p> <p>The 1st parameter (ID17 to ID10) : LCD module's manufacturer ID. The 2nd parameter (ID26 to ID20) : LCD module/driver version ID.</p> <p>It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:</p> <table border="1"> <thead> <tr> <th>ID Byte Value</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td>Version1</td> <td>:</td> </tr> <tr> <td>81h</td> <td>Version2</td> <td>:</td> </tr> <tr> <td>82h</td> <td>Version3</td> <td>:</td> </tr> </tbody> </table> <p>The 3rd parameter (ID37 to ID30) : LCD module/driver ID.</p>		ID Byte Value	Version	Changes	80h	Version1	:	81h	Version2	:	82h	Version3	:
	ID Byte Value	Version	Changes											
80h	Version1	:												
81h	Version2	:												
82h	Version3	:												
Restriction	-													
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Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													

RDNUMED (05h): Read Number of the Errors on DSI

Address (MDDI I/F)	0500h						Access Attribute			R
Address (Other I/F)	05h						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description	<p>- The first parameter is telling a number of the errors on DSI. The more detailed description of the bit is explained in below. D[6 : 0] bits are telling a number of the errors. D[7] is set to '1' if there is overflow with P[6 : 0] bits. D[7 : 0] bits are set to '0's (as well as GET_SIGNAL_MODE (0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed).</p> <p>Please also refer to the sections: "Acknowledge with Error Report (AwER)" and "Read Display Signal Mode (0Eh)".</p>												
Restriction	-												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

GET_POWER_MODE (0Ah): Read Display Power Mode

Address (MDDI I/F)	0A00h						Access Attribute			R
Address (Other I/F)	0Ah						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	0	0	08h

Description	- This command indicates the current status of the display as described in the table below:																											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Booster Voltage Status</td> <td>"1"=Booster on, "0"=Booster off</td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td>"1" = Idle Mode On, "0"= Idle Mode Off</td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td>"1" = Partial Mode On, "0" = Partial Mode Off</td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td>"1" = Sleep Out, "0" = Sleep In</td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td>"1" = Normal Display On, "0" = Normal Display Off</td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td>"1" = Display On, "0" = Display Off</td> </tr> <tr> <td>D1</td> <td>Not Used</td> <td>"0"</td> </tr> <tr> <td>D0</td> <td>Not Used</td> <td>"0"</td> </tr> </tbody> </table>	Bit	Description	Value	D7	Booster Voltage Status	"1"=Booster on, "0"=Booster off	D6	Idle Mode On/Off	"1" = Idle Mode On, "0"= Idle Mode Off	D5	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off	D4	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In	D3	Display Normal Mode On/Off	"1" = Normal Display On, "0" = Normal Display Off	D2	Display On/Off	"1" = Display On, "0" = Display Off	D1	Not Used	"0"	D0	Not Used	"0"
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GET_ADDRESS_MODE (0Bh): Get the Frame Memory to the Display Panel Read Order

Address (MDDI I/F)	0B00h						Access Attribute			R
Address (Other I/F)	0Bh						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	0	0	00h

Description	- This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Row Address Order (MY) "1"=Decrement (MY = 1) "0"=Increment (MY = 0)
	D6	Column Address Order (MX) "1"=Decrement (MX = 1) "0"=Increment (MX = 0)
	D5	Row/Column Order (MV) "1"= Row / column exchange (MV=1) "0"= Normal (MV=0)
	D4	Vertical fresh Order & Display change (ML) "1"=Decrement (ML = 1) "0"=Increment (ML = 0)
	D3	RGB/BGR Order "1"=BGR (register bit RGB of register 0x3600 is "1") "0"=RGB (register bit RGB of register 0x3600 is "0")
	D2	Horizontal fresh Order & Display change (MH) "1"=Decrement (MH = 1) "0"=Increment (MH = 0)
D1	Not Used "0"	
D0	Not Used "0"	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes	
Default Value	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

GET_PIXEL_MODE (0Ch): Read Input Pixel Format

Address (MDDI I/F)	0C00h						Access Attribute			R
Address (Other I/F)	0Ch						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	D1	D0	06h

Description	- This command indicates the current status of the display as described in the table below:																															
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GET_DISPLAY_MODE (0Dh): Read the Current Display Mode

Address (MDDI I/F)	0D00h						Access Attribute			R
Address (Other I/F)	0Dh						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description	- This command indicates the current status of the display as described in the table below:																																									
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Register Availability	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #2e4190; color: white;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																				
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H/W Reset	00h																																									

GET_SIGNAL_MODE (0Eh): Get Display Module Signaling Mode

Address (MDDI I/F)	0E00h						Access Attribute			R
Address (Other I/F)	0Eh						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description	- This command indicates the current status of the display as described in the table below:										
	Bit	Description					Value				
	D7	Frame Tearing Effect Line On/Off					"1" = On, "0" = Off				
	D6	Tearing Effect Line Output Mode					"1" = Mode B, "0" = Mode A				
	D5	Horizontal Sync. (RGB I/F)On/Off					"1" = On, "0" = Off				
	D4	Vertical Sync. (RGB I/F)On/Off					"1" = On, "0" = Off				
	D3	Pixel Clock (DCK, RGB I/F)On/Off					"1" = On, "0" = Off				
	D2	Data Enable (ENABLE, RGB I/F)On/Off					"1" = On, "0" = Off				
	D1	No used									
D0	Error on DSI					"1" = Error, "0" = NO Error					
Restriction	-										
Register Availability	Status					Availability					
	Normal Mode On, Idle Mode Off, Sleep Out					Yes					
	Normal Mode On, Idle Mode On, Sleep Out					Yes					
	Partial Mode On, Idle Mode Off, Sleep Out					Yes					
	Partial Mode On, Idle Mode On, Sleep Out					Yes					
	Sleep In					Yes					
Default Value	Status					Default Value					
	Power On Sequence					00h					
	S/W Reset					00h					
	H/W Reset					00h					

RDDSDR (0Fh): Read Display Self-Diagnostic Result

Address (MDDI I/F)	0F00h						Access Attribute			R
Address (Other I/F)	0Fh						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description	<p>-This command indicates the status of the display self-diagnostic results after Sleep Out. This command is described in the table below.</p> <p>-The inverse of checksum comparison will output to GPIO pin when select this function. Normally GPIO pin remains high, when ESD occurs leads to checksum comparison fail, it will output low pulse or keep low to notify the ESD alarm to host.</p>																																												
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th colspan="2">Value</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Register Loading Detection</td> <td colspan="2"></td> </tr> <tr> <td>D6</td> <td>Functionality Detection</td> <td colspan="2"></td> </tr> <tr> <td>D5</td> <td>Chip Attachment Detection</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D4</td> <td>Display Glass Break Detection</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D3</td> <td>Not Used</td> <td colspan="2">"0" (Not used)</td> </tr> <tr> <td>D2</td> <td>Not Used</td> <td colspan="2">"0" (Not used)</td> </tr> <tr> <td>D1</td> <td>Not Used</td> <td colspan="2">"0" (Not used)</td> </tr> <tr> <td>D0</td> <td>Checksums Compare</td> <td>"1"=Checksums are not same</td> <td>"0"=Checksums are same (Default)</td> </tr> </tbody> </table>										Bit	Description	Value		D7	Register Loading Detection			D6	Functionality Detection			D5	Chip Attachment Detection	"0" (Not used)		D4	Display Glass Break Detection	"0" (Not used)		D3	Not Used	"0" (Not used)		D2	Not Used	"0" (Not used)		D1	Not Used	"0" (Not used)		D0	Checksums Compare	"1"=Checksums are not same
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Restriction	- It will be necessary to wait 300ms after there is the last write access on DCS area registers before there can read Bit D0 value.																																												
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ENTER_SLEEP_MODE (10h): Enter the Sleep-In Mode

Address (MDDI I/F)		1000h					Access Attribute			W
Address (Other I/F)		10h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Sleep-In Mode

Description	<ul style="list-style-type: none"> - This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received. - In Sleep-in mode, the power of SRAM is default to keep SRAM power. It can be changed to turned off in order to reduce leakage current by DSIN bit in page 0 of CMD2, therefore the SRAM data will be lost in Sleep-in mode. Also either write or read SRAM is not possible in Sleep-in mode. 												
Restriction	- This command has no effect when the display module is already in Sleep Mode.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Status												
Power On Sequence	Sleep-In												
S/W Reset	Sleep-In												
H/W Reset	Sleep-In												

EXIT_SLEEP_MODE (11h): Exit the Sleep-In Mode

Address (MDDI I/F)		1100h					Access Attribute			W
Address (Other I/F)		11h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Sleep-In Mode

Description	- This command initiates the power-up sequence. The Sleep Out profile will be executed when this command is received. The Sleep Out will load register value. It will be necessary to wait 5 msec before sending next command.
--------------------	---

Restriction	- This command will not cause any visible effect on the display when the display is not in Sleep Mode.
--------------------	--

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	

Default Value	Status		Default Status	
	Power On Sequence		Sleep-In	
	S/W Reset		Sleep-In	
	H/W Reset		Sleep-In	

ENTER_PARTIAL_MODE (12h): Partial Display Mode On

Address (MDDI I/F)		1200h					Access Attribute			W
Address (Other I/F)		12h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Normal Mode

Description	<p>- This command sets the display mode to Partial Mode in which the display is refreshed using timing and image data based upon register settings and the Partial Display Memory contents, respectively.</p> <p>The Partial Mode profile will be executed when this command is received in the Sleep Out state. If in the Sleep-In state, the profile will not be executed until the device is placed into the Sleep-Out state.</p>													
Restriction	<p>- This command has no effect when Partial Display Mode is already active.</p> <p>- This command is not available in RGB interface.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Status</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Display Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Display Mode</td> </tr> </tbody> </table>		Status	Default Status	Power On Sequence	Normal Display Mode	S/W Reset	Normal Display Mode	H/W Reset	Normal Display Mode				
Status	Default Status													
Power On Sequence	Normal Display Mode													
S/W Reset	Normal Display Mode													
H/W Reset	Normal Display Mode													

ENTER_NORMAL_MODE (13h): Normal Display Mode On

Address (MDDI I/F)		1300h					Access Attribute			W
Address (Other I/F)		13h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Normal Mode

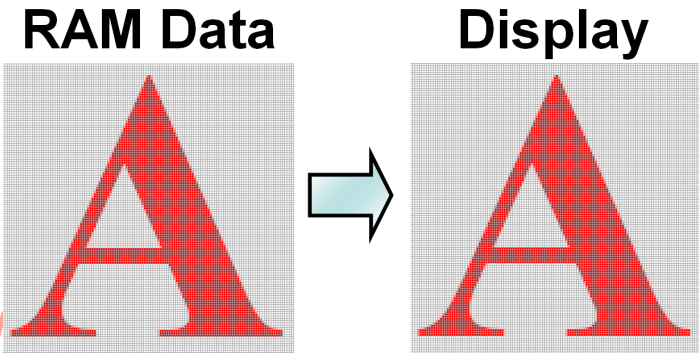
Description	- This command returns the display to normal mode. Normal Display Mode On means the Partial mode off, and the Scroll mode Off. Exit from NORON by the Partial mode On command (12h). There is no abnormal visual effect during the mode changes from Normal mode On to Partial mode On.
Restriction	- This command has no effect when Display Mode is already in Normal Display Mode.

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	

Default Value	Status		Default Status	
	Power On Sequence		Normal Display Mode	
	S/W Reset		Normal Display Mode	
	H/W Reset		Normal Display Mode	

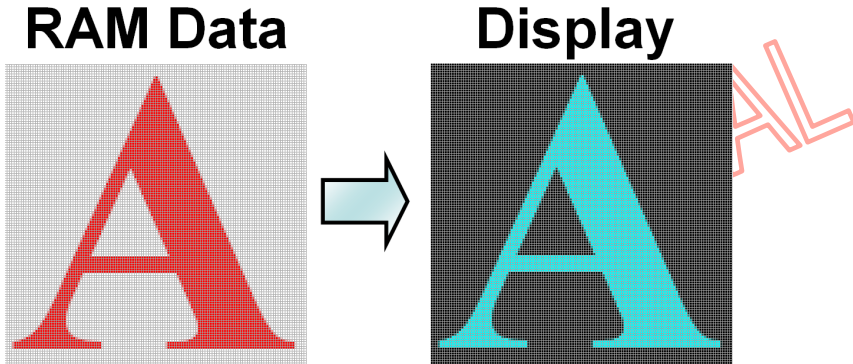
EXIT_INVERT_MODE (20h): Display Inversion Off

Address (MDDI I/F)		2000h					Access Attribute			W
Address (Other I/F)		20h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Inversion Off

Description	<p>- This command is used to recover from display reverse mode, makes no change of contents of frame memory, and does not change any other status. Example:</p> <div style="text-align: center;">  </div>												
Restriction	- This command has no effect when the module is already in inversion off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Status												
Power On Sequence	Display Inversion Off												
S/W Reset	Display Inversion Off												
H/W Reset	Display Inversion Off												

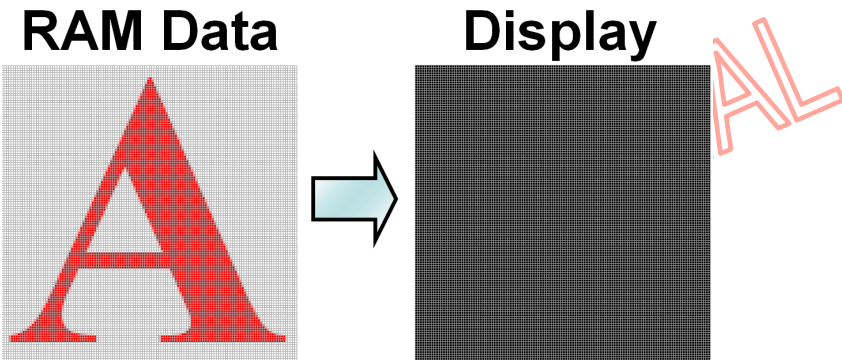
ENTER_INVERT_MODE (21h): Display Inversion On

Address (MDDI I/F)		2100h					Access Attribute			W
Address (Other I/F)		21h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Inversion Off

Description	<p>- This command is used to enter display Inversion mode, makes no change of contents of frame memory, and does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. Example:</p> <div style="text-align: center;">  </div>												
Restriction	- This command has no effect when the module is already in inversion off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Status												
Power On Sequence	Display Inversion Off												
S/W Reset	Display Inversion Off												
H/W Reset	Display Inversion Off												

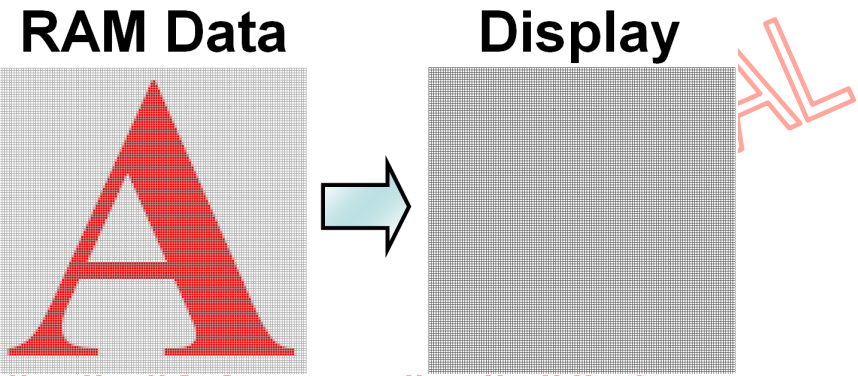
ALLPOFF (22h): All Pixel Off

Address (MDDI I/F)		2200h					Access Attribute			W
Address (Other I/F)		22h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Disable

Description	<p>- This command turns the display panel black in "Sleep Out" –mode and a status of the "Display On / Off": Register can be "on" or "off". This command makes no change of contents of frame memory. This command does not change any other status. Example:</p> <div style="text-align: center;">  </div> <p>"All Pixels On", "Normal Display Mode On" or "Partial Mode On" - commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display Mode On" and "Partial Mode On" - commands.</p>												
Restriction	- This command has no effect when module is already in all pixels off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default Value	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Default Status</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Disable</td> </tr> <tr> <td>S/W Reset</td> <td>Disable</td> </tr> <tr> <td>H/W Reset</td> <td>Disable</td> </tr> </tbody> </table>	Status	Default Status	Power On Sequence	Disable	S/W Reset	Disable	H/W Reset	Disable				
Status	Default Status												
Power On Sequence	Disable												
S/W Reset	Disable												
H/W Reset	Disable												

ALLPON (23h): All Pixel On

Address (MDDI I/F)		2300h					Access Attribute			W
Address (Other I/F)		23h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Disable

Description	<p>- This command turns the display panel white in "Sleep out"- mode and a status of the "Display On/Off". Register can be "on" or "off" This command makes no change of contents of frame memory. This command does not change any other status. Example:</p> <div style="text-align: center;">  </div> <p>"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" - commands are used to leave this mode. The display is showing the content of the frame memory after "Normal Display Mode On" and "Partial Mode On" - commands.</p>												
Restriction	- This command has no effect when module is already in all pixels on mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Default Status</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Disable</td> </tr> <tr> <td>S/W Reset</td> <td>Disable</td> </tr> <tr> <td>H/W Reset</td> <td>Disable</td> </tr> </tbody> </table>	Status	Default Status	Power On Sequence	Disable	S/W Reset	Disable	H/W Reset	Disable				
Status	Default Status												
Power On Sequence	Disable												
S/W Reset	Disable												
H/W Reset	Disable												

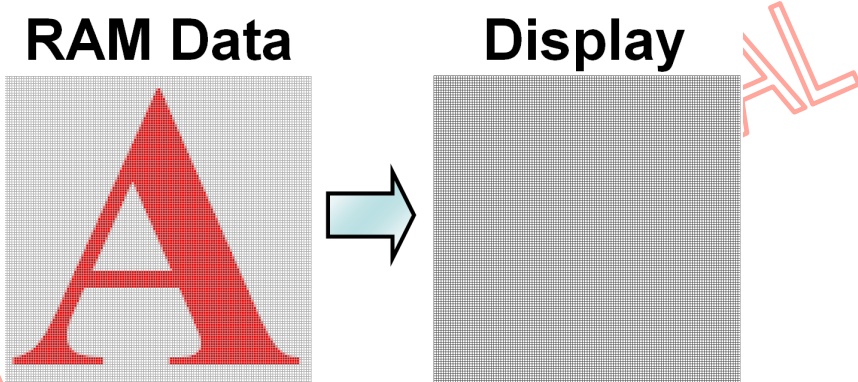
GMASET (26h): Gamma Curves Selection

Address (MDDI I/F)		2600h					Access Attribute			R/W
Address (Other I/F)		26h					Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

Description	<p>This command is used to select the desired Gamma curve for the current display. Only 1 fixed gamma curve can be selected. The curves are defined in Section "Gamma Curve Correction Power Supply Circuit". The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p>																					
	GC[7:0]		Parameter			Curve Selected																
	01h		GC0			Gamma Curve 1 (Gamma 2.2)																
	02h		GC1			Reversed																
	04h		GC2			Reversed																
08h		GC3			Reversed																	
Restriction	<p>Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.</p>																					
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Partial Mode On, Idle Mode Off, Sleep Out	Yes																					
Partial Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default Value	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">01h</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">01h</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">01h</td> </tr> </tbody> </table>					Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h									
Status	Default Value																					
Power On Sequence	01h																					
S/W Reset	01h																					
H/W Reset	01h																					

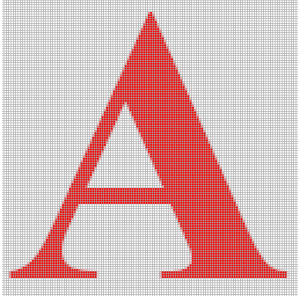
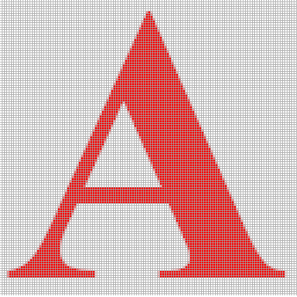
SET_DISPLAY_OFF (28h): Display Off

Address (MDDI I/F)		2800h					Access Attribute			W
Address (Other I/F)		28h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Display Off

Description	<p>- This command is used to enter to the DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page is inserted. This command makes no change of contents of frame memory, and does not change any other status. There will be no abnormal visible effects on the display. Exit from this command by the Display On command (29h) Example:</p> <div style="text-align: center;">  <p>RAM Data Display</p> </div>												
Restriction	- This command has no effect when the module is already in Display Off mode.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Status</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>	Status	Default Status	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Status												
Power On Sequence	Display Off												
S/W Reset	Display Off												
H/W Reset	Display Off												

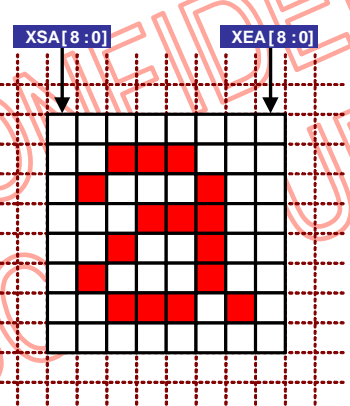
SET_DISPLAY_ON (29h): Display On

Address (MDDI I/F)		2900h					Access Attribute			W
Address (Other I/F)		29h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Display Off

Description	<p>- This command is used to recover from the DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory, and does not change any other status. Example:</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>RAM Data</p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div>													
	<p>- This command has no effect when the module is already in Display On mode</p>													
Restriction														
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Sleep In	Yes													
Default Value	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Status</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>		Status	Default Status	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
	Status	Default Status												
	Power On Sequence	Display Off												
	S/W Reset	Display Off												
H/W Reset	Display Off													

SET_HORIZONTAL_ADDRESS (2Ah): Set the Column Address

Address (MDDI I/F)		2A00h ~2A03h					Access Attribute				R/W
Address (Other I/F)		2Ah					Number of Parameter(s)				4
Address (MDDI I/F)	Parameter	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
2A00h	Parameter 1	00h	0	0	0	0	0	0	0	XSA8	00h
2A01h	Parameter 2	00h	XSA7	XSA6	XSA5	XSA4	XSA3	XSA2	XSA1	XSA0	00h
2A02h	Parameter 3	00h	0	0	0	0	0	0	0	XEA8	By Resolution
2A03h	Parameter 4	00h	XEA7	XEA6	XEA5	XEA4	XEA3	XEA2	XEA1	XEA0	By Resolution

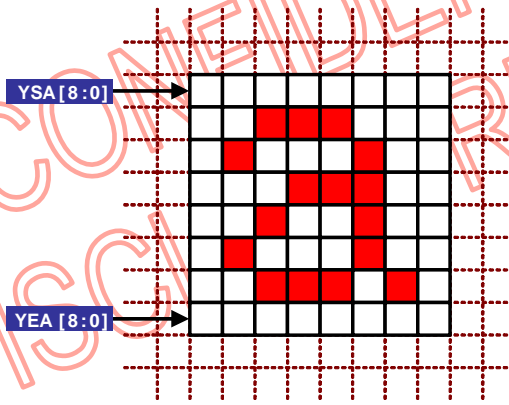
Description	<p>- This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. The value of XSA [8 : 0] and XEA [8 : 0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. Example:</p> <div style="text-align: center;">  </div>												
Restriction	<p>(1) XSA[8 : 0] must always be equal to or less than XEA[8 : 0] (2) If XSA[8 : 0] or XEA[8 : 0] is greater than the available frame memory then the parameter is not updated.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #4a7ebb; color: white;">Status</th> <th style="background-color: #4a7ebb; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	<p>2A00h ~ 2A01h:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f2f1;">Status</th> <th style="background-color: #e0f2f1;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

Default Value	2A02h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h
	Status	Default Value									
	Power On Sequence	01h									
	S/W Reset	01h									
	H/W Reset	01h									
	2A03h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	3Fh	S/W Reset	3Fh	H/W Reset	3Fh
	Status	Default Value									
	Power On Sequence	3Fh									
	S/W Reset	3Fh									
	H/W Reset	3Fh									

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SET_VERTICAL_ADDRESS (2Bh): Set Page Address

Address (MDDI I/F)		2B00h ~ 2B03h					Access Attribute				R/W
Address (Other I/F)		2B					Number of Parameter(s)				4
Address (Other I/F)	Parameter	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
2B00h	Parameter 1	00h	0	0	0	0	0	0	0	YSA8	00h
2B01h	Parameter 2	00h	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0	00h
2B02h	Parameter 3	00h	0	0	0	0	0	0	0	YEA8	By Resolution
2B03h	Parameter 4	00h	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0	By Resolution

Description	<p>- This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. The value of YSA [8 : 0] and YEA [8 : 0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. Example:</p> 												
Restriction	<p>(1) YSA[8 : 0] must always be equal to or less than YEA[8 : 0] (2) If YSA[8 : 0] or YEA[8 : 0] is greater than the available frame memory then the parameter is not updated.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #4a7ebb; color: white;">Status</th> <th style="background-color: #4a7ebb; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	<p>2B00h ~ 2B01h:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #e0f7fa;">Status</th> <th style="background-color: #e0f7fa;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">00h</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">00h</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

Default Value	2B02h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h
	Status	Default Value								
	Power On Sequence	01h								
	S/W Reset	01h								
	H/W Reset	01h								
	2B03h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>DFh</td> </tr> <tr> <td>S/W Reset</td> <td>DFh</td> </tr> <tr> <td>H/W Reset</td> <td>DFh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	DFh	S/W Reset	DFh	H/W Reset	DFh
	Status	Default Value								
	Power On Sequence	DFh								
	S/W Reset	DFh								
	H/W Reset	DFh								

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WRITE_MEMORY_START (2Ch): Memory Write Start Command

Address (MDDI I/F)	2C00h						Access Attribute			W
Address (Other I/F)	2Ch						Number of Parameter(s)			By Application
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Image Data 1	D0[15 : 8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	N/A
Image Data 2	D1[15 : 8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	N/A
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Image Data N	Dn[15 : 8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	N/A

Description	- This command writes data into the partial memory. It initializes the memory write address pointer to the start of the memory. Frame pointer auto-increments when data is written. Note: About Read / Write Frame Data via all kinds of supported interface, please refer to the chapter 5 for detailed.												
Restriction	(1) A WRITE_MEMORY_START should follow a SET_COLUMN_ADDRESS, SET_PAGE_ADDRESS or SET_ADDRESS_MODE to define the write location. Otherwise, data written with WRITE_MEMORY_START and any following WRITE_MEMORY_CONTINUE commands is written to undefined locations. (2) This command is not supported MDDI interface.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	N/A												

SET_MDDI_RAM_READ_ADDRESS (2Dh): Set the RAM Horizontal and Vertical Address

Address (MDDI I/F)		2D00h ~ 2D03h					Access Attribute				R/W
Address (Other I/F)		2Dh					Number of Parameter(s)				4
Address (Other I/F)	Parameter	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
2D00h	Parameter 1	00h	0	0	0	0	0	0	0	XAD8	00h
2D01h	Parameter 2	00h	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0	00h
2D02h	Parameter 3	00h	0	0	0	0	0	0	0	YAD8	00h
2D03h	Parameter 4	00h	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0	00h

Description	<p>- XAD[8 : 0], YAD[8 : 0]: MDDI RAM read address, which is set initially in the AC (Address Counter). The NT35310 writes data to the internal RAM so that data is written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal RAM.</p> <table border="1"> <thead> <tr> <th>YAD[8 : 0] — XAD[8 : 0]</th> <th>RAM Data Setting</th> </tr> </thead> <tbody> <tr> <td>20'h000:000 – 20'h000:67B</td> <td>Bitmap data on the 1st line</td> </tr> <tr> <td>20'h001:000 – 20'h001:67B</td> <td>Bitmap data on the 2nd line</td> </tr> <tr> <td>20'h002:000 – 20'h002:67B</td> <td>Bitmap data on the 3rd line</td> </tr> <tr> <td>20'h003:000 – 20'h003:67B</td> <td>Bitmap data on the 4th line</td> </tr> <tr> <td>20'h004:000 – 20'h004:67B</td> <td>Bitmap data on the 5th line</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>20'h1DC:000 – 20'h1DC:67B</td> <td>Bitmap data on the 477 line</td> </tr> <tr> <td>20'h1DD:000 – 20'h1DD:67B</td> <td>Bitmap data on the 478 line</td> </tr> <tr> <td>20'h1DE:000 – 20'h1DE:67B</td> <td>Bitmap data on the 479 line</td> </tr> <tr> <td>20'h1DF:000 – 20'h1DF:67B</td> <td>Bitmap data on the 480 line</td> </tr> </tbody> </table> <p><i>Note: This table is for portrait (320RGBx480) application.</i></p>											YAD[8 : 0] — XAD[8 : 0]	RAM Data Setting	20'h000:000 – 20'h000:67B	Bitmap data on the 1 st line	20'h001:000 – 20'h001:67B	Bitmap data on the 2 nd line	20'h002:000 – 20'h002:67B	Bitmap data on the 3 rd line	20'h003:000 – 20'h003:67B	Bitmap data on the 4 th line	20'h004:000 – 20'h004:67B	Bitmap data on the 5 th line	:	:	20'h1DC:000 – 20'h1DC:67B	Bitmap data on the 477 line	20'h1DD:000 – 20'h1DD:67B	Bitmap data on the 478 line	20'h1DE:000 – 20'h1DE:67B	Bitmap data on the 479 line	20'h1DF:000 – 20'h1DF:67B	Bitmap data on the 480 line
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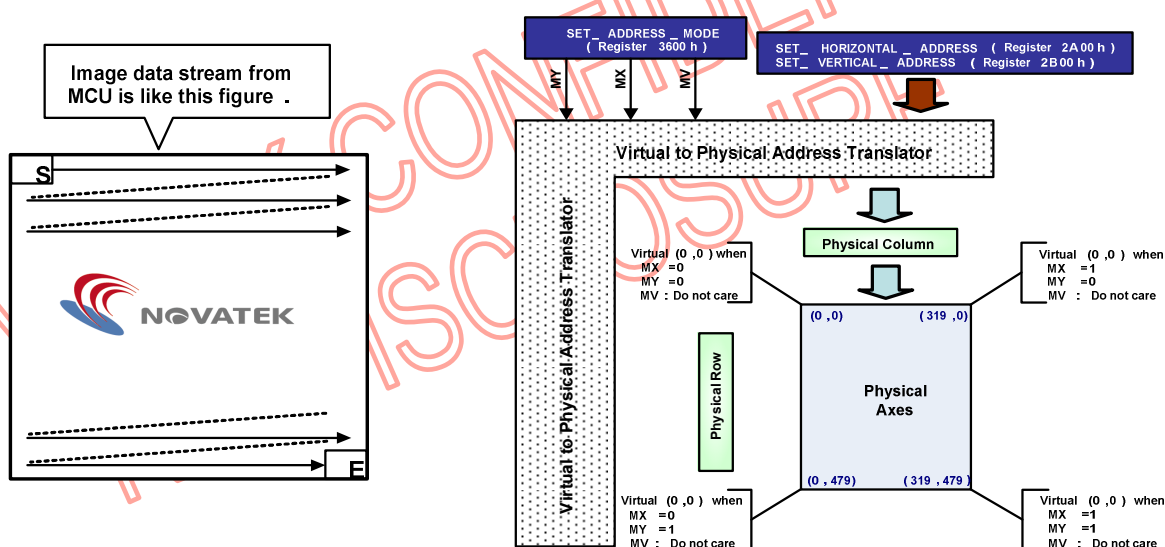
READ_MEMORY_START (2Eh): Memory Read Start Command

Address (MDDI I/F)	2E00h						Access Attribute			R
Address (Other I/F)	2Eh						Number of Parameter(s)			By Application
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Image Data 1	D0[15 : 8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	N/A
Image Data 2	D1[15 : 8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	N/A
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Image Data N	Dn[15 : 8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	N/A

- This command is used to transfer data from frame memory to MPU.

When this command is accepted, the column register and the row register are reset to the Start Column / Start Row positions. And the Start Column / Start Row positions are different in accordance with SET_ADDRESS_MODE (Register 3600h) setting.

Description



Note:

1. Commands "Memory Write Continuously (3C00h)" and "Memory Read Continuously (3E00h)" do not return the column counter to "Start Column" and the row counter to "Start Row".
2. Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MSET_ADDRESS_MODE bit MY, MX and MV.

Restriction	(1) There is no restriction on length of parameters in MIPI, CPU interface and SPI. (2) MDDI interface only support single RAM read.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default Value	N/A													

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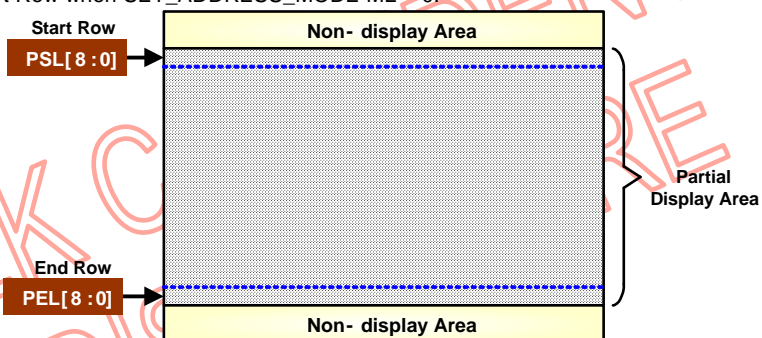
SET_PARTIAL_AREA (30h): Defines the Partial Display Area

Address (MDDI I/F)		3000h ~ 3003h					Access Attribute				R/W
Address (Other I/F)		30h					Number of Parameter(s)				4
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
3000h	Parameter 1	00h	0	0	0	0	0	0	0	PSL8	00h
3001h	Parameter 2	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h
3002h	Parameter 3	00h	0	0	0	0	0	0	0	PEL8	By Resolution
3003h	Parameter 4	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	By Resolution

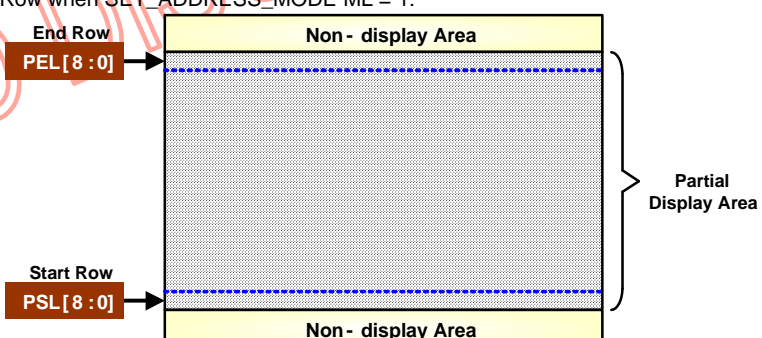
Description

- This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

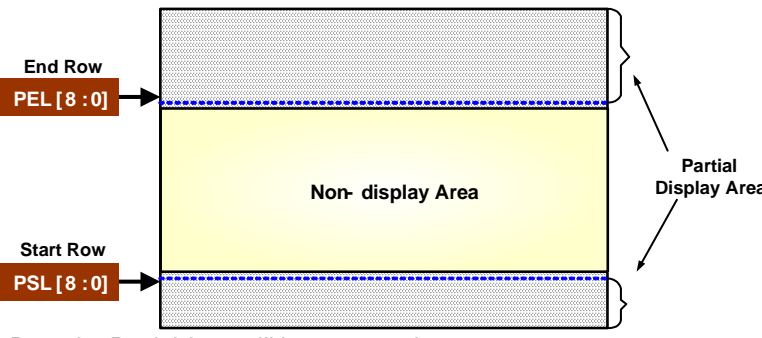
If End Row > Start Row when SET_ADDRESS_MODE ML = 0:



If End Row > Start Row when SET_ADDRESS_MODE ML = 1:



If End Row < Start Row when SET_ADDRESS_MODE ML = 0:



If End Row = Start Row, the Partial Area will be one row deep.

Restriction

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default Value	3000h ~ 3001h:	
	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
	3002h:	
	Status	Default Value
	Power On Sequence	01h
	S/W Reset	01h
	H/W Reset	01h
	3003h:	
	Status	Default Value
Power On Sequence	DFh	
S/W Reset	DFh	
H/W Reset	DFh	

SCRLAR (33h): Set Scroll Area

Address (MDDI I/F)		3300h ~ 3305h					Access Attribute				R/W
Address (Other I/F)		33h					Number of Parameter(s)				6
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
3300h	Parameter 1	00h	0	0	0	0	0	0	0	TFA8	00h
3301h	Parameter 2	00h	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	00h
3302h	Parameter 3	00h	0	0	0	0	0	0	0	VSA8	By Resolution
3303h	Parameter 4	00h	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	By Resolution
3304h	Parameter 5	00h	0	0	0	0	0	0	0	BFA8	00h
3305h	Parameter 6	00h	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	00h

Description

- This command defines the Vertical Scrolling Area of the display.

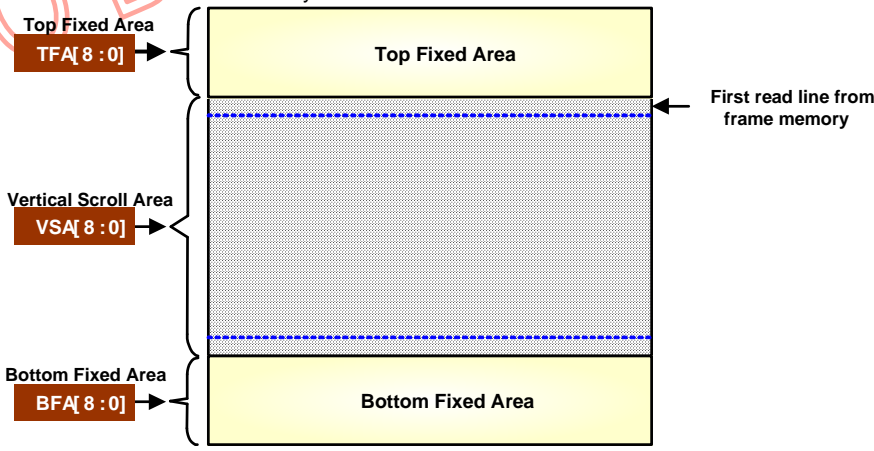
When MADCTR ML = 0:

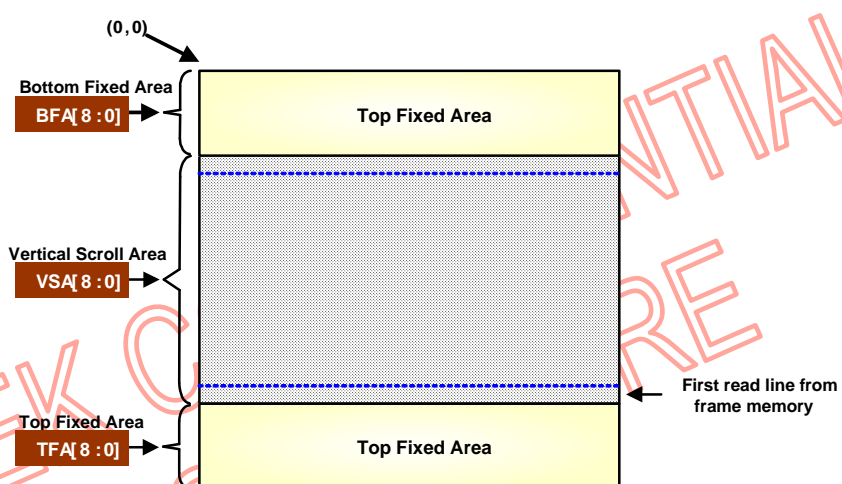
TFA [8 : 0]: Describes the Top Fixed Area (in number of lines from Top of the Frame Memory and Display).

VSA [8 : 0]: Describes the height of the Vertical Scrolling Area (in number of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.

BFA [8 : 0]: Describes the Bottom Fixed Area (in number of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory row address.



Description	<p>When MADCTR ML = 1:</p> <p>TFA [8 : 0]: Describes the Top Fixed Area (in number of lines from Bottom of the Frame Memory and Display).</p> <p>VSA [8 : 0]: Describes the height of the Vertical Scrolling Area (in number of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the top most line of the Top Fixed Area.</p> <p>BFA [8 : 0]: Describes the Bottom Fixed Area (in number of lines from Top of the Frame Memory and Display).</p> 												
Restriction	<p>(1) The condition is $(TFA + VSA + BFA) = \text{Scan Line}$, otherwise Scrolling mode is undefined.</p> <p>(2) In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'. It only affects the Frame Memory Write.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default Value	3300h, 3301h, 3304h, 3305h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
	Status	Default Value									
	Power On Sequence	00h									
	S/W Reset	00h									
	H/W Reset	00h									
	3302h:	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h
	Status	Default Value									
	Power On Sequence	01h									
	S/W Reset	01h									
	H/W Reset	01h									
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	Status	Default Value									
Power On Sequence	E0h										
S/W Reset	E0h										
H/W Reset	E0h										

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SET_TEAR_OFF (34h): Tearing Effect Line OFF

Address (MDDI I/F)		3400h					Access Attribute			W
Address (Other I/F)		34h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									TE Line Off

Description	- This command is used to turn OFF (Active Low) the output TE trigger message from the display module.
Restriction	- This command has no effect when TE is already OFF.

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	

Default Value	Status		Default Status	
	Power On Sequence		TE Line Off	
	S/W Reset		TE Line Off	
	H/W Reset		TE Line Off	

SET_TEAR_ON (35h): Tearing Effect Line ON

Address (MDDI I/F)	3500h					Access Attribute				R/W
Address (Other I/F)	35h					Number of Parameter(s)				1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	TEW3	TEW2	TEW1	TEW0	0	0	TEP	M	00h

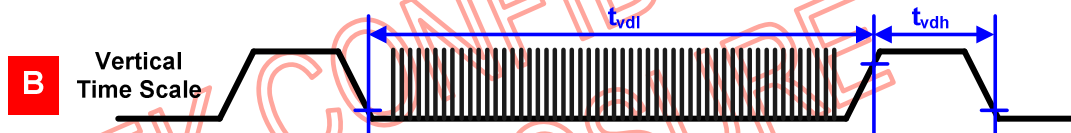
- This command is used to turn ON the Tearing Effect output from the TE signal. This output is not affected by changing MADCTR bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

When **M = 0** : The Tearing Effect Output line consists of V-Blanking information only.



When **M = 1** : The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.



Note : During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Register 35h & 44h both define TE Output :

Register 35h	Register 44h	TE Output
M	N	
0	0	TE high in V-porch region (A)
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

This command is used to turn ON the output TE trigger message from display module.

This output is not affected by changing SET_ADDRESS_MODE bit ML.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X = Don't Care).

TEP: Set the polarity of FTE signal.

0: Active High.

1: Active Low.

Description

Description	TEW[3:0]: Tearing output width control for type C.														
	<table border="1"> <thead> <tr> <th>TE_W[3:0]</th> <th>TE output period</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TE output 1 line period</td> </tr> <tr> <td>1</td> <td>TE output 2 line period</td> </tr> <tr> <td>2</td> <td>TE output 3 line period</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>14</td> <td>TE output 15 line period</td> </tr> <tr> <td>15</td> <td>TE output 16 line period</td> </tr> </tbody> </table>		TE_W[3:0]	TE output period	0	TE output 1 line period	1	TE output 2 line period	2	TE output 3 line period	:	:	14	TE output 15 line period	15
TE_W[3:0]	TE output period														
0	TE output 1 line period														
1	TE output 2 line period														
2	TE output 3 line period														
:	:														
14	TE output 15 line period														
15	TE output 16 line period														
Restriction	- This command has no effect when Tearing Effect output is already ON.														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Sleep In	Yes														
Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> <th>Notes</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>TEW[3 : 0]= 0 (1 Line)</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>TEP = 0 (Active High)</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>M = 0(TE high in V-porch region (A))</td> </tr> </tbody> </table>		Status	Default Value	Notes	Power On Sequence	00h	TEW[3 : 0]= 0 (1 Line)	S/W Reset	00h	TEP = 0 (Active High)	H/W Reset	00h	M = 0(TE high in V-porch region (A))	
Status	Default Value	Notes													
Power On Sequence	00h	TEW[3 : 0]= 0 (1 Line)													
S/W Reset	00h	TEP = 0 (Active High)													
H/W Reset	00h	M = 0(TE high in V-porch region (A))													

SET_ADDRESS_MODE (36h): Memory Data Access Control

Address (MDDI I/F)		3600h					Access Attribute			R/W
Address (Other I/F)		36h					Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	MY	MX	MV	ML	RGB	MH	0	0	00h

Description	<p>- This command defines read/write scanning direction of the frame memory. This command makes no change on the other driver status.</p> <p>MY:</p> <p>- Automatically increments (+1) or decrements (-1) the row address counter (AC)</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MY</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Increase in vertical</td> </tr> <tr> <td>1</td> <td>Decrease in vertical</td> </tr> </tbody> </table>	MY	Function	0	Increase in vertical	1	Decrease in vertical
	MY	Function					
	0	Increase in vertical					
	1	Decrease in vertical					
	<p>MX:</p> <p>- Automatically increments (+1) or decrements (-1) the column address counter (AC)</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MX</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Increase in horizon</td> </tr> <tr> <td>1</td> <td>Decrease in horizon</td> </tr> </tbody> </table>	MX	Function	0	Increase in horizon	1	Decrease in horizon
	MX	Function					
0	Increase in horizon						
1	Decrease in horizon						
<p>MV:</p> <p>- Determines the direction in which the address counter is updated automatically as the NT35310 writes data to the internal GRAM.</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MV</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Horizontal Direction</td> </tr> <tr> <td>1</td> <td>Vertical Direction</td> </tr> </tbody> </table>	MV	Function	0	Horizontal Direction	1	Vertical Direction	
MV	Function						
0	Horizontal Direction						
1	Vertical Direction						
<p>ML:</p> <p>- This bit is used to control the LCD refresh order in vertical direction</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>ML</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Top to Bottom</td> </tr> <tr> <td>1</td> <td>Bottom to Top</td> </tr> </tbody> </table>	ML	Function	0	Top to Bottom	1	Bottom to Top	
ML	Function						
0	Top to Bottom						
1	Bottom to Top						
<p>MH:</p> <p>- This bit is used to control the LCD refresh order in horizontal direction</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>MH</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Left to Right</td> </tr> <tr> <td>1</td> <td>Right to Left</td> </tr> </tbody> </table>	MH	Function	0	Left to Right	1	Right to Left	
MH	Function						
0	Left to Right						
1	Right to Left						

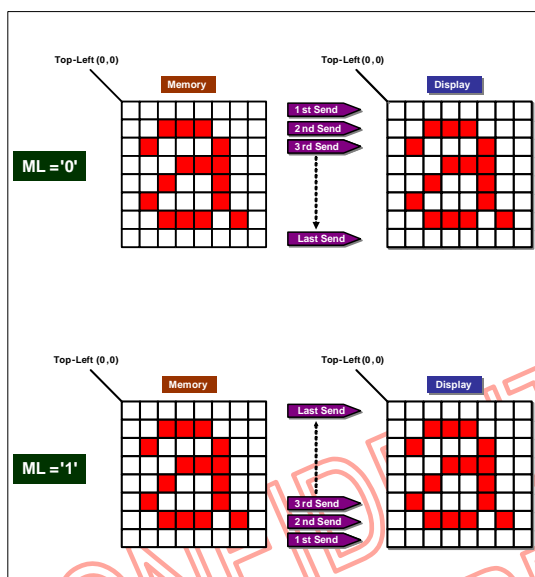
Description
RGB:

- Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

Note : The R,B Gamma will also swap.

Note:

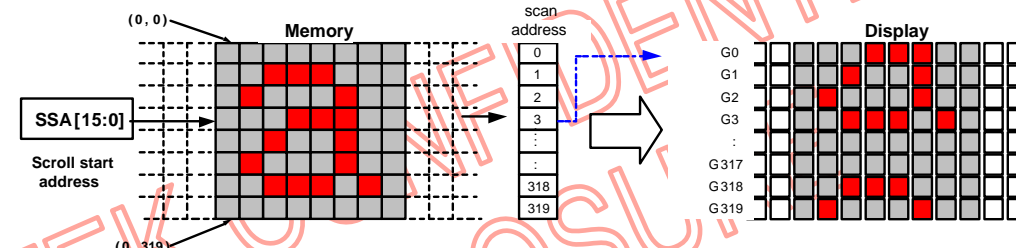
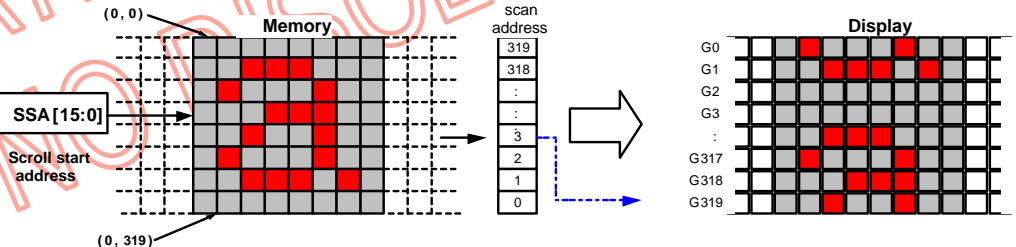
Register			SRAM Address & Source			Panel
MX	CRL	MH	Horizon SRAM Write	Horizon SRAM Display Read	Source Scane	Display
0	0	0	Increase	Increase	Increase	Normal
0	0	1	Increase	Decrease	Decrease	Normal
0	1	0	Increase	Increase	Decrease	Reverse
0	1	1	Increase	Decrease	Increase	Reverse
1	0	0	Decrease	Increase	Increase	Reverse
1	0	1	Decrease	Decrease	Decrease	Reverse
1	1	0	Decrease	Increase	Decrease	Normal
1	1	1	Decrease	Decrease	Increase	Normal



Description	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th colspan="3">Register</th> <th colspan="3">SRAM Address</th> <th>Panel</th> </tr> <tr style="background-color: #800080; color: white;"> <th>MY</th> <th>ML</th> <th>CTB</th> <th>Vertical SRAM Write</th> <th>Vertical SRAM Display Read</th> <th>Gate Scane</th> <th>Display</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Increase</td> <td>Increase</td> <td>Top to Bottom</td> <td>Normal</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Increase</td> <td>Increase</td> <td>Bottom to Top</td> <td>Reverse</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Increase</td> <td>Decrease</td> <td>Bottom to Top</td> <td>Normal</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Increase</td> <td>Decrease</td> <td>Top to Bottom</td> <td>Reverse</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Decrease</td> <td>Increase</td> <td>Top to Bottom</td> <td>Reverse</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Decrease</td> <td>Increase</td> <td>Bottom to Top</td> <td>Normal</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Decrease</td> <td>Decrease</td> <td>Bottom to Top</td> <td>Reverse</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Decrease</td> <td>Decrease</td> <td>Top to Bottom</td> <td>Normal</td> </tr> </tbody> </table>							Register			SRAM Address			Panel	MY	ML	CTB	Vertical SRAM Write	Vertical SRAM Display Read	Gate Scane	Display	0	0	0	Increase	Increase	Top to Bottom	Normal	0	0	1	Increase	Increase	Bottom to Top	Reverse	0	1	0	Increase	Decrease	Bottom to Top	Normal	0	1	1	Increase	Decrease	Top to Bottom	Reverse	1	0	0	Decrease	Increase	Top to Bottom	Reverse	1	0	1	Decrease	Increase	Bottom to Top	Normal	1	1	0	Decrease	Decrease	Bottom to Top	Reverse	1	1	1	Decrease	Decrease	Top to Bottom	Normal
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Restriction	- This command has no effect when Tearing Effect output is already ON.																																																																												
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VSCSAD (37h): Vertical Scroll Start Address of RAM

Address (MDDI I/F)		3700h ~ 3701h					Access Attribute				R/W
Address (Other I/F)		37h					Number of Parameter(s)				2
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
3700h	Parameter 1	00h	0	0	0	0	0	0	0	SSA8	00h
3701h	Parameter 2	00h	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	00h

Description	<p>- This command is used together with Vertical Scrolling Definition. These two commands describe the scrolling area and the scrolling mode.</p> <p>The Vertical Scrolling Start Address command has one parameter that describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below :</p> <p>When MADCTR ML = "0": When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and Vertical Scrolling Pointer, SSA = '3'.</p> 
	<p>When MADCTR ML = "1": When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and SSA = '3'</p> 
Restriction	<p>Note : When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel</p> <p>Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.</p>
	<p>- Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h), otherwise undesirable image will be displayed on the Panel. SSA[15 : 0] is based on 1-line unit.</p>

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	No
	Partial Mode On, Idle Mode On, Sleep Out	No
	Sleep In	Yes
Default Value	3700h ~ 3701h:	
	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

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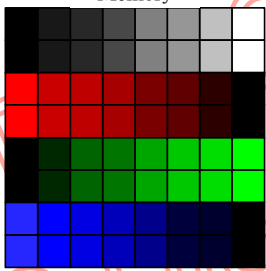
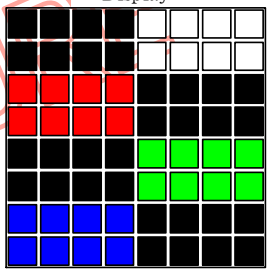
EXIT_IDLE_MODE (38h): Idle Mode Off

Address (MDDI I/F)		3800h					Access Attribute			W
Address (Other I/F)		38h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Idle Mode Off

Description	<p>- This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition.</p> <p>When the Idle Mode is "Off":</p> <p>(1) LCD can display with maximum 65k or 262k-colors. (2) Normal frame frequency is applied.</p>												
Restriction	- This command has no effect when module is already in idle off mode.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Status												
Power On Sequence	Idle Mode Off												
S/W Reset	Idle Mode Off												
H/W Reset	Idle Mode Off												

ENTER_IDLE_MODE (39h): Idle Mode On

Address (MDDI I/F)		3900h					Access Attribute			W
Address (Other I/F)		39h					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									Idle Mode Off

Description	<p>- This command is used to enter into Idle mode on.</p> <p>There will be no abnormal visible effect on the display mode change transition.</p> <p>When the Idle Mode is "On":</p> <ol style="list-style-type: none"> (1) Color expression is reduced. The primary and the secondary colors using MSB of each RMG and B in the Frame Memory, 8 color depth data is displayed. (2) 8-Color mode frame frequency is applied. (3) Exit from IDMON by Idle Mode Off (3800h) command <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="font-size: 2em; color: gray;">→</div> <div style="text-align: center;"> <p>Display</p>  </div> </div> <table border="1" style="margin-top: 10px; width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>Color</th> <th>R5R4R3R2R1R0</th> <th>G5G4G3G2G1G0</th> <th>B5B4B3B4B1B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td>0XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>0XXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td>1XXXXX</td> <td>1XXXXX</td> </tr> </tbody> </table>	Color	R5R4R3R2R1R0	G5G4G3G2G1G0	B5B4B3B4B1B0	Black	0XXXXX	0XXXXX	0XXXXX	Blue	0XXXXX	0XXXXX	1XXXXX	Red	1XXXXX	0XXXXX	0XXXXX	Magenta	1XXXXX	0XXXXX	1XXXXX	Green	0XXXXX	1XXXXX	0XXXXX	Cyan	0XXXXX	1XXXXX	1XXXXX	Yellow	1XXXXX	1XXXXX	0XXXXX	White	1XXXXX	1XXXXX	1XXXXX
	Color	R5R4R3R2R1R0	G5G4G3G2G1G0	B5B4B3B4B1B0																																	
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Blue	0XXXXX	0XXXXX	1XXXXX																																		
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Restriction	- This command has no effect when module is already in Idle On Mode.																																				
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Default Value	Status	Default Status
	Power On Sequence	Idle Mode Off
	S/W Reset	Idle Mode Off
	H/W Reset	Idle Mode Off

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SET_PIXEL_FORMAT (3Ah): Set the Interface Pixel Format

Address (MDDI I/F)	3A00h						Access Attribute			R/W
Address (Other I/F)	3Ah						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter	00h	0	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	66h

Description	<p>- This command is used to define the format of RGB picture data, which is to be transferred via the MPU Interface. The formats are shown in the table:</p> <p>IFPF[2 : 0]: Set the pixel format on MCU I/F</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">IFPF[2 : 0]</th> <th rowspan="2">MCU Interface Color Format</th> </tr> <tr> <th>Binary</th> <th>DEC</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">101</td> <td style="text-align: center;">5</td> <td style="text-align: center;">16-bits / pixel</td> </tr> <tr> <td style="text-align: center;">110</td> <td style="text-align: center;">6</td> <td style="text-align: center;">18-bits / pixel</td> </tr> <tr> <td style="text-align: center;">111</td> <td style="text-align: center;">7</td> <td style="text-align: center;">24-bits / pixel (MIPI only)</td> </tr> <tr> <td colspan="3">Others are not defined.</td> </tr> </tbody> </table> <p>VIPF[2 : 0] : Set the pixel format on RGB I/F</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">VIPF[2 : 0]</th> <th rowspan="2">RGB Interface Color Format</th> </tr> <tr> <th>Binary</th> <th>DEC</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">101</td> <td style="text-align: center;">5</td> <td style="text-align: center;">16 bits / pixel (1-time transfer)</td> </tr> <tr> <td style="text-align: center;">110</td> <td style="text-align: center;">6</td> <td style="text-align: center;">18 bits / pixel (1-time transfer)</td> </tr> <tr> <td colspan="3">Others are not defined.</td> </tr> </tbody> </table>	IFPF[2 : 0]		MCU Interface Color Format	Binary	DEC	101	5	16-bits / pixel	110	6	18-bits / pixel	111	7	24-bits / pixel (MIPI only)	Others are not defined.			VIPF[2 : 0]		RGB Interface Color Format	Binary	DEC	101	5	16 bits / pixel (1-time transfer)	110	6	18 bits / pixel (1-time transfer)	Others are not defined.		
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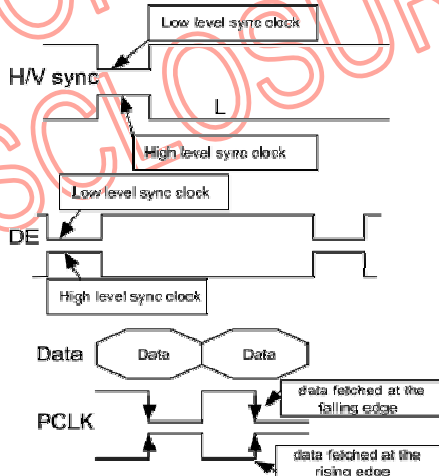
RGBCTRL (3Bh): RGB Interface Signal Control

Address (MDDI I/F)		3B00h ~ 3B04h					Access Attribute				R/W
Address (Other I/F)		3Bh					Number of Parameter(s)				5
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
3B00h	Parameter 1	00h	0	CRCM	0	0	DP	EP	HSP	VSP	03h
3B01h	Parameter 2	00h	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	0Ch
3B02h	Parameter 3	00h	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	04h
3B03h	Parameter 4	00h	0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	28h
3B04h	Parameter 5	00h	0	HFP6	HFP5	HFP4	HFP3	HFP2	HFP1	HFP0	32h

- Set the operation status on the RGB interface. The setting becomes effective as long as the command is received.

CRCM: Determines the RGB Mode 1 & RGB Mode 2

CRCM	RGB Mode Selection
0	RGB Mode 1
1	RGB Mode 2



Description

RGB I/F Mode	PCLK	DE	D[17 : 0]	VS	HS	Register VBP[6 : 0], HBP[6 : 0], VFP[6 : 0], HFP[6 : 0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

DP / EP / HSP / VSP: Clock polarity set for RGB Interface

Symbol	Name	Clock Polarity Set For RGB Interface
DP	PCLK Polarity Set	'0' = Data fetched at the rising edge '1' = Data fetched at the falling edge
EP	DE Polarity Set	'0' = High enable for RGB interface '1' = Low enable for RGB interface
HSP	Hsync Polarity Set	'0' = High level sync clock '1' = Low level sync clock
VSP	Vsync Polarity Set	'0' = High level sync clock '1' = Low level sync clock

VBP[6 : 0], VFP[6 : 0], HBP[6 : 0], and HFP[6 : 0]:

Vertical and Horizontal back and front porch control when RGB I/F mode 2 only.

VBP[6 : 0]: Number of lines for the back porch of VSYNC.

VFP[6 : 0]: Number of lines for the front porch of VSYNC.

HBP[6 : 0]: Number of clock for the back porch of HSYNC.

HFP[6 : 0]: Number of clock for the front porch of HSYNC.

VBP[6 : 0]	Back Porch Line Number	VFP[6 : 0]	Front Porch Line Number	HBP[6 : 0]	Back Porch Pixel clocks	HFP[6 : 0]	Front Porch Pixel Clocks
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved	01d	1	01d	1
Reserved	Reserved	Reserved	Reserved	02d	2	02d	2
Reserved	Reserved	Reserved	Reserved	03d	3	03d	3
04d	4	04d	4	04d	4	04d	4
:	:	:	:	:	:	:	:
:	(STEP 1)	:	(STEP 1)	:	(STEP 1)	:	(STEP 1)
:	:	:	:	:	:	:	:
61d	61	61d	61	61d	61	61d	61
62d	62	62d	62	62d	62	62d	62
63d	63	63d	63	63d	63	63d	63

Description

Note: MIPI Video mode please keep HBP at 2us, HFP at 500UI.

Restriction

- There is no visible effect until the Frame Memory is written to.

Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default Value	3B00h:		
	Status	Default Value	Note
	Power On Sequence	03h	CRCM = '0' (RGB Mode 1) ICM = '0' (PCLK) DP = '0', EP = '0', HSP = '1' (Low Level), VSP = '1' (Low Level)
	H/W Reset	03h	
	3B01h:		
	Status	Default Value	Note
	Power On Sequence	06h	VBP[5 : 0] = 6 VFP[5 : 0] = 2
	H/W Reset	06h	
	3B02h:		
	Status	Default Value	Note
	Power On Sequence	02h	VBP[5 : 0] = 6 VFP[5 : 0] = 2
	H/W Reset	02h	
	3B03h:		
	Status	Default Value	Note
	Power On Sequence	14h	HBP[5 : 0] = 14 HFP[5 : 0] = 19
	H/W Reset	14h	
	3B04h:		
	Status	Default Value	Note
	Power On Sequence	19h	HBP[5 : 0] = 14 HFP[5 : 0] = 19
	H/W Reset	19h	

RAMWRC (3Ch): Memory Write Continuously

Address (MDDI I/F)	3C00h						Access Attribute			W
Address (Other I/F)	3Ch						Number of Parameter(s)			By Application
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Image Data 1	D0[15 : 8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	N/A
Image Data 2	D1[15 : 8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	N/A
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Image Data N	Dn[15 : 8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	N/A

Description	- This command is used to transfer data from MCU to display area, if wants to continue memory write after Memory Write (2Ch) command.												
Restriction	- This command is not supported in MDDI I/F.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	N/A												

RAMRDC (3Eh) : RAM Read Continuously

Address (MDDI I/F)	3E00h						Access Attribute			R
Address (Other I/F)	3Eh						Number of Parameter(s)			By Application
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Image Data 1	D0[15 : 8]	D0[7]	D0[6]	D0[5]	D0[4]	D0[3]	D0[2]	D0[1]	D0[0]	N/A
Image Data 2	D1[15 : 8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	N/A
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Image Data N	Dn[15 : 8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	N/A

Description	- This command is used to transfer data from frame memory to MCU, if wants to continue memory write after Memory Read Start (2Eh) command.	
Restriction	- This command is not supported in MDDI I/F.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default Value	N/A	

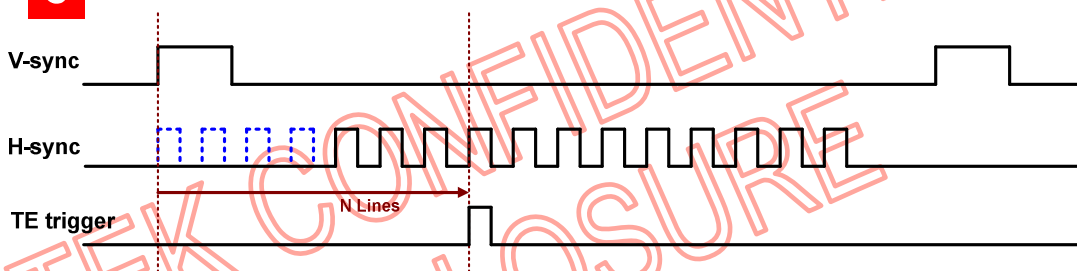
SET_TEAR_SCANLINE (44h): Set Tear Line

Address (MDDI I/F)		4400h ~ 4401h					Access Attribute				R/W
Address (Other I/F)		44h					Number of Parameter(s)				2
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
4400h	Parameter 1	00h	0	0	0	0	0	0	0	N8	00h
4401h	Parameter 2	00h	N7	N6	N5	N4	N3	N2	N1	N0	00h

- The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.

Note :

- (1) That TEARLINE with N = '0' is equivalent to TEON with M = '0'.
- (2) The Tearing Effect Output line shall be active low when the display module is in Sleep mode.



Register 3500h, 4400h and 4401h both define TE Output :

3500h	4400h ~ 4401h	TE Output
M	N	
0	0	TE high in V-porch region (A)
1	0	TE high in all V-porch and H-porch region (B)
0	≠ 0	TE high at N-th line (C)
1	≠ 0	TE high in all V-porch and H-porch region (B)

Description

This command is used to set the FTE output position.
Use "SET_TEAR_ON (3500h)" to set the FTE polarity and pulse width.

N[8 : 0]	Function Description
000h	1st Line
001h	2nd Line
002h	3rd Line
003h	4th Line
:	:
:	:
1DDh	478th Line
1DEh	479th Line
1DFh	480th Line

Restriction

- This command takes affect on the frame following the current frame. Therefore, if the Tear Effect (FTE) output is

	already ON, the FTE output shall continue to operate as programmed by the previous SET_TEAR_ON, or SET_TEAR_SCANLINE, command until the end of the frame.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes													
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	Status	Default Value	Note											
	Power On Sequence	00h	(1) N[8 : 0] = 000h: FTE outputs at 1st line. (2) Tearing effect off and M = '0'.											
	S/W Reset	00h												
H/W Reset	00h													

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RDSCL (45h) : Read Scan Line

Address (MDDI I/F)		4500h ~ 4501h					Access Attribute				R
Address (Other I/F)		45h					Number of Parameter(s)				2
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
4500h	Parameter 1	00h	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8	N/A
4501h	Parameter 2	00h	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	N/A

Description	- This command is used to read scan line data.												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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	Status	Default Value											
	Power On Sequence	N/A											
	S/W Reset	N/A											
H/W Reset	N/A												

ENTER_DSTB_MODE (4Fh): Enter the Deep Standby Mode

Address (MDDI I/F)		4F00h					Access Attribute				R/W
Address (Other I/F)		4Fh					Number of Parameter(s)				1
Address (MDDI I/F)	Address (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
4F00h	Parameter 1	00h	0	0	0	0	0	0	0	DSTB	00h

Description	<p>- This command is used to enter deep standby mode. DSTB = '1': Enter the deep standby mode.</p> <p>Notice 1: It can't exit deep standby mode when set DSTB from '1' to '0'. Notice 2: User can not write this register in Sleep-Out or Display-On mode.</p> <p>Note: To exit deep standby mode, please set RESX pin low pulse more than 3 msec</p>												
Restriction	-												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #2e418c; color: white;">Status</th> <th style="background-color: #2e418c; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

WRDISBV (51h): Write Display Brightness

Address (MDDI I/F)		5100h					Access Attribute				W
Address (Other I/F)		51h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5100h	Parameter 1	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description	<p>- This command is used to adjust or returns the brightness value of the display. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <table border="1"> <thead> <tr> <th>DBV[7 : 0]</th> <th>PWM Duty (Ratio)</th> <th>PWM Duty (%)</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Off</td> <td>0%</td> </tr> <tr> <td>01h</td> <td>2 / 256</td> <td>0.78125 %</td> </tr> <tr> <td>02h</td> <td>3 / 256</td> <td>1.171875 %</td> </tr> <tr> <td>03h</td> <td>4 / 256</td> <td>1.5625 %</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>FDh</td> <td>254 / 256</td> <td>99.21875 %</td> </tr> <tr> <td>FEh</td> <td>255 / 256</td> <td>99.609375 %</td> </tr> <tr> <td>FFh</td> <td>1 (Default)</td> <td>100 %</td> </tr> </tbody> </table>		DBV[7 : 0]	PWM Duty (Ratio)	PWM Duty (%)	00h	Off	0%	01h	2 / 256	0.78125 %	02h	3 / 256	1.171875 %	03h	4 / 256	1.5625 %	:	:	:	:	:	:	FDh	254 / 256	99.21875 %	FEh	255 / 256	99.609375 %	FFh	1 (Default)	100 %
	DBV[7 : 0]	PWM Duty (Ratio)	PWM Duty (%)																													
00h	Off	0%																														
01h	2 / 256	0.78125 %																														
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Status	Default Value																															
Power On Sequence	00h																															
S/W Reset	00h																															
H/W Reset	00h																															

RDDISBV (52h): Read Display Brightness

Address (MDDI I/F)		5200h					Access Attribute				R
Address (Other I/F)		52h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5200h	Parameter 1	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description	<p>- This command is used to returns the brightness value of the display.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. Please refer the register "WRDISBV (5100h)" for detailed.</p> <p>DBV[7 : 0] is "0" (RDDISBV, 52h) when display is in sleep-in mode.</p> <p>DBV[7 : 0] is "0" (RDDISBV, 52h) when bit BCTRL of "Write CTRL Display (5300h)" command is "0".</p> <p>DBV[7 : 0] is manual set brightness specified with "Write CTRL Display (5300h)" command when bit BCTRL is "1".</p> <p>When bit BCTRL of "Write CTRL Display (5300h)" command are "1", DBV[7 : 0] output is the brightness value specified with "Write Profile Value for Display (5000h)" command according to the ambient light.</p>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

WRCTRLD (53h): Write CTRL Display

Address (MDDI I/F)		5300h					Access Attribute				W
Address (Other I/F)		53h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5300h	Parameter 1	00h	0	0	BCTRL	-	DD	BL	-	-	00h

Description	<p>- This command is used to control the "LEDPWM" pin, dimming function for CABC. BCTRL: Turn On / Off the brightness control block with the dimming effect. About the register "LEDPWPOL", please refer to the register "ABC_CTRL02 (02C0h)"</p>									
	BCTRL	LEDPWPOL	LEDPWM Pin Final State		Backlight Final State					
	0	0	Keep "LOW" (0% PWM Duty) (Default)		OFF					
	1	0	PWM Output (High level is duty)		ON					
	0	1	Keep "HIGH" (0% PWM Duty)		OFF					
1	1	Inversed PWM Output (Low level is duty)		ON						
<p>DD: Enable / Disable dimming function only for CABC.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #800080; color: white;">DD</th> <th style="background-color: #800080; color: white;">CABC Dimming Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Disabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Enabled (Default)</td> </tr> </tbody> </table>					DD	CABC Dimming Function	0	Disabled	1	Enabled (Default)
DD	CABC Dimming Function									
0	Disabled									
1	Enabled (Default)									
<p>BL: Turn On/Off the backlight control without dimming effect.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #800080; color: white;">BL</th> <th style="background-color: #800080; color: white;">Backlight Control</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">OFF (Default)</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">ON</td> </tr> </tbody> </table>					BL	Backlight Control	0	OFF (Default)	1	ON
BL	Backlight Control									
0	OFF (Default)									
1	ON									
<p>When BL bit change from '1' to '0', backlight is turned off without gradual dimming, even if dimming-on (DD = '1') are selected.</p>										

Description													
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
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Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
	Status	Default Value											
	Power On Sequence	00h											
S/W Reset	00h												
H/W Reset	00h												

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RDCTRLD (54h): Read CTRL Display

Address (MDDI I/F)		5400h					Access Attribute				R
Address (Other I/F)		54h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5400h	Parameter 1	00h	0	0	BCTRL	-	DD	BL	-	-	00h

Description	<p>- This command is used to "read" the setting status of "LEDPWM" pin, dimming function for CABC.</p> <p>BCTRL: Turn On / Off the brightness control block with the dimming effect. About the register "LEDPWPOL", please refer to the register (19C0h)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>BCTRL</th> <th>LEDPWPOL</th> <th>LEDPWM Pin Final State</th> <th>Backlight Final State</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>Keep "LOW" (0% PWM Duty) (Default)</td> <td style="text-align: center;">OFF</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>PWM Output (High level is duty)</td> <td style="text-align: center;">ON</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>Keep "HIGH" (0% PWM Duty)</td> <td style="text-align: center;">OFF</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Inversed PWM Output (Low level is duty)</td> <td style="text-align: center;">ON</td> </tr> </tbody> </table> <p>DD: Enable / Disable dimming function only for CABC.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>DD</th> <th>CABC Dimming Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Disabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Enabled (Default)</td> </tr> </tbody> </table> <p>BL: Turn On/Off the backlight control without dimming effect.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>BL</th> <th>Backlight Control</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>OFF (Default)</td> </tr> <tr> <td style="text-align: center;">1</td> <td>ON</td> </tr> </tbody> </table> <p>When BL bit change from '1' to '0', backlight is turned off without gradual dimming, even if dimming-on (DD = '1') are selected.</p>	BCTRL	LEDPWPOL	LEDPWM Pin Final State	Backlight Final State	0	0	Keep "LOW" (0% PWM Duty) (Default)	OFF	1	0	PWM Output (High level is duty)	ON	0	1	Keep "HIGH" (0% PWM Duty)	OFF	1	1	Inversed PWM Output (Low level is duty)	ON	DD	CABC Dimming Function	0	Disabled	1	Enabled (Default)	BL	Backlight Control	0	OFF (Default)	1	ON
	BCTRL	LEDPWPOL	LEDPWM Pin Final State	Backlight Final State																													
0	0	Keep "LOW" (0% PWM Duty) (Default)	OFF																														
1	0	PWM Output (High level is duty)	ON																														
0	1	Keep "HIGH" (0% PWM Duty)	OFF																														
1	1	Inversed PWM Output (Low level is duty)	ON																														
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1	ON																																
Restriction	-																																
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #2e5496; color: white;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																				
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Power On Sequence	00h																																
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WRCTRLD (55h): Write CTRL Display

Address (MDDI I/F)		5500h					Access Attribute				W
Address (Other I/F)		55h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5500h	Parameter 1	00h	IMAGE_ENHANCEMENT [3:0]			0	0	CABC_COND[1 : 0]			00h

Description	<p>- This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1"> <thead> <tr> <th colspan="2">CABC_COND[1 : 0]</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image (UI-Mode)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture Image (Still-Mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image (Moving-Mode)</td> </tr> </tbody> </table> <p>- The NT35310 provides 4 different Image Enhancement (IE) technologies that include Smart Contrast, Vivid Color, Smart Color and Edge Enhancement. The three sets for IE Low/Medium/High level can be selected by IMAGE_ENHANCE[3:0] as below table. User can define each IE level value of these four IE technologies independently in "CMD2 Page2" Registers. The real register addresses are also described in below table.</p> <table border="1"> <thead> <tr> <th colspan="4">IMAGE_ENHANCEMENT[3:0]</th> <th>IE Level</th> <th>Smart Contrast</th> <th>Vivid Color</th> <th>Smart Color</th> <th>Edge Enhancement</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td colspan="5">IE and OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>IE_Low</td> <td>LEVEL_01</td> <td>LEVEL01</td> <td>RATIO_SEL01</td> <td>LEVEL_01</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>IE_Medium</td> <td>LEVEL_02</td> <td>LEVEL02</td> <td>RATIO_SEL02</td> <td>LEVEL_02</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>IE_High</td> <td>LEVEL_03</td> <td>LEVEL03</td> <td>RATIO_SEL03</td> <td>LEVEL_03</td> </tr> </tbody> </table>											CABC_COND[1 : 0]		Function	0	0	Off (Default)	0	1	User Interface Image (UI-Mode)	1	0	Still Picture Image (Still-Mode)	1	1	Moving Image (Moving-Mode)	IMAGE_ENHANCEMENT[3:0]				IE Level	Smart Contrast	Vivid Color	Smart Color	Edge Enhancement	0	0	0	0	IE and OFF					1	0	0	0	IE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	LEVEL_01	1	0	0	1	IE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	LEVEL_02	1	0	1	1	IE_High	LEVEL_03	LEVEL03	RATIO_SEL03	LEVEL_03
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Restriction	- This register is synchronized with V-sync by internal circuit.																																																																						
Register Availability	Status		Availability																																																																				
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RDCABC (56h): Read Content Adaptive Brightness Control (CABC) Mode

Address (MDDI I/F)		5600h					Access Attribute				R
Address (Other I/F)		56h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5600h	Parameter 1	00h	IMAGE_ENHANCEMENT [3:0]				0	0	CABC_COND[1 : 0]		00h

Description	<p>- This command is used to "read" the CABC operation mode. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1"> <thead> <tr> <th colspan="2">CABC_COND[1 : 0]</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off (Default)</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image (UI-Mode)</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture Image (Still-Mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image (Moving-Mode)</td> </tr> </tbody> </table> <p>- Image Enhancement (IE) read by IMAGE_ENHANCEMENT [3:0] as below table.</p> <table border="1"> <thead> <tr> <th colspan="4">IMAGE_ENHANCEMENT[3:0]</th> <th>IE Level</th> <th>Smart Contrast</th> <th>Vivid Color</th> <th>Smart Color</th> <th>Edge Enhancement</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td colspan="5">IE and OFF</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>IE_Low</td> <td>LEVEL_01</td> <td>LEVEL01</td> <td>RATIO_SEL01</td> <td>LEVEL_01</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>IE_Medium</td> <td>LEVEL_02</td> <td>LEVEL02</td> <td>RATIO_SEL02</td> <td>LEVEL_02</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>IE_High</td> <td>LEVEL_03</td> <td>LEVEL03</td> <td>RATIO_SEL03</td> <td>LEVEL_03</td> </tr> </tbody> </table>											CABC_COND[1 : 0]		Function	0	0	Off (Default)	0	1	User Interface Image (UI-Mode)	1	0	Still Picture Image (Still-Mode)	1	1	Moving Image (Moving-Mode)	IMAGE_ENHANCEMENT[3:0]				IE Level	Smart Contrast	Vivid Color	Smart Color	Edge Enhancement	0	0	0	0	IE and OFF					1	0	0	0	IE_Low	LEVEL_01	LEVEL01	RATIO_SEL01	LEVEL_01	1	0	0	1	IE_Medium	LEVEL_02	LEVEL02	RATIO_SEL02	LEVEL_02	1	0	1	1	IE_High	LEVEL_03	LEVEL03	RATIO_SEL03	LEVEL_03
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	S/W Reset					00h																																																																	
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WRCABCMB (5Eh): Write CABc Minimum Brightness

Address (MDDI I/F)		5E00h					Access Attribute				W
Address (Other I/F)		5Eh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5E00h	Parameter 1	00h	CMB[7 : 0]							00h	

Description	<p>- This command is used to set the minimum brightness value of the display for CABc function.</p> <p>00h value means the lowest brightness for CABc and FFh value means the highest brightness for CABc.</p>													
	Restriction -													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Sleep In	Yes													
Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
	Status	Default Value												
	Power On Sequence	00h												
S/W Reset	00h													
H/W Reset	00h													

RDCABCMB (5Fh): Read CABC Minimum Brightness

Address (MDDI I/F)		5F00h					Access Attribute				R
Address (Other I/F)		5Fh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
5F00h	Parameter 1	00h	CMB[7 : 0]								00h

Description	<p>- This command is used to “read” the minimum brightness value of the display for CABC function.</p> <p>00h value means the lowest brightness for Full-ABC (CABC + LABC) and FFh value means the highest brightness for CABC.</p>												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

RDDSDR (68h): Read Display Self-Diagnostic Result

Address (MDDI I/F)		6800h						Access Attribute			R
Address (Other I/F)		68h						Number of Parameter(s)			1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
6800h	Parameter 1	00h	D7	D6	D5	D4	D3	D2	D1	D0	00h

Description	<ul style="list-style-type: none"> - This command indicates the status of the display self-diagnostic results after Sleep Out. This command is described in the table below. - The inverse of checksum compare will output to GPIO pin when select this function. Normally GPIO pin remains high, when ESD occurs leads to checksum comparison fail, it will output low pulse or keep low to notify the ESD alarm to host. 																																			
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th colspan="2">Value</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Register Loading Detection</td> <td colspan="2">See section "Register Loading Detection"</td> </tr> <tr> <td>D6</td> <td>Functionality Detection</td> <td colspan="2">See section "Functionality Detection"</td> </tr> <tr> <td>D5</td> <td>Chip Attachment Detection</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D4</td> <td>Display Glass Break Detection</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D3</td> <td>Not Used</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D2</td> <td>Not Used</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D1</td> <td>Not Used</td> <td>"0" (Not used)</td> <td></td> </tr> <tr> <td>D0</td> <td>Checksums Compare</td> <td>"1"=Checksums are not same</td> <td>"0"=Checksums are same (Default)</td> </tr> </tbody> </table>	Bit	Description	Value		D7	Register Loading Detection	See section "Register Loading Detection"		D6	Functionality Detection	See section "Functionality Detection"		D5	Chip Attachment Detection	"0" (Not used)		D4	Display Glass Break Detection	"0" (Not used)		D3	Not Used	"0" (Not used)		D2	Not Used	"0" (Not used)		D1	Not Used	"0" (Not used)		D0	Checksums Compare	"1"=Checksums are not same
Bit	Description	Value																																		
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D0	Checksums Compare	"1"=Checksums are not same	"0"=Checksums are same (Default)																																	
Restriction	- It will be necessary to wait 300ms after there is the last write access on DCS area registers before there can read Bit D0 value.																																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
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SET_MDDI (8Fh)

Address (MDDI I/F)		8F00h					Access Attribute				R/W
Address (Other I/F)		8Fh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
8F00h	Parameter 1	00h	0	0	0	0	0	0	0	MDDI_I	01h

Description	- MDDI output current selection.												
	<table border="1"> <thead> <tr> <th>MDDI_I</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>3.5mA (MDDI 1.0)</td> </tr> <tr> <td>1(default)</td> <td>2.0mA (MDDI 1.2)</td> </tr> </tbody> </table>	MDDI_I	Function Description	0	3.5mA (MDDI 1.0)	1(default)	2.0mA (MDDI 1.2)						
	MDDI_I	Function Description											
0	3.5mA (MDDI 1.0)												
1(default)	2.0mA (MDDI 1.2)												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	01h												
S/W Reset	01h												
H/W Reset	01h												

RDDDBS (A1h): Read DDB Start

Address (MDDI I/F)		A100h ~ A104h					Access Attribute				R
Address (Other I/F)		A1h					Number of Parameter(s)				5
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
A100h	Parameter 1	00h	SID[7 : 0]								N/A
A101h	Parameter 2	00h	SID[15 : 8]								N/A
A102h	Parameter 3	00h	MRID[7 : 0]								N/A
A103h	Parameter 4	00h	MRID[15 : 8]								N/A
A104h	Parameter 5	00h	FFh								FFh

Description	<p>-This command returns the supplier identification and display module mode/revision information.</p> <p>Note: This information is not the same what “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)” commands are returning.</p> <p>SID[7:0]: LCD module’s manufacturer ID. SID[15:8]: LCD module/driver version ID MRID[7:0]: LCD module/driver ID MRID[15:8]: IC version code FFh : Exit code – there is no more data in the Descriptor Block</p> <p>This read sequence can be interrupted by any command and it can be continued by “Read DDB Continue (A8h)” command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.</p>
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Restriction	-
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Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #4a7ebb; color: white;">Status</th> <th style="background-color: #4a7ebb; color: white;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												

Default Value	<p>A100h ~ A103h:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #4a7ebb; color: white;">Status</th> <th style="background-color: #4a7ebb; color: white;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">N/A</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">N/A</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">N/A</td> </tr> </tbody> </table> <p>A104h:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #4a7ebb; color: white;">Status</th> <th style="background-color: #4a7ebb; color: white;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">FFh</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">FFh</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">FFh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A	Status	Default Value	Power On Sequence	FFh	S/W Reset	FFh	H/W Reset	FFh
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Status	Default Value																
Power On Sequence	FFh																
S/W Reset	FFh																
H/W Reset	FFh																

RDDDBC (A8h): Read DDB Continue

Address (MDDI I/F)		A800h ~ A806h					Access Attribute				R	
Address (Other I/F)		A8h					Number of Parameter(s)				7	
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value	
A800h	Parameter 1	00h	SID[7 : 0]									N/A
A801h	Parameter 2	00h	SID[15 : 8]									N/A
A802h	Parameter 3	00h	MRID[7 : 0]									N/A
A803h	Parameter 4	00h	MRID[15 : 8]									N/A
A804h	Parameter 5	00h	FFh									FFh

Description	-A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.																
Restriction	- SPI IF don't support continue read.																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																
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Default Value	<p>A800h ~ A803h:</p> <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table> <p>A804h:</p> <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>FFh</td> </tr> <tr> <td>S/W Reset</td> <td>FFh</td> </tr> <tr> <td>H/W Reset</td> <td>FFh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A	Status	Default Value	Power On Sequence	FFh	S/W Reset	FFh	H/W Reset	FFh
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Status	Default Value																
Power On Sequence	FFh																
S/W Reset	FFh																
H/W Reset	FFh																

RDFCS (AAh): Read First Checksum

Address (MDDI I/F)		AA00h					Access Attribute				R
Address (Other I/F)		AAh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
AA00h	Parameter 1	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00h

Description	- This command returns the first checksum what has been calculated from System function registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	<p>(1) It will be necessary to wait 150 ms after there is the last write access on System function registers before there can read this checksum value.</p> <p>(2) The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

MDDI_WAKE_TOGGLE (ADh): MDDI VSYNC BASED LINK WAKE-UP

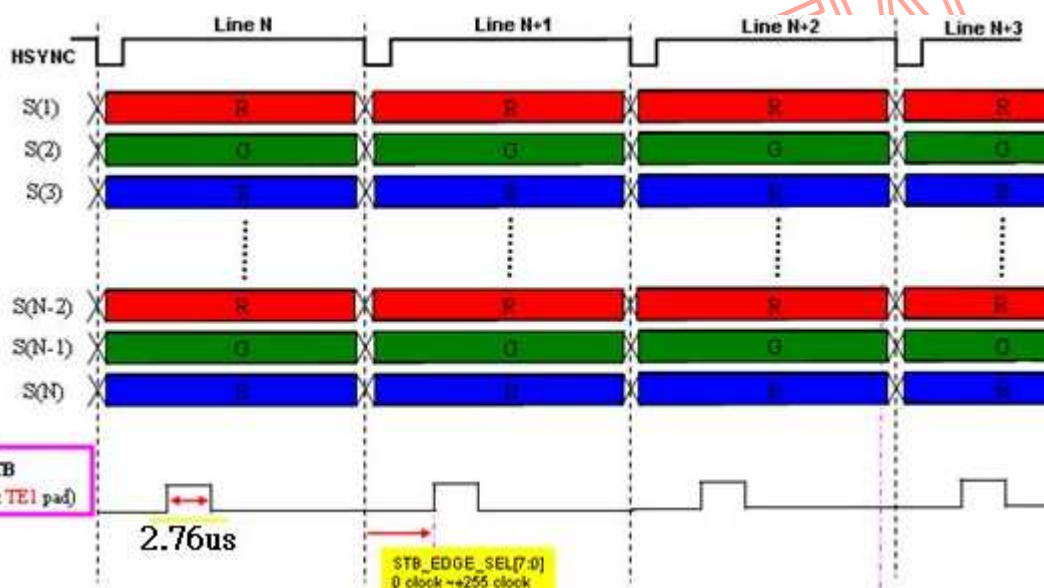
Address (MDDI I/F)		AD00h					Access Attribute			W
Address (Other I/F)		ADh					Number of Parameter(s)			0
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	No Argument									

Description	<p>- This register enables the Vsync based Link wakeup in Client for MDDI interface. After the host brings the link out of hibernation, this register is cleared. Detail please refer to Vsync Based Link Wakeup section.</p> <p>- Vsync based Link wakeup function is turned on when 0xAD00 is written, no matter "with" or "without" parameter.</p>												
Restriction													
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Status	Default Status												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

STB EDGE POSITION (AEh)

Address (MDDI I/F)		AE00h					Access Attribute				R/W
Address (Other I/F)		AEh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
AE00h	Parameter 1	00h	STB_EDGE_SEL[7:0]								00h

-It is used to set a rising edge position of STB signal that refers to the falling edge of Display HSYNC. Its minimum adjusted step is one display clock period (around 230ns). STB signal is repeated at per line except VBP/VFP region and outputs from TE1 pad. It can be enable or disable by MTP register B3h of CMD2 Page0 (bit "LPM_HZ" is 0; and bit "TE1_ON" is 1).



Description

STB_EDGE_SEL[7:0]	Adjusted STB rising edge position
00h	Aligned to the falling edge of HSYNC
01h	+1
02h	+2
:	:
:	:
80h	+128
:	:
:	:
FFh	+255

Note:

1. In above table, "+" index that STB rising edge is set to lag the falling edge of Display HSYNC.
2. The unit of "Adjusted STB rising edge position" is number of Display Clock.

Restriction

-

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default Value	AE00h:			
	Status		Default Value	
	Power On Sequence		00h	
	S/W Reset		00h	
	H/W Reset		00h	

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RDCCS (AFh): Read Continue Checksum

Address (MDDI I/F)		AF00h					Access Attribute				R
Address (Other I/F)		AFh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
AF00h	Parameter 1	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00h

Description	- This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from System function registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	<p>(1) It will be necessary to wait 300 ms after there is the last write access on System function registers before there can read this checksum value in the first time.</p> <p>(2) The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

RDID1 (DAh): Read ID1

Address (MDDI I/F)		DA00h					Access Attribute				R
Address (Other I/F)		DAh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DA00h	Parameter 1	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	N/A

Description	- This read byte identifies the display module's manufacturer.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Default Value	DA00h: <table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													

RDID2 (DBh): Read ID2

Address (MDDI I/F)		DB00h					Access Attribute				R
Address (Other I/F)		DBh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DB00h	Parameter 1	00h	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	N/A

Description	- This read byte is used to track the display module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:												
	<table border="1"> <thead> <tr> <th>ID Byte Value</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr> <td>80h</td> <td>Version1</td> <td>:</td> </tr> <tr> <td>81h</td> <td>Version2</td> <td>:</td> </tr> <tr> <td>82h</td> <td>Version3</td> <td>:</td> </tr> </tbody> </table>	ID Byte Value	Version	Changes	80h	Version1	:	81h	Version2	:	82h	Version3	:
ID Byte Value	Version	Changes											
80h	Version1	:											
81h	Version2	:											
82h	Version3	:											
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
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Status	Default Value												
Power On Sequence	N/A												
S/W Reset	N/A												
H/W Reset	N/A												

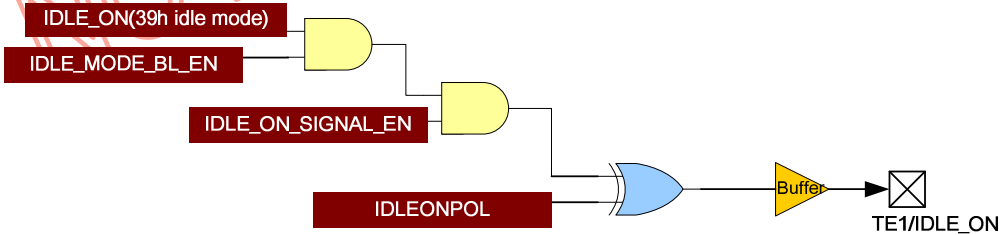
RDID3 (DCh): Read ID3

Address (MDDI I/F)		DC00h					Access Attribute				R
Address (Other I/F)		DCh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DC00h	Parameter 1	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	N/A

Description	- This read byte identifies the display module / driver.												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Value												
Power On Sequence	N/A												
S/W Reset	N/A												
H/W Reset	N/A												

IDLEMODE_BL_Control (E1h): Write IDLEMODE_BL_Control

Address (MDDI I/F)		E100h		Access Attribute							W
Address (Other I/F)		E1h		Number of Parameter(s)							1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E100h	Parameter 1	00h	0	0	0	0	0	0	IDLE_ON_SIGNAL_EN	IDLE_MODE_BL_EN	00h

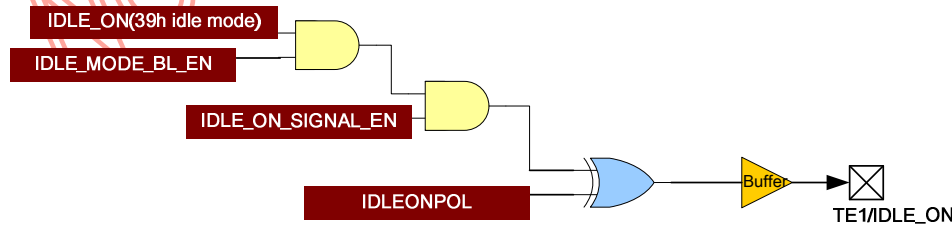
Description	<p>- The content of the register IDLEMODE_BL_control will define the functionality of the transmissive LCD display backlight behavior in idle mode which is enabled by command IDMON (39h). In this mode, the backlight power consumption will be reduced with several methods.</p> <p>IDLE_ON_SIGNAL_EN: This bits controls the HW signal called IDLE_ON, which is wired from display to handset backlight drive. This bits can be used to dim handset backlight DC drive current in the idle mode. Note that display BC output will be still controllable by the register Write Display Brightness.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>IDLE_ON_SIGNAL_EN</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>output signal IDLE_ON is disabled and set to GND</td> </tr> <tr> <td style="text-align: center;">1</td> <td>output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).</td> </tr> </tbody> </table> <p style="color: red;">※The idle on signal should toggle state upon falling edge of the BC signal.</p> <p>IDLE_MODE_BL_EN:</p> <p>0 = Entering idle mode using command IDMON has no effect to display backlight behavior. Backlight control is controlled by Write Display Brightness (51h) and Write CTRL Display (53h) registers.</p> <p>1 = Entering the idle mode will cause display to enter into idle mode specific backlight state defined by IDLE_ON_SIGNAL_EN bit.</p> <div style="text-align: center;">  </div>	IDLE_ON_SIGNAL_EN	Function	0	output signal IDLE_ON is disabled and set to GND	1	output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).						
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Restriction	-												
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Default Value	E100h:								
	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></tbody></table>	Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A
	Status	Default Value							
	Power On Sequence	N/A							
S/W Reset	N/A								
H/W Reset	N/A								

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IDLEMODE_BL_Control (E2h): Read IDLEMODE_BL_Control

Address (MDDI I/F)		E200h									Access Attribute		R
Address (Other I/F)		E2h									Number of Parameter(s)		1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value		
E200h	Parameter 1	00h	0	0	0	0	0	0	IDLE_ON_SIGNAL_EN	IDLE_MODE_BL_EN	00h		

Description	<p>- The content of the register IDLEMODE_BL_control will define the functionality of the transmissive LCD display backlight behavior in idle mode which is enabled by command IDMON (39h). In this mode, the backlight power consumption will be reduced with several methods.</p> <p>IDLE_ON_SIGNAL_EN: This bits controls the HW signal called IDLE_ON, which is wired from display to handset backlight drive. This bits can be used to dim handset backlight DC drive current in the idle mode. Note that display BC output will be still controllable by the register Write Display Brightness.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th>IDLE_ON_SIGNAL_EN</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>output signal IDLE_ON is disabled and set to GND</td> </tr> <tr> <td style="text-align: center;">1</td> <td>output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).</td> </tr> </tbody> </table> <p>※The idle on signal should toggle state upon falling edge of the BC signal.</p> <p>IDLE_MODE_BL_EN:</p> <p>0 = Entering idle mode using command IDMON has no effect to display backlight behavior. Backlight control is controlled by Write Display Brightness (51h) and Write CTRL Display (53h) registers.</p> <p>1 = Entering the idle mode will cause display to enter into idle mode specific backlight state defined by IDLE_ON_SIGNAL_EN bit.</p> <div style="text-align: center;">  </div>											IDLE_ON_SIGNAL_EN	Function	0	output signal IDLE_ON is disabled and set to GND	1	output signal IDLE_ON is enabled and set to logical high when idle mode is entered. (Logical high means VDDI).						
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Sleep In	Yes																						
Default Value	<p>E200h:</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr style="background-color: #4a7ebb; color: white;"> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
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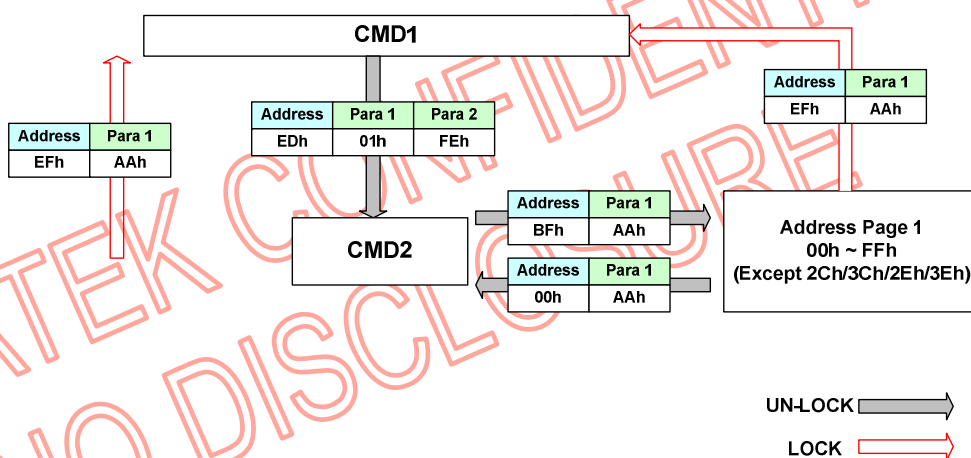
PAGE_CTRL (EDh) : Unlock CMD2

Address (MDDI I/F)		ED00h ~ ED01h					Access Attribute				W
Address (Other I/F)		EDh					Number of Parameter(s)				2
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
ED00h	Parameter 1	0	0	0	0	0	0	0	0	1	01h
ED01h	Parameter 2	0	1	1	1	1	1	1	1	0	FEh

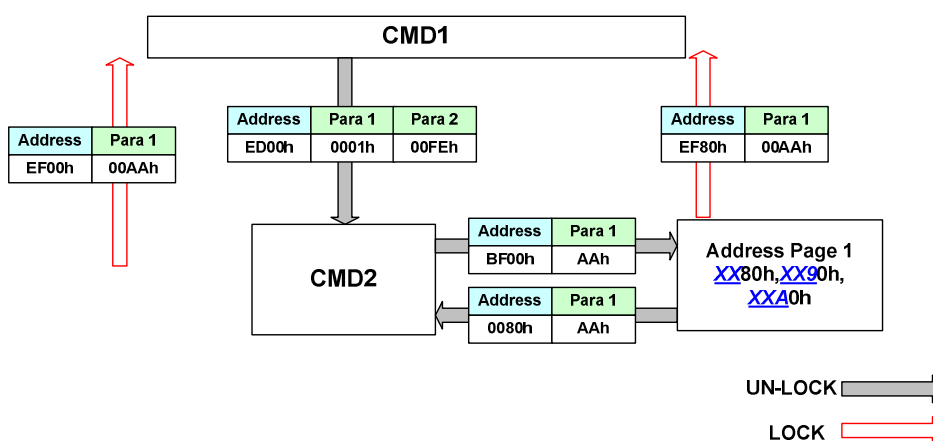
This command is used for UNLOCK of CMD2.

Note : After hardware reset or software reset input, the input of Driver Function command is locked.

Register structure for CPU80 / 86, SPI and MIPI interface



Register structure for MDDI interface



Description

Restriction

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
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Status	Default Value (ED00h)	Default Value (ED01h)												
Default Value														

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PAGE_STATUS (FFh) : PAGE unlock status

Address (MDDI I/F)		FF00h					Access Attribute				R
Address (Other I/F)		FFh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
-	Parameter 1	-	0	0	0	0	0	CMD2_P1	CMD2_P0	CMD1	01h

Description	- This command is used for checking the current CMD accessing status (except MDDI I/F).												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value D[15 : 0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0001h</td> </tr> <tr> <td>S/W Reset</td> <td>0001h</td> </tr> <tr> <td>H/W Reset</td> <td>0001h</td> </tr> </tbody> </table>	Status	Default Value D[15 : 0]	Power On Sequence	0001h	S/W Reset	0001h	H/W Reset	0001h				
Status	Default Value D[15 : 0]												
Power On Sequence	0001h												
S/W Reset	0001h												
H/W Reset	0001h												

6.2 CMD2_P0 register list

Para	Addr.	R/W	Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Code	MTP
DISPLAY_CTRL	B0h	R/W	1	DSIN	-	PT1[1:0]		CRL	CTB	PT[1:0]		00h	V
PORCH_CTRL	B1h	R/W	1	BPAC[7:0]								1Ch	V
		R/W	2	BPB[7:0]								1Ch	V
		R/W	3	-	BPAC[8]	-	BPB[8]	FP[3:0]			04h	V	
FRAMERATE_CTRL	B2h	R/W	1	RTNA[7:0]								8Dh	V
		R/W	2	RTNB[7:0]								D3h	
		R/W	3	RTNC[7:0]								8Dh	
SPI&RGB IF SETTING	B3h	R/W	1	SDA_EN	BYPASS	LPM_HZ	TE1_ON	-	-	-	DM	20h	V
INVCTRL	B4h	R/W	1	-	-	NLC[1:0]		NLB[1:0]		NLA[1:0]		0Ch	V
PMTCTL Partial and Partial Idle Mode Timing Control	B5h	R/W	1	INCYLB[3:0]				INCYLC[3:0]				00h	V
		R/W	2	AVEE_NDISP_DIV	VGH_NDISP_DIV	VCL_NDISP_DIV	AVDD_NDISP_DIV			00h			
SOURCE EQ	B6h	R/W	1	-	-	-	SDT[4:0]				02h	V	
		R/W	2	-	-	-	EQI1[4:0]				08h		
		R/W	3	-	-	-	EQI2[4:0]				08h		
		R/W	4	-	-	-	EQG[4:0]				08h		
		R/W	5	-	-	-	SOE_S[4:0]				10h		
		R/W	6	-	-	-	SOE_W[5:0]				23h		
DISPLAY_CTRL 2	B7h	R/W	1	-	-	REV	SRGB	CTS	-	-	-	00h	V
MTP Selection	B8h	R/W	1	-	-	-	-	-	PTM[1:0]		MTP_W_GMA	00h	
CABC Control	BBh	R/W	1	-	-	-	-	-	SYNC_PWM_FR EQ[2:0]		00h	V	
PWR_CTRL1 ADJ GVDDP/N	C0h	R/W	1	-	VRHP[6:0]						44h	V	
		R/W	2	-	VRHN[6:0]						44h		
		R/W	3	-	VGSP[6:0]						10h		
		R/W	4	-	VGSN[6:0]						10h		
PWR_CTRL2 AVDD	C1h	R/W	1	-	CP1_MODE	PUMP_MODE[1:0]		-	BTP1CKA_EXT[2:0]			13h	V
		R/W	2	-	BTP1CKB_EXT[2:0]			-	BTP1CKC_EXT[2:0]			33h	
PWR_CTRL3 VGHL & VGL	C2h	R/W	1	-	VGHL_A[2:0]			-	VGHL_CLKA[2:0]			44h	V
		R/W	2	-	VGHL_B[2:0]			-	VGHL_CLKB[2:0]			44h	
		R/W	3	-	VGHL_C[2:0]			-	VGHL_CLKC[2:0]			44h	
PWR_CTRL5 (AVEE)	C3h	R/W	1	-	-	BTP5CKC_EXT[1:0]	BTP5CKB_EXT[1:0]	BTP5CKA_EXT[1:0]			2Ah	V	
PWR_CTRL6 VCOM	C4h	R/W	1	VMDC[7:0]								40h	V
PWR_CTRL6 VCOM	C5h	R/W	1	-	ISOPP[2:0]			BIAS_REDUCE	ISOPN[2:0]			4Ch	V
		R/W	2	-	SAPPA[2:0]			-	SAPNA[2:0]			44h	
		R/W	3	-	SAPPB[2:0]			-	SAPNB[2:0]			44h	
		R/W	4	-	SAPPC[2:0]			-	SAPNC[2:0]			44h	
PWR_CTRL6 VGHL&VGL CLAMP	C6h	R/W	4	-	-	-	-	-	-	VGHL_OFF	VGLCL_OFF	00h	V
				VGL_CLAMP_A[3:0]				VGHL_CLAMP_A[3:0]				E2h	V

				VGL_CLAMPB[3:0]				VGH_CLAMPB[3:0]				E2h	V
				VGL_CLAMPPC[3:0]				VGH_CLAMPPC[3:0]				E2h	V
WRID1	D1h	R/W	1	WID1[7]	WID1[6]	WID1[5]	WID1[4]	WID1[3]	WID1[2]	WID1[1]	WID1[0]	00h	V
WRID2	D2h	R/W	1	1	WID2[6]	WID2[5]	WID2[4]	WID2[3]	WID2[2]	WID2[1]	WID2[0]	80h	V
WRID3	D3h	R/W	1	WID3[7]	WID3[6]	WID3[5]	WID3[4]	WID3[3]	WID3[2]	WID3[1]	WID3[0]	00h	V
RDID4	D4h	R	1	0	0	0	0	0	0	0	1	01h	
		R	2	0	1	0	1	0	0	1	1	53h	
		R	3	0	0	0	1	0	0	0	0	10h	
		R	4	0	0	0	0	ID4[3]	ID4[2]	ID4[1]	ID4[0]	00h	
WRDDB	D5h	R/W	1	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	00h	V
		R/W	2	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	00h	
		R/W	3	MRID7	MRID6	MRID5	MRID4	MRID3	MRID2	MRID1	MID0	00h	
		R/W	4	MRID15	MRID14	MID13	MRID12	MRID11	MRID10	MRID9	MID8	00h	
RDVNT	DDh	R	1	NV_N3	NV_N2	NV_N1	NV_N0	NV_GMA	0	NVP_F	NV_P	00h	
EPR/W	DEh	R/W	1	0	1	0	1	0	1	0	1	55h	
		R/W	2	1	0	1	0	1	0	1	0	AAh	
		R/W	3	0	1	1	0	0	1	1	0	66h	
MTPWR	DFh	R/W	1	0	0	0	nROM	0	0	0	MTP_W	00h	
RDREGEXT1	EBh	R/W	1	Add7	Add6	Add5	Add4	Add3	Add2	Add1	Add0		
RDREGEXT2	ECh	R	1	Para17	Para16	Para15	Para14	Para13	Para12	Para11	Para10		
		R	2	Para27	Para26	Para25	Para24	Para23	Para22	Para21	Para20		
		:	:	:	:	:	:	:	:	:	:		
		R	N	ParaN7	ParaN6	ParaN5	ParaN4	ParaN3	ParaN2	ParaN1	ParaN0		
PAGE_CTRL Into CMD3	EEh	W	1	1	1	0	1	1	1	1	0	DEh	
		W	2	0	0	1	0	0	0	0	0	1	
PAGE_CTRL Lock CMD2	EFh	W	1	1	0	1	0	1	0	1	0	AAh	
PAGE_CTRL Into CMD2_P1	BFh	W	1	1	0	1	0	1	0	1	0	AAh	

DISPLAY_CTRL (B0h)

Address (MDDI I/F)		B000h					Access Attribute				R/W
Address (Other I/F)		B0h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
B000h	Parameter 1	0	DSIN	0	PT1[1:0]		CRL	CTB	PT[1:0]		00h

Description	<p>PT[1:0]: Source setting in non-display area at partial mode.</p> <table border="1"> <thead> <tr> <th>PT[1:0]</th> <th>Source (Positive/Negative)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>V63+/ V63-</td> </tr> <tr> <td>1</td> <td>V0+/V0-</td> </tr> <tr> <td>2</td> <td>VSSA/VSSA</td> </tr> <tr> <td>3</td> <td>Hi-Z</td> </tr> </tbody> </table> <p>PT1[1:0]: Source setting in porch area.</p> <table border="1"> <thead> <tr> <th>PT1[1:0]</th> <th>Source (Positive/Negative)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>V63+/ V63-</td> </tr> <tr> <td>1</td> <td>V0+/V0-</td> </tr> <tr> <td>2</td> <td>VSSA/VSSA</td> </tr> <tr> <td>3</td> <td>Hi-Z</td> </tr> </tbody> </table> <p>CTB: Gate Scan Direction Select</p> <table border="1"> <thead> <tr> <th>CTB</th> <th>Gate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>G0→G479</td> </tr> <tr> <td>1</td> <td>G479→G0</td> </tr> </tbody> </table> <p>CRL: Source Scan Direction Select</p> <table border="1"> <thead> <tr> <th>CRL</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>S0→S959</td> </tr> <tr> <td>1</td> <td>S959→S0</td> </tr> </tbody> </table> <p>DSIN : This command is use to power on/ off the SRAM at SLP_IN mode to prevent current leakage.</p> <table border="1"> <thead> <tr> <th>DSIN</th> <th>Power ON / OFF</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Power ON SRAM at SLP_IN Mode (Default)</td> </tr> <tr> <td>1h</td> <td>Power OFF SRAM at SLP_IN Mode</td> </tr> </tbody> </table> <p><i>Note : If SRAM is powered off in SLP-IN mode, the leakage current can be reduced but the SRAM data will be lost. Also either read or write SRAM is NOT possible.</i></p>											PT[1:0]	Source (Positive/Negative)	0	V63+/ V63-	1	V0+/V0-	2	VSSA/VSSA	3	Hi-Z	PT1[1:0]	Source (Positive/Negative)	0	V63+/ V63-	1	V0+/V0-	2	VSSA/VSSA	3	Hi-Z	CTB	Gate	0	G0→G479	1	G479→G0	CRL	Source	0	S0→S959	1	S959→S0	DSIN	Power ON / OFF	0h	Power ON SRAM at SLP_IN Mode (Default)	1h	Power OFF SRAM at SLP_IN Mode
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	Sleep In						Yes																																										

Default Value	Status		Default Value D[7 : 0]	
	Power On Sequence			00h
	S/W Reset			00h
	H/W Reset			00h

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PORCH_CTRL: Front & Back Porch Setting (B1h)

Address (MDDI I/F)		B100h ~ B101h					Access Attribute				R/W	
Address (Other I/F)		B1h					Number of Parameter(s)				3	
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value	
B100h	Parameter 1	0	BPAC[7 : 0]									1Ch
B101h	Parameter 2	0	BPB[7 : 0]									1Ch
B102h	Parameter 3	0	0	BPAC[8]	0	BPB[8]	FP[3:0]				04h	

Description	<p>BPAC[9:0] : Determines the number of lines for internal display back porch period (in normal mode and idle mode).</p> <p style="text-align: center;">Number of Lines for Internal Display Back Porch</p> <table border="1"> <thead> <tr> <th>BPAC[8:0]</th> <th>Back Porch period(Line periods)</th> </tr> </thead> <tbody> <tr><td>000h</td><td>Setting Inhibited</td></tr> <tr><td>001h</td><td>1 lines</td></tr> <tr><td>002h</td><td>2 lines</td></tr> <tr><td>003h</td><td>3 lines</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>01Ch</td><td>28lines(Default)</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1FFh</td><td>511lines</td></tr> </tbody> </table>	BPAC[8:0]	Back Porch period(Line periods)	000h	Setting Inhibited	001h	1 lines	002h	2 lines	003h	3 lines	:	:	01Ch	28lines(Default)	:	:	1FFh	511lines
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<p>BPB[9:0] : Determines the number of lines for internal display back porch period (in partial mode).</p> <p style="text-align: center;">Number of Lines for Internal Display Back Porch</p> <table border="1"> <thead> <tr> <th>BPB[8:0]</th> <th>Back Porch period(Line periods)</th> </tr> </thead> <tbody> <tr><td>000h</td><td>Setting Inhibited</td></tr> <tr><td>001h</td><td>1 lines</td></tr> <tr><td>002h</td><td>2 lines</td></tr> <tr><td>003h</td><td>3 lines</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>01Ch</td><td>28lines(Default)</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1FFh</td><td>511lines</td></tr> </tbody> </table>	BPB[8:0]	Back Porch period(Line periods)	000h	Setting Inhibited	001h	1 lines	002h	2 lines	003h	3 lines	:	:	01Ch	28lines(Default)	:	:	1FFh	511lines	
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<p>FP[3:0] : Determines the number of lines for internal display front porch period (a blank period at the end of display).</p> <p style="text-align: center;">Number of Lines for Internal Display Front Porch</p> <table border="1"> <thead> <tr> <th>FP[3:0]</th> <th>Back Porch period(Line periods)</th> </tr> </thead> <tbody> <tr><td>0000</td><td>Setting Inhibited</td></tr> <tr><td>0001</td><td>1 lines</td></tr> <tr><td>0010</td><td>2 lines</td></tr> <tr><td>0011</td><td>3 lines</td></tr> <tr><td>0100</td><td>4 lines(Default)</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>15 lines</td></tr> </tbody> </table>	FP[3:0]	Back Porch period(Line periods)	0000	Setting Inhibited	0001	1 lines	0010	2 lines	0011	3 lines	0100	4 lines(Default)	:	:	:	:	1111	15 lines	
FP[3:0]	Back Porch period(Line periods)																		
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1111	15 lines																		

Restriction																	
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Power On Sequence	1Ch	1Ch	04h														
S/W Reset	1Ch	1Ch	04h														
H/W Reset	1Ch	1Ch	04h														

FRAMERATE_CTRL (B2h)

Address (MDDI I/F)		B200h ~ B202h					Access Attribute				R/W	
Address (Other I/F)		B2h					Number of Parameter(s)				3	
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value	
B200h	Parameter 1	0	RTNA[7 : 0]									8Dh
B201h	Parameter 2	0	RTNB[7 : 0]									D3h
B202h	Parameter 3	0	RTNC[7 : 0]									8Dh

Description	<p>RTNA[7 : 0] : Frame rate control in full colors normal mode (Normal mode on) RTNB[7 : 0] : Frame rate control in Idle mode (Idle mode on) RTNC[7 : 0] : Frame rate control in full colors Partial mode (Partial mode on / Idle mode off)</p> <p>- RTNA[7 : 0] / RTNB[7 : 0] / RTNC[7 : 0] are used to determine the 1H (line) period when NT35310 is under internal clock synchronized display operation.</p> <p>- The RTNA[7 : 0] / RTNB[7 : 0] / RTNC[7 : 0] are set depending on the panel resolution for frame rate adjustment. The following table is the setting example of RTNA[7 : 0] / RTNB[7 : 0] / RTNC[7 : 0] for different panel resolutions according to the frame frequency calculation formula below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>H Line no.</th> <th>RTNA/B/C [7:0]</th> <th>Fosc (MHz)</th> <th>BP + FP</th> <th>Frame rate (Hz)</th> </tr> </thead> <tbody> <tr> <td>480</td> <td>141</td> <td>13</td> <td>32</td> <td>60</td> </tr> </tbody> </table> <p>Note: Default value for Normal mode and Partial mode</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>H Line no.</th> <th>RTNA/B/C [7:0]</th> <th>Fosc (MHz)</th> <th>BP + FP</th> <th>Frame rate (Hz)</th> </tr> </thead> <tbody> <tr> <td>480</td> <td>211</td> <td>13</td> <td>32</td> <td>40</td> </tr> </tbody> </table> <p>Note: Default value for Idle mode</p> $\text{FrameRate} = \frac{\text{Fosc} / 3}{\text{RTN} * (\text{Line} + \text{BP} + \text{FP})} \text{Hz}$ <p>- The frame frequency can be changed by modifying the RTNA[7 : 0] / RTNB[7 : 0] / RTNC[7 : 0] setting. - Make sure to set the proper frame frequency whenever the number of lines to drive the liquid crystal panel is changed.</p>	H Line no.	RTNA/B/C [7:0]	Fosc (MHz)	BP + FP	Frame rate (Hz)	480	141	13	32	60	H Line no.	RTNA/B/C [7:0]	Fosc (MHz)	BP + FP	Frame rate (Hz)	480	211	13	32	40
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Clocks in 1H Period (Internal clock Operation, unit: DCK)																			
Description	RTN[8 : 0]	Clocks per Line	RTN[8 : 0]	Clocks per Line		RTN[8 : 0]	Clocks per Line												
		000h	Reserved	076h	Reserved	0A5h	165	0D4h	212										
	001h	Reserved	077h	Reserved	0A6h	166	0D5h	213											
	:	:	078h	Reserved	0A7h	167	0D6h	214											
	:	:	079h	Reserved	0A8h	168	0D7h	215											
	:	:	07Ah	Reserved	0A9h	169	0D8h	216											
	04Ch	Reserved	07Bh	123	0AAh	170	0D9h	217											
	04Dh	Reserved	07Ch	124	0ABh	171	0DAh	218											
	04Eh	Reserved	07Dh	125	0ACh	172	0DBh	219											
	04Fh	Reserved	07Eh	126	0ADh	173	0DCh	220											
	050h	Reserved	07Fh	127	0AEh	174	0DDh	221											
	051h	Reserved	080h	128	0AFh	175	0DEh	222											
	052h	Reserved	081h	129	0B0h	176	0DFh	223											
	053h	Reserved	082h	130	0B1h	177	0E0h	224											
	054h	Reserved	083h	131	0B2h	178	0E1h	225											
	055h	Reserved	084h	132	0B3h	179	0E2h	226											
	056h	Reserved	085h	133	0B4h	180	0E3h	227											
	057h	Reserved	086h	134	0B5h	181	0E4h	228											
	058h	Reserved	087h	135	0B6h	182	0E5h	229											
	059h	Reserved	088h	136	0B7h	183	0E6h	230											
	05Ah	Reserved	089h	137	0B8h	184	0E7h	231											
	05Bh	Reserved	08Ah	138	0B9h	185	0E8h	232											
	05Ch	Reserved	08Bh	139	0BAh	186	0E9h	233											
	05Dh	Reserved	08Ch	140	0BBh	187	0EAh	234											
	05Eh	Reserved	08Dh	141	0BCh	188	0EBh	235											
	05Fh	Reserved	08Eh	142	0BDh	189	0ECh	236											
	060h	Reserved	08Fh	143	0BEh	190	0EDh	237											
	061h	Reserved	090h	144	0BFh	191	0EEh	238											
	062h	Reserved	091h	145	0C0h	192	0EFh	239											
	063h	Reserved	092h	146	0C1h	193	0F0h	240											
	064h	Reserved	093h	147	0C2h	194	0F1h	241											
	065h	Reserved	094h	148	0C3h	195	0F2h	242											
	066h	Reserved	095h	149	0C4h	196	0F3h	243											
	067h	Reserved	096h	150	0C5h	197	0F4h	244											
	068h	Reserved	097h	151	0C6h	198	0F5h	245											
	069h	Reserved	098h	152	0C7h	199	0F6h	246											
	06Ah	Reserved	099h	153	0C8h	200	0F7h	247											
	06Bh	Reserved	09Ah	154	0C9h	201	0F8h	248											
	06Ch	Reserved	09Bh	155	0CAh	202	0F9h	249											
	06Dh	Reserved	09Ch	156	0CBh	203	0FAh	250											
	06Eh	Reserved	09Dh	157	0CCh	204	0FBh	251											
	06Fh	Reserved	09Eh	158	0CDh	205	0FCh	252											
	070h	Reserved	09Fh	159	0CEh	206	0FDh	253											
	071h	Reserved	0A0h	160	0CFh	207	0FEh	254											
	072h	Reserved	0A1h	161	0D0h	208	0FFh	255											
	073h	Reserved	0A2h	162	0D1h	209													
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Partial Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		

Default Value	B200h:	<table border="1"> <thead> <tr> <th style="background-color: #000080; color: white;">Status</th> <th style="background-color: #000080; color: white;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8Dh</td> </tr> <tr> <td>S/W Reset</td> <td>8Dh</td> </tr> <tr> <td>H/W Reset</td> <td>8Dh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	8Dh	S/W Reset	8Dh	H/W Reset	8Dh
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SPI&RGB IF SETTING (B3h): SPI&RGB INTERFACE SETTING

Address (MDDI I/F)	B300h						Access Attribute			W/R
Address (Other I/F)	B3h						Number of Parameter(s)			1
	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Status
Parameter	-	SDA_EN	BYPASS	LPM_HZ	TE1_ON	0	0	0	DM	20h

Description	<p>-This command is used to set RGB interface related register.</p> <p>DM bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock,VSYNC, or RGB signal.</p> <table border="1"> <thead> <tr> <th>DM</th> <th>Display Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Internal oscillation clock</td> </tr> <tr> <td>1</td> <td>RGB Interface</td> </tr> </tbody> </table> <p>BYPASS: Select the display data pathe whether memory or direct to display in RGB interface.</p> <table border="1"> <thead> <tr> <th>BYPASS</th> <th>Interface Select</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Memory</td> </tr> <tr> <td>1</td> <td>Direction to display</td> </tr> </tbody> </table> <p>SDA_EN: 3/4 wire serial interface selection SDA_EN = "0", DIN and DOUT pins are used for 3/4 wire serial interface. SDA_EN = "1", DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used.</p> <table border="1"> <thead> <tr> <th>SDA_EN</th> <th>Input Pin</th> <th>Output Pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SDA</td> <td>Dout</td> </tr> <tr> <td>1</td> <td>SDA</td> <td>SDA</td> </tr> </tbody> </table> <p>LPM_HZ: Used with TE1_ON.</p> <table border="1"> <thead> <tr> <th>LPM_HZ</th> <th>TE1_ON</th> <th>TE1/IDLE_ON</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LPM function (Control by E1h)</td> </tr> <tr> <td>0</td> <td>1</td> <td>TE1 output</td> </tr> <tr> <td>1</td> <td>X</td> <td>Hiz</td> </tr> </tbody> </table>	DM	Display Mode	0	Internal oscillation clock	1	RGB Interface	BYPASS	Interface Select	0	Memory	1	Direction to display	SDA_EN	Input Pin	Output Pin	0	SDA	Dout	1	SDA	SDA	LPM_HZ	TE1_ON	TE1/IDLE_ON	0	0	LPM function (Control by E1h)	0	1	TE1 output	1	X	Hiz
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INVCTRL (B4h): Inversion Control

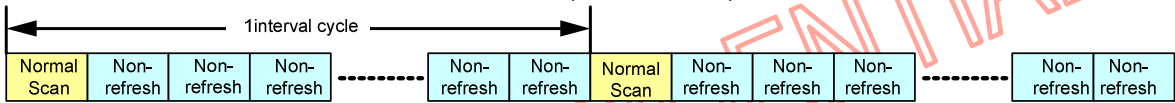
Address (MDDI I/F)		B400h					Access Attribute				R/W
Address (Other I/F)		B4h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
B400h	Parameter 1	0	0	0	NLC[1:0]		NLB[1:0]		NLA[1:0]		0Ch

Description	Display inversion mode set NLA: Inversion setting in full colors normal mode (Normal mode on) NLB: Inversion setting in Idle mode (Idle mode on) NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)													
	<table border="1"> <thead> <tr> <th>NLA / NLB / NLC [1:0]</th> <th>Inversion</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1dot inversion</td> </tr> <tr> <td>1</td> <td>2dot inversion</td> </tr> <tr> <td>2</td> <td>4dot inversion</td> </tr> <tr> <td>3</td> <td>column inversion</td> </tr> </tbody> </table>		NLA / NLB / NLC [1:0]	Inversion	0	1dot inversion	1	2dot inversion	2	4dot inversion	3	column inversion		
NLA / NLB / NLC [1:0]	Inversion													
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Power On Sequence	0Ch													
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H/W Reset	0Ch													

PMTCTL (B5h) : Partial and Idle Mode Timing Control

Address (MDDI I/F)		B500h~B501h					Access Attribute				R/W
Address (Other I/F)		B5h					Number of Parameter(s)				2
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
B500h	Parameter 1	0	INCYLB[3:0]			INCYLC[3:0]				00h	
B501h	Parameter 2	0	AVEE_NDISP_DIV	VGH_NDISP_DIV	VCL_NDISP_DIV	AVDD_NDISP_DIV				00h	

Interval Partial Mode: To achieve lower power driving, non-refresh frame frequency should be able to set lower than normal refresh (Normal Frame).



INTCYLC[3 : 0] : This command is use to set interval cycle frames in partial mode.

INTCYLC[3 : 0]	Interval Cycle Frame
0000	Normal Refresh
0001	Normal Refresh
0010	3
0011	5
0100	7
:	:
:	:
1111	29

Note: When INTCYLC[3:0] = 4'h0 means scan by normal partial mode

INCYLB[3 : 0] : This command is use to set interval cycle frames in idle mode.

INCYLB[3 : 0]	Interval Cycle Frame
0000	Normal Refresh
0001	Normal Refresh
0010	3
0011	5
0100	7
:	:
:	:
1111	29

Note: When INCYLB[3:0] = 4'h0 means scan by idle mode

AVEE_NDISP_DIV: Set the operating frequency of the step-up circuit2(AVEE) in non-refresh status.
VGH_NDISP_DIV: Set the operating frequency of the step-up circuit2(VGH) in non-refresh status.
VCL_NDISP_DIV: Set the operating frequency of the step-up circuit2(VCL) in non-refresh status.
AVDD_NDISP_DIV: Set the operating frequency of the step-up circuit2(AVDD) in non-refresh status.

	<table border="1"> <thead> <tr> <th> AVEE_NDISP_DIV [1:0] / VGH_NDISP_DIV [1:0] / VCL_NDISP_DIV [1:0] / AVDD_NDISP_DIV [1:0] </th> <th> Charge pump CLK </th> </tr> </thead> <tbody> <tr> <td>00</td> <td>CP_CLK</td> </tr> <tr> <td>01</td> <td>CP_CLK/2</td> </tr> <tr> <td>10</td> <td>CP_CLK/4</td> </tr> <tr> <td>11</td> <td>CP_CLK/8</td> </tr> </tbody> </table> <p>Note1:CP_CLK= Nomal display mode CLK</p> <p>Note2: BT5CKB / C_EXT[1:0] + AVEE_NDISP_DIV [1:0] <= 4</p>	AVEE_NDISP_DIV [1:0] / VGH_NDISP_DIV [1:0] / VCL_NDISP_DIV [1:0] / AVDD_NDISP_DIV [1:0]	Charge pump CLK	00	CP_CLK	01	CP_CLK/2	10	CP_CLK/4	11	CP_CLK/8		
AVEE_NDISP_DIV [1:0] / VGH_NDISP_DIV [1:0] / VCL_NDISP_DIV [1:0] / AVDD_NDISP_DIV [1:0]	Charge pump CLK												
00	CP_CLK												
01	CP_CLK/2												
10	CP_CLK/4												
11	CP_CLK/8												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th> Status </th> <th> Availability </th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default Value	<table border="1"> <thead> <tr> <th> Status </th> <th> Default Value </th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

DISPLAY_CTRL_NORM (B6h)

Address (MDDI I/F)		B600h ~ B603h					Access Attribute				R/W
Address (Other I/F)		B6h					Number of Parameter(s)				6
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
B600h	Parameter 1	0	0	0	0	SDT[4:0]				02h	
B601h	Parameter 2	0	0	0	0	EQ11[4:0]				08h	
B602h	Parameter 3	0	0	0	0	EQ12[4:0]				08h	
B603h	Parameter 4	0	0	0	0	EQG [4:0]				08h	
B604h	Parameter 5	0	0	0	0	SOE_S [4:0]				10h	
B605h	Parameter 6	0	0	0	SOE_W[5:0]				23h		

Description	SDT[4:0]: Sets the source delay time.																		
	<table border="1"> <thead> <tr> <th>SDT[4:0]</th> <th>EQG time (clk)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>0</td></tr> <tr><td>01h</td><td>1</td></tr> <tr><td>02h</td><td>2</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>11h</td><td>17</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1Eh</td><td>30</td></tr> <tr><td>1Fh</td><td>31</td></tr> </tbody> </table> <p>Note: 1 clk period = 1/4.33M</p>	SDT[4:0]	EQG time (clk)	00h	0	01h	1	02h	2	:	:	11h	17	:	:	1Eh	30	1Fh	31
	SDT[4:0]	EQG time (clk)																	
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	<table border="1" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;">1Fh</td> <td style="width: 50%; text-align: center;">31</td> </tr> </table> <p style="color: red; font-size: small;">Note: 1 clk period = 1/4.33M</p> <p>SOE_S[4:0]: Source output enable start time.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th style="width: 20%;">SOE_S[4:0]</th> <th style="width: 80%;">SOE Start Time (clk)</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">00h</td><td style="text-align: center;">0</td></tr> <tr><td style="text-align: center;">01h</td><td style="text-align: center;">1</td></tr> <tr><td style="text-align: center;">02h</td><td style="text-align: center;">2</td></tr> <tr><td style="text-align: center;">03h</td><td style="text-align: center;">3</td></tr> <tr><td style="text-align: center;">04h</td><td style="text-align: center;">4</td></tr> <tr><td style="text-align: center;">:</td><td style="text-align: center;">:</td></tr> <tr><td style="text-align: center;">1Fh</td><td style="text-align: center;">31</td></tr> </tbody> </table> <p style="color: red; font-size: small;">Note: 1 clk period = 1/4.33M</p> <p>SOE_W[5:0]: Source output enable start time.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #800080; color: white;"> <th style="width: 20%;">SOE_W[5:0]</th> <th style="width: 80%;">SOE Start Time (clk)</th> </tr> </thead> <tbody> <tr><td style="text-align: center;">00h</td><td style="text-align: center;">0</td></tr> <tr><td style="text-align: center;">01h</td><td style="text-align: center;">1</td></tr> <tr><td style="text-align: center;">02h</td><td style="text-align: center;">2</td></tr> <tr><td style="text-align: center;">03h</td><td style="text-align: center;">3</td></tr> <tr><td style="text-align: center;">04h</td><td style="text-align: center;">4</td></tr> <tr><td style="text-align: center;">:</td><td style="text-align: center;">:</td></tr> <tr><td style="text-align: center;">3Fh</td><td style="text-align: center;">62</td></tr> </tbody> </table> <p style="color: red; font-size: small;">Note: 1 clk period = 1/4.33M</p>	1Fh	31	SOE_S[4:0]	SOE Start Time (clk)	00h	0	01h	1	02h	2	03h	3	04h	4	:	:	1Fh	31	SOE_W[5:0]	SOE Start Time (clk)	00h	0	01h	1	02h	2	03h	3	04h	4	:	:	3Fh	62
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Restriction	-																																		
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #000080; color: white;"> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr><td style="text-align: center;">Sleep In</td><td style="text-align: center;">Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																						
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Default Value	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #000080; color: white;"> <th style="width: 25%;">Status</th> <th style="width: 12.5%;">B600h</th> <th style="width: 12.5%;">B601h</th> <th style="width: 12.5%;">B602h</th> <th style="width: 12.5%;">B603h</th> <th style="width: 12.5%;">B604h</th> <th style="width: 12.5%;">B605h</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="color: red; text-align: center;">02h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">10h</td> <td style="color: red; text-align: center;">23h</td> </tr> <tr> <td>S/W Reset</td> <td style="color: red; text-align: center;">02h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">10h</td> <td style="color: red; text-align: center;">23h</td> </tr> <tr> <td>H/W Reset</td> <td style="color: red; text-align: center;">02h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">08h</td> <td style="color: red; text-align: center;">10h</td> <td style="color: red; text-align: center;">23h</td> </tr> </tbody> </table>	Status	B600h	B601h	B602h	B603h	B604h	B605h	Power On Sequence	02h	08h	08h	08h	10h	23h	S/W Reset	02h	08h	08h	08h	10h	23h	H/W Reset	02h	08h	08h	08h	10h	23h						
Status	B600h	B601h	B602h	B603h	B604h	B605h																													
Power On Sequence	02h	08h	08h	08h	10h	23h																													
S/W Reset	02h	08h	08h	08h	10h	23h																													
H/W Reset	02h	08h	08h	08h	10h	23h																													

DISPLAY_CTRL2: Set the States for LED Control (B7h)

Address (MDDI I/F)		B700h						Access Attribute				R/W
Address (Other I/F)		B7h						Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value	
B700h	Parameter 1	0	0	0	REV	SRGB	CTS	0	0	0	00h	

Description	CTS : This command is use to selection for CMD1 instruction code. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>CTS</th> <th>Selection for CMD1 Instruction Code</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Support FULL Command Set (Default)</td> </tr> <tr> <td>1h</td> <td>Only Support Nokia Command Set</td> </tr> </tbody> </table>	CTS	Selection for CMD1 Instruction Code	0h	Support FULL Command Set (Default)	1h	Only Support Nokia Command Set														
	CTS	Selection for CMD1 Instruction Code																			
	0h	Support FULL Command Set (Default)																			
	1h	Only Support Nokia Command Set																			
	REV : Normally White or Normally Black Select. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>REV</th> <th>Panel</th> <th>Data</th> <th>Color</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td rowspan="2">0</td> <td rowspan="2">NW</td> <td>0x00</td> <td>Black</td> <td>V0+/V0-</td> </tr> <tr> <td>0xFF</td> <td>White</td> <td>V63+/V63-</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">NB</td> <td>0x00</td> <td>Black</td> <td>V63+/V63-</td> </tr> <tr> <td>0xFF</td> <td>White</td> <td>V0+/V0-</td> </tr> </tbody> </table> <p>Example: Using NW Panel, set REV = 0 (digital not reverse data) => Data code = 'd0, results in BLACK, vice versa.</p>	REV	Panel	Data	Color	Source	0	NW	0x00	Black	V0+/V0-	0xFF	White	V63+/V63-	1	NB	0x00	Black	V63+/V63-	0xFF	White
REV	Panel	Data	Color	Source																	
0	NW	0x00	Black	V0+/V0-																	
		0xFF	White	V63+/V63-																	
1	NB	0x00	Black	V63+/V63-																	
		0xFF	White	V0+/V0-																	
SRGB : RGB Order Select <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SRGB</th> <th>Order</th> <th>Gamma</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>RGB</td> <td>Normal</td> </tr> <tr> <td>1</td> <td>BGR</td> <td>RB Swap</td> </tr> </tbody> </table>	SRGB	Order	Gamma	0	RGB	Normal	1	BGR	RB Swap												
SRGB	Order	Gamma																			
0	RGB	Normal																			
1	BGR	RB Swap																			
Restriction																					
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Status	B700h																				
Power On Sequence	00h																				
S/W Reset	00h																				
H/W Reset	00h																				

MTP Selection (B8h)

Address (MDDI I/F)		B800h					Access Attribute				R/W
Address (Other I/F)		B8h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
B800h	Parameter 1	0	0	0	0	0	0	PTM[1:0]		MTP_W_GMA	00h

Description	PTM:MTP margin read mode select.	<table border="1"> <thead> <tr> <th>PTM[1:0]</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>00h(Default)</td> </tr> <tr> <td>01</td> <td>Full Access Margin</td> </tr> <tr> <td>10</td> <td>Reversed</td> </tr> <tr> <td>11</td> <td>Reversed</td> </tr> </tbody> </table>	PTM[1:0]	Function	00	00h(Default)	01	Full Access Margin	10	Reversed	11	Reversed		
	PTM[1:0]	Function												
00	00h(Default)													
01	Full Access Margin													
10	Reversed													
11	Reversed													
	MTP_W_GMA: Used to enable/disable MTP write gamma.	<table border="1"> <thead> <tr> <th>MTP_W_GMA</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable(Default)</td> </tr> </tbody> </table>	MTP_W_GMA	Function	0	Disable	1	Enable(Default)						
MTP_W_GMA	Function													
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1	Enable(Default)													
Restriction														
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Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
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Status	Default Value D[7 : 0]													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

PWR_CTRL1 (C0h)

Address (MDDI I/F)			C000h ~ C001h				Access Attribute				R/W
Address (Other I/F)			C0h				Number of Parameter(s)				2
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C000h	Parameter 1	0	0	VRHP[6:0]						44h	
C001h	Parameter 2	0	0	VRHN[6:0]						44h	
C002h	Parameter 3	0	0	VGSP[6:0]						10h	
C003h	Parameter 4	0	0	VGSN[6:0]						10h	

Description	Set the GVDD regulator output voltage.					
	VRHP[6:0]: set the GVDDP regulator output voltage.					
		DEC	VRHP (V)		DEC	VRHP (V)
		0	2.8	01000000	64	4.4
		1	2.825	01000001	65	4.425
		2	2.85	01000010	66	4.45
		3	2.875	01000011	67	4.475
	Reserved	4	2.9	01000100	68	4.5
		5	2.925	01000101	69	4.525
		6	2.95	01000110	70	4.55
		7	2.975	01000111	71	4.575
	00001000	8	3	01001000	72	4.6
	00001001	9	3.025	01001001	73	4.625
	00001010	10	3.05	01001010	74	4.65
	00001011	11	3.075	01001011	75	4.675
	00001100	12	3.1	01001100	76	4.7
	00001101	13	3.125	01001101	77	4.725
	00001110	14	3.15	01001110	78	4.75
	00001111	15	3.175	01001111	79	4.775
	00010000	16	3.2	01010000	80	4.8
	00010001	17	3.225	01010001	81	4.825
	00010010	18	3.25	01010010	82	4.85
	00010011	19	3.275	01010011	83	4.875
	00010100	20	3.3	01010100	84	4.9
	00010101	21	3.325	01010101	85	4.925
	00010110	22	3.35	01010110	86	4.95
	00010111	23	3.375	01010111	87	4.975
	00011000	24	3.4	01011000	88	5
	00011001	25	3.425	01011001	89	5.025
	00011010	26	3.45	01011010	90	5.05
	00011011	27	3.475	01011011	91	5.075
	00011100	28	3.5	01011100	92	5.1
	00011101	29	3.525	01011101	93	5.125
	00011110	30	3.55	01011110	94	5.15
00011111	31	3.575	01011111	95	5.175	
00100000	32	3.6	01100000	96	5.2	
00100001	33	3.625	01100001	97	5.225	

00100010	34	3.65	01100010	98	5.25
00100011	35	3.675	01100011	99	5.275
00100100	36	3.7	01100100	100	5.3
00100101	37	3.725	01100101	101	5.325
00100110	38	3.75	01100110	102	5.35
00100111	39	3.775	01100111	103	5.375
00101000	40	3.8	01101000	104	5.4
00101001	41	3.825	01101001	105	5.425
00101010	42	3.85	01101010	106	5.45
00101011	43	3.875	01101011	107	5.475
00101100	44	3.9	01101100	108	5.5
00101101	45	3.925	01101101	109	
00101110	46	3.95	01101110	110	
00101111	47	3.975	01101111	111	
00110000	48	4	01110000	112	
00110001	49	4.025	01110001	113	
00110010	50	4.05	01110010	114	
00110011	51	4.075	01110011	115	
00110100	52	4.1	01110100	116	
00110101	53	4.125	01110101	117	
00110110	54	4.15	01110110	118	Reserved
00110111	55	4.175	01110111	119	
00111000	56	4.2	01111000	120	
00111001	57	4.225	01111001	121	
00111010	58	4.25	01111010	122	
00111011	59	4.275	01111011	123	
00111100	60	4.3	01111100	124	
00111101	61	4.325	01111101	125	
00111110	62	4.35	01111110	126	
00111111	63	4.375	01111111	127	

VRHN[6:0]: set the GVDDN regulator output voltage.

	DEC	VRHN (V)		DEC	VRHN (V)
Reserved	0	-2.8	01000000	64	-4.4
	1	-2.825	01000001	65	-4.425
	2	-2.85	01000010	66	-4.45
	3	-2.875	01000011	67	-4.475
	4	-2.9	01000100	68	-4.5
	5	-2.925	01000101	69	-4.525
	6	-2.95	01000110	70	-4.55
	7	-2.975	01000111	71	-4.575
00001000	8	-3	01001000	72	-4.6
00001001	9	-3.025	01001001	73	-4.625
00001010	10	-3.05	01001010	74	-4.65
00001011	11	-3.075	01001011	75	-4.675
00001100	12	-3.1	01001100	76	-4.7
00001101	13	-3.125	01001101	77	-4.725
00001110	14	-3.15	01001110	78	-4.75

00001111	15	-3.175	01001111	79	-4.775
00010000	16	-3.2	01010000	80	-4.8
00010001	17	-3.225	01010001	81	-4.825
00010010	18	-3.25	01010010	82	-4.85
00010011	19	-3.275	01010011	83	-4.875
00010100	20	-3.3	01010100	84	-4.9
00010101	21	-3.325	01010101	85	-4.925
00010110	22	-3.35	01010110	86	-4.95
00010111	23	-3.375	01010111	87	-4.975
00011000	24	-3.4	01011000	88	-5
00011001	25	-3.425	01011001	89	-5.025
00011010	26	-3.45	01011010	90	-5.05
00011011	27	-3.475	01011011	91	-5.075
00011100	28	-3.5	01011100	92	-5.1
00011101	29	-3.525	01011101	93	-5.125
00011110	30	-3.55	01011110	94	-5.15
00011111	31	-3.575	01011111	95	-5.175
00100000	32	-3.6	01100000	96	-5.2
00100001	33	-3.625	01100001	97	-5.225
00100010	34	-3.65	01100010	98	-5.25
00100011	35	-3.675	01100011	99	-5.275
00100100	36	-3.7	01100100	100	-5.3
00100101	37	-3.725	01100101	101	-5.325
00100110	38	-3.75	01100110	102	-5.35
00100111	39	-3.775	01100111	103	-5.375
00101000	40	-3.8	01101000	104	-5.4
00101001	41	-3.825	01101001	105	-5.425
00101010	42	-3.85	01101010	106	-5.45
00101011	43	-3.875	01101011	107	-5.475
00101100	44	-3.9	01101100	108	-5.5
00101101	45	-3.925	01101101	109	Reserved
00101110	46	-3.95	01101110	110	
00101111	47	-3.975	01101111	111	
00110000	48	-4	01110000	112	
00110001	49	-4.025	01110001	113	
00110010	50	-4.05	01110010	114	
00110011	51	-4.075	01110011	115	
00110100	52	-4.1	01110100	116	
00110101	53	-4.125	01110101	117	
00110110	54	-4.15	01110110	118	
00110111	55	-4.175	01110111	119	
00111000	56	-4.2	01111000	120	
00111001	57	-4.225	01111001	121	
00111010	58	-4.25	01111010	122	

00111011	59	-4.275	01111011	123
00111100	60	-4.3	01111100	124
00111101	61	-4.325	01111101	125
00111110	62	-4.35	01111110	126
00111111	63	-4.375	01111111	127

VGSP [6:0]: set the VGSP regulator output voltage.

	DEC	VGMP (V)		DEC	VGMP (V)
	0	0	1000000	64	1.6
	1	0.025	1000001	65	1.625
	2	0.05	1000010	66	1.65
	3	0.075	1000011	67	1.675
	4	0.1	1000100	68	1.7
	5	0.125	1000101	69	1.725
	6	0.15	1000110	70	1.75
Reserved	7	0.175	1000111	71	1.775
0001000	8	0.2	1001000	72	1.8
0001001	9	0.225	1001001	73	1.825
0001010	10	0.25	1001010	74	1.85
0001011	11	0.275	1001011	75	1.875
0001100	12	0.3	1001100	76	1.9
0001101	13	0.325	1001101	77	1.925
0001110	14	0.35	1001110	78	1.95
0001111	15	0.375	1001111	79	1.975
0010000	16	0.4	1010000	80	2
0010001	17	0.425	1010001	81	2.025
0010010	18	0.45	1010010	82	2.05
0010011	19	0.475	1010011	83	2.075
0010100	20	0.5	1010100	84	2.1
0010101	21	0.525	1010101	85	2.125
0010110	22	0.55	1010110	86	2.15
0010111	23	0.575	1010111	87	2.175
0011000	24	0.6	1011000	88	2.2
0011001	25	0.625	1011001	89	2.225
0011010	26	0.65	1011010	90	2.25
0011011	27	0.675	1011011	91	2.275
0011100	28	0.7	1011100	92	2.3
0011101	29	0.725	1011101	93	2.325
0011110	30	0.75	1011110	94	2.35
0011111	31	0.775	1011111	95	2.375
0100000	32	0.8	1100000	96	2.4
0100001	33	0.825	1100001	97	2.425
0100010	34	0.85	1100010	98	2.45
0100011	35	0.875	1100011	99	2.475
0100100	36	0.9	1100100	100	2.5
0100101	37	0.925	1100101	101	2.525
0100110	38	0.95	1100110	102	2.55
0100111	39	0.975	1100111	103	2.575
0101000	40	1	1101000	104	2.6
0101001	41	1.025	1101001	105	2.625
0101010	42	1.05	1101010	106	2.65
0101011	43	1.075	1101011	107	2.675

0101100	44	1.1	1101100	108	2.7
0101101	45	1.125	1101101	109	2.725
0101110	46	1.15	1101110	110	2.75
0101111	47	1.175	1101111	111	2.775
0110000	48	1.2	1110000	112	2.8
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0110010	50	1.25	1110010	114	2.85
0110011	51	1.275	1110011	115	2.875
0110100	52	1.3	1110100	116	2.9
0110101	53	1.325	1110101	117	2.925
0110110	54	1.35	1110110	118	2.95
0110111	55	1.375	1110111	119	2.975
0111000	56	1.4	1111000	120	
0111001	57	1.425	1111001	121	
0111010	58	1.45	1111010	122	
0111011	59	1.475	1111011	123	
0111100	60	1.5	1111100	124	
0111101	61	1.525	1111101	125	
0111110	62	1.55	1111110	126	
0111111	63	1.575	1111111	127	Reserved

VGSN [6:0]: set the VGSN regulator output voltage.

DEC	VGMP (V)	DEC	VGMP (V)	
0	0	1000000	64	-1.6
1	-0.025	1000001	65	-1.625
2	-0.05	1000010	66	-1.65
Reserved	-0.075	1000011	67	-1.675
	-0.1	1000100	68	-1.7
	-0.125	1000101	69	-1.725
	-0.15	1000110	70	-1.75
	-0.175	1000111	71	-1.775
0001000	-0.2	1001000	72	-1.8
0001001	-0.225	1001001	73	-1.825
0001010	-0.25	1001010	74	-1.85
0001011	-0.275	1001011	75	-1.875
0001100	-0.3	1001100	76	-1.9
0001101	-0.325	1001101	77	-1.925
0001110	-0.35	1001110	78	-1.95
0001111	-0.375	1001111	79	-1.975
0010000	-0.4	1010000	80	-2
0010001	-0.425	1010001	81	-2.025
0010010	-0.45	1010010	82	-2.05
0010011	-0.475	1010011	83	-2.075
0010100	-0.5	1010100	84	-2.1
0010101	-0.525	1010101	85	-2.125
0010110	-0.55	1010110	86	-2.15
0010111	-0.575	1010111	87	-2.175
0011000	-0.6	1011000	88	-2.2
0011001	-0.625	1011001	89	-2.225

	0011010	26	-0.65	1011010	90	-2.25	
	0011011	27	-0.675	1011011	91	-2.275	
	0011100	28	-0.7	1011100	92	-2.3	
	0011101	29	-0.725	1011101	93	-2.325	
	0011110	30	-0.75	1011110	94	-2.35	
	0011111	31	-0.775	1011111	95	-2.375	
	0100000	32	-0.8	1100000	96	-2.4	
	0100001	33	-0.825	1100001	97	-2.425	
	0100010	34	-0.85	1100010	98	-2.45	
	0100011	35	-0.875	1100011	99	-2.475	
	0100100	36	-0.9	1100100	100	-2.5	
	0100101	37	-0.925	1100101	101	-2.525	
	0100110	38	-0.95	1100110	102	-2.55	
	0100111	39	-0.975	1100111	103	-2.575	
	0101000	40	-1	1101000	104	-2.6	
	0101001	41	-1.025	1101001	105	-2.625	
	0101010	42	-1.05	1101010	106	-2.65	
	0101011	43	-1.075	1101011	107	-2.675	
	0101100	44	-1.1	1101100	108	-2.7	
	0101101	45	-1.125	1101101	109	-2.725	
	0101110	46	-1.15	1101110	110	-2.75	
	0101111	47	-1.175	1101111	111	-2.775	
	0110000	48	-1.2	1110000	112	-2.8	
	0110001	49	-1.225	1110001	113	-2.825	
	0110010	50	-1.25	1110010	114	-2.85	
	0110011	51	-1.275	1110011	115	-2.875	
	0110100	52	-1.3	1110100	116	-2.9	
	0110101	53	-1.325	1110101	117	-2.925	
	0110110	54	-1.35	1110110	118	-2.95	
	0110111	55	-1.375	1110111	119	-2.975	
	0111000	56	-1.4	1111000	120		
	0111001	57	-1.425	1111001	121		
	0111010	58	-1.45	1111010	122		
	0111011	59	-1.475	1111011	123		
	0111100	60	-1.5	1111100	124		Reserved
	0111101	61	-1.525	1111101	125		
	0111110	62	-1.55	1111110	126		
	0111111	63	-1.575	1111111	127		

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Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	

Default Value	Status	C000h	C001h	C002h	C003h
	Power On Sequence	44h	44h	10h	10h
	S/W Reset	44h	44h	10h	10h
	H/W Reset	44h	44h	10h	10h

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PWR_CTRL2 (C1h)

Address (MDDI I/F)		C100h ~ C101h					Access Attribute				R/W
Address (Other I/F)		C1h					Number of Parameter(s)				2
Address (MDDI I/F)	Parameter (Other I/F)	D[17 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C100h	Parameter 1	0	0	CP1_mode	PUMP_MODE[1:0]		0	BTP1CKA_EXT[2:0]			13h
C101h	Parameter 2	0	0	BTP1CKB_EXT[2:0]		0	BTP1CKC_EXT[2:0]			33h	

Description	<p>CP1_Mode : This bit used to enable select BTP1CKA_EXT[2:0] and PUMP_MODE[1:0].</p> <table border="1"> <thead> <tr> <th>CP1_Mode</th> <th>Function Selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Only support AVDDx2 pump & only fixed on one operating frequency.</td> </tr> <tr> <td>1</td> <td>Support all case of pump mode select & operating frequency select.</td> </tr> </tbody> </table>	CP1_Mode	Function Selection	0	Only support AVDDx2 pump & only fixed on one operating frequency.	1	Support all case of pump mode select & operating frequency select.											
	CP1_Mode	Function Selection																
	0	Only support AVDDx2 pump & only fixed on one operating frequency.																
	1	Support all case of pump mode select & operating frequency select.																
	<p>PUMP_MODE[1:0]: AVDD pump mode selection.</p> <table border="1"> <thead> <tr> <th>PUMP_MODE[1:0]</th> <th>Mode Selection</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Reserved</td> </tr> <tr> <td>01</td> <td>AVDD x 2</td> </tr> <tr> <td>10</td> <td>AVDD x 3</td> </tr> <tr> <td>11</td> <td>Reserved</td> </tr> </tbody> </table>	PUMP_MODE[1:0]	Mode Selection	00	Reserved	01	AVDD x 2	10	AVDD x 3	11	Reserved							
	PUMP_MODE[1:0]	Mode Selection																
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<p>BTP1CKA_EXT[2:0]: Set the operating frequency of the step-up circuit 1 in full colors normal mode.(Normal mode on)</p> <table border="1"> <thead> <tr> <th>BTP1CKA_EXT[2:0]</th> <th>Step-up cycle for step-up circuit 1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reserved</td> </tr> <tr> <td>001</td> <td>DCCLK/4</td> </tr> <tr> <td>010</td> <td>DCCLK/8</td> </tr> <tr> <td>011</td> <td>DCCLK/16</td> </tr> <tr> <td>100</td> <td>DCCLK/32</td> </tr> <tr> <td>101</td> <td>DCCLK/64</td> </tr> <tr> <td>110</td> <td>DCCLK/128</td> </tr> <tr> <td>111</td> <td>Reserved</td> </tr> </tbody> </table>	BTP1CKA_EXT[2:0]	Step-up cycle for step-up circuit 1	000	Reserved	001	DCCLK/4	010	DCCLK/8	011	DCCLK/16	100	DCCLK/32	101	DCCLK/64	110	DCCLK/128	111	Reserved
BTP1CKA_EXT[2:0]	Step-up cycle for step-up circuit 1																	
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110	DCCLK/128																	
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<p>BTP1CKB_EXT[2:0]: Set the operating frequency of the step-up circuit 1 in idle mode.(Idle mode on)</p> <table border="1"> <thead> <tr> <th>BTP1CKB_EXT[2:0]</th> <th>Step-up cycle for step-up circuit 1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reserved</td> </tr> <tr> <td>001</td> <td>DCCLK/4</td> </tr> <tr> <td>010</td> <td>DCCLK/8</td> </tr> <tr> <td>011</td> <td>DCCLK/16</td> </tr> <tr> <td>100</td> <td>DCCLK/32</td> </tr> <tr> <td>101</td> <td>DCCLK/64</td> </tr> <tr> <td>110</td> <td>DCCLK/128</td> </tr> <tr> <td>111</td> <td>Reserved</td> </tr> </tbody> </table>	BTP1CKB_EXT[2:0]	Step-up cycle for step-up circuit 1	000	Reserved	001	DCCLK/4	010	DCCLK/8	011	DCCLK/16	100	DCCLK/32	101	DCCLK/64	110	DCCLK/128	111	Reserved
BTP1CKB_EXT[2:0]	Step-up cycle for step-up circuit 1																	
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<p>BTP1CKC_EXT[2:0]: Set the operating frequency of the step-up circuit 1 in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1"> <thead> <tr> <th>BTP1CKC_EXT[2:0]</th> <th>Step-up cycle for step-up circuit 1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reserved</td> </tr> <tr> <td>001</td> <td>DCCLK/4</td> </tr> <tr> <td>010</td> <td>DCCLK/8</td> </tr> <tr> <td>011</td> <td>DCCLK/16</td> </tr> <tr> <td>100</td> <td>DCCLK/32</td> </tr> <tr> <td>101</td> <td>DCCLK/64</td> </tr> <tr> <td>110</td> <td>DCCLK/128</td> </tr> <tr> <td>111</td> <td>Reserved</td> </tr> </tbody> </table>	BTP1CKC_EXT[2:0]	Step-up cycle for step-up circuit 1	000	Reserved	001	DCCLK/4	010	DCCLK/8	011	DCCLK/16	100	DCCLK/32	101	DCCLK/64	110	DCCLK/128	111	Reserved
BTP1CKC_EXT[2:0]	Step-up cycle for step-up circuit 1																	
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111	Reserved																	
<p>Note: DCCLK is 8 times the unit frequency of one line.</p>																		

Default Value	<table border="1"><thead><tr><th>Status</th><th>C100h</th><th>C101h</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>13h</td><td>33h</td></tr><tr><td>S/W Reset</td><td>13h</td><td>33h</td></tr><tr><td>H/W Reset</td><td>13h</td><td>33h</td></tr></tbody></table>	Status	C100h	C101h	Power On Sequence	13h	33h	S/W Reset	13h	33h	H/W Reset	13h	33h
	Status	C100h	C101h										
	Power On Sequence	13h	33h										
	S/W Reset	13h	33h										
H/W Reset	13h	33h											

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PWR_CTRL3 (C2h)

Address (MDDI I/F)			C200h ~ C202h				Access Attribute				R/W
Address (Other I/F)			C2h				Number of Parameter(s)				3
Address (MDDI I/F)	Parameter (Other I/F)	D[17 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C200h	Parameter 1	0	0	VGHLA[2:0]			0	VGHL_CLKA[2:0]			44h
C201h	Parameter 2	0	0	VGHLB[2:0]			0	VGHL_CLKB[2:0]			44h
C202h	Parameter 3	0	0	VGHLC[2:0]			0	VGHL_CLKC[2:0]			44h

Description	<p>VGHA[2:0]: VGH charge pump circuit selection in full colors normal mode.(Normal mode on) VGHB[2:0]: VGH charge pump circuit selection in idle mode.(Idle mode on) VGHC[2:0]: VGH charge pump circuit selection in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1"> <thead> <tr> <th rowspan="2">VGHLA[2:0] / VGHLB [2:0] / VGHLC[2:0]</th> <th colspan="2">Charge pump level for VGHLA/B/C</th> </tr> <tr> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr><td>000</td><td>3xAVDD</td><td>-3xAVDD</td></tr> <tr><td>001</td><td>3xAVDD</td><td>-2xAVDD</td></tr> <tr><td>010</td><td>3xAVDD</td><td>-2xAVDD</td></tr> <tr><td>011</td><td>VCI+2xAVDD</td><td>-VCI-2xAVDD</td></tr> <tr><td>100</td><td>VCI+2xAVDD</td><td>-2xAVDD</td></tr> <tr><td>101</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>110</td><td>2xAVDD</td><td>-2xAVDD</td></tr> <tr><td>111</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table> <p>VGHL_CLKA[2:0]: Set the operating frequency of the step-up circuit2 (VGH) in full colors normal mode.(Normal mode on) VGHL_CLKB[2:0]: Set the operating frequency of the step-up circuit2 (VGH) in idle mode.(Idle mode on) VGHL_CLKC[2:0]: Set the operating frequency of the step-up circuit2 (VGH) in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1"> <thead> <tr> <th>VGHL_CLKA[2:0] / VGHL_CLKB[2:0] / VGHL_CLKC[2:0]</th> <th>Step-up cycle for VGHL step-up circuit</th> </tr> </thead> <tbody> <tr><td>000</td><td>DCCLK</td></tr> <tr><td>001</td><td>DCCLK/2</td></tr> <tr><td>010</td><td>DCCLK/4</td></tr> <tr><td>011</td><td>DCCLK/8</td></tr> <tr><td>100</td><td>DCCLK/16</td></tr> <tr><td>101</td><td>DCCLK/32</td></tr> <tr><td>110</td><td>DCCLK/64</td></tr> <tr><td>111</td><td>DCCLK/128</td></tr> </tbody> </table>	VGHLA[2:0] / VGHLB [2:0] / VGHLC[2:0]	Charge pump level for VGHLA/B/C		VGH	VGL	000	3xAVDD	-3xAVDD	001	3xAVDD	-2xAVDD	010	3xAVDD	-2xAVDD	011	VCI+2xAVDD	-VCI-2xAVDD	100	VCI+2xAVDD	-2xAVDD	101	Reserved	Reserved	110	2xAVDD	-2xAVDD	111	Reserved	Reserved	VGHL_CLKA[2:0] / VGHL_CLKB[2:0] / VGHL_CLKC[2:0]	Step-up cycle for VGHL step-up circuit	000	DCCLK	001	DCCLK/2	010	DCCLK/4	011	DCCLK/8	100	DCCLK/16	101	DCCLK/32	110	DCCLK/64	111	DCCLK/128
	VGHLA[2:0] / VGHLB [2:0] / VGHLC[2:0]		Charge pump level for VGHLA/B/C																																													
VGH		VGL																																														
000	3xAVDD	-3xAVDD																																														
001	3xAVDD	-2xAVDD																																														
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VGHL_CLKA[2:0] / VGHL_CLKB[2:0] / VGHL_CLKC[2:0]	Step-up cycle for VGHL step-up circuit																																															
000	DCCLK																																															
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Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>C200h</th> <th>C201h</th> <th>C202h</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>44h</td> <td>44h</td> <td>44h</td> </tr> <tr> <td>S/W Reset</td> <td>44h</td> <td>44h</td> <td>44h</td> </tr> <tr> <td>H/W Reset</td> <td>44h</td> <td>44h</td> <td>44h</td> </tr> </tbody> </table>	Status	C200h	C201h	C202h	Power On Sequence	44h	44h	44h	S/W Reset	44h	44h	44h	H/W Reset	44h	44h	44h																															
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Power On Sequence	44h	44h	44h																																													
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PWR_CTRL5 (C3h)

Address (MDDI I/F)		C300h ~ C301h					Access Attribute				R/W
Address (Other I/F)		C3h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[17 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C300h	Parameter 1	0	0	0	BTP5CKC_EXT[1:0]		BTP5CKB_EXT[1:0]		BTP5CKA_EXT[1:0]		2Ah

Description	<p>BTP5CKA_EXT[1:0]: Set the operating frequency of the step-up circuit 5 in full colors normal mode.(Normal mode on)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BTP5CKA_EXT[1:0]</th> <th>Step-up cycle for step-up circuit 5</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Reserved</td> </tr> <tr> <td>01</td> <td>DCCLK/4</td> </tr> <tr> <td>10</td> <td>DCCLK/8</td> </tr> <tr> <td>11</td> <td>DCCLK/16</td> </tr> </tbody> </table>	BTP5CKA_EXT[1:0]	Step-up cycle for step-up circuit 5	00	Reserved	01	DCCLK/4	10	DCCLK/8	11	DCCLK/16
	BTP5CKA_EXT[1:0]	Step-up cycle for step-up circuit 5									
	00	Reserved									
01	DCCLK/4										
10	DCCLK/8										
11	DCCLK/16										
<p>BTP5CKB_EXT[1:0]: Set the operating frequency of the step-up circuit 5 in idle mode.(Idle mode on)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BTP5CKB_EXT[1:0]</th> <th>Step-up cycle for step-up circuit 5</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Reserved</td> </tr> <tr> <td>01</td> <td>DCCLK/4</td> </tr> <tr> <td>10</td> <td>DCCLK/8</td> </tr> <tr> <td>11</td> <td>DCCLK/16</td> </tr> </tbody> </table>	BTP5CKB_EXT[1:0]	Step-up cycle for step-up circuit 5	00	Reserved	01	DCCLK/4	10	DCCLK/8	11	DCCLK/16	
BTP5CKB_EXT[1:0]	Step-up cycle for step-up circuit 5										
00	Reserved										
01	DCCLK/4										
10	DCCLK/8										
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<p>BTP5CKC_EXT[1:0]: Set the operating frequency of the step-up circuit 5 in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BTP5CKC_EXT[1:0]</th> <th>Step-up cycle for step-up circuit 5</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Reserved</td> </tr> <tr> <td>01</td> <td>DCCLK/4</td> </tr> <tr> <td>10</td> <td>DCCLK/8</td> </tr> <tr> <td>11</td> <td>DCCLK/16</td> </tr> </tbody> </table>	BTP5CKC_EXT[1:0]	Step-up cycle for step-up circuit 5	00	Reserved	01	DCCLK/4	10	DCCLK/8	11	DCCLK/16	
BTP5CKC_EXT[1:0]	Step-up cycle for step-up circuit 5										
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Status	C300h										
Power On Sequence	2Ah										
S/W Reset	2Ah										
H/W Reset	2Ah										

Default Value	<table border="1"><thead><tr><th>Status</th><th>C400h</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>40h</td></tr><tr><td>S/W Reset</td><td>40h</td></tr><tr><td>H/W Reset</td><td>40h</td></tr></tbody></table>	Status	C400h	Power On Sequence	40h	S/W Reset	40h	H/W Reset	40h
	Status	C400h							
	Power On Sequence	40h							
	S/W Reset	40h							
H/W Reset	40h								

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PWR_CTRL7 (C5h)

Address (MDDI I/F)		C500h ~ C504h					Access Attribute				R/W
Address (Other I/F)		C5h					Number of Parameter(s)				4
Address (MDDI I/F)	Parameter (Other I/F)	D[17 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C500h	Parameter 1	0	0	ISOPP[2:0]			BIAS_REDUCE	ISOPN[2:0]			4Ch
C501h	Parameter 2	0	0	SAPPA[2:0]			0	SAPNA[2:0]			44h
C502h	Parameter 3	0	0	SAPPB[2:0]			0	SAPNB[2:0]			44h
C503h	Parameter 4	0	0	SAPPC[2:0]			0	SAPNC[2:0]			44h

Description	<p>ISOPP[2:0]: Positive Source OP output stage current control</p> <p>ISOPN[2:0]: Negative Source OP output stage current control</p> <p>SAPPA[2:0]: Positive Source OP current control in full colors normal mode.(Normal mode on)</p> <p>SAPPB[2:0]: Positive Source OP current control in idle mode.(Idle mode on)</p> <p>SAPPC[2:0]: Positive Source OP current control in full colors partial mode.(Partial mode on / Idle mode off)</p>																		
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<p>SAPNA[2:0]: Negative Source OP current control in full colors normal mode.(Normal mode on)</p> <p>SAPNB[2:0]: Negative Source OP current control in idle mode.(Idle mode on)</p> <p>SAPNC[2:0]: Negative Source OP current control in full colors partial mode.(Partial mode on / Idle mode off)</p>																			
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Default Value	Parameter1 ~ Parameter4:	
	Status	Default Value
	Power On Sequence	44h
	S/W Reset	44h
	HW Reset	44h

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PWR_CTRL8 (C6h)

Address (MDDI I/F)			C600h ~ C603h				Access Attribute				R/W
Address (Other I/F)			C6h				Number of Parameter(s)				4
Address (MDDI I/F)	Parameter (Other I/F)	D[17 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
C600h	Parameter 1	0	0	0	0	0	0	0	VGHCL_OFF	VGLCL_OFF	00h
C601h	Parameter 2	0	VGL_CLAMP[A:2:0]				VGH_CLAMP[A:2:0]				E2h
C602h	Parameter 3	0	VGL_CLAMP[B:2:0]				VGH_CLAMP[B:2:0]				E2h
C603h	Parameter 4	0	VGL_CLAMP[C:2:0]				VGH_CLAMP[C:2:0]				E2h

Description	<p>VGLA[2:0]: VGL clamp voltage selection in full colors normal mode.(Normal mode on) VGLB[2:0]: VGL clamp voltage selection in idle mode.(Idle mode on) VGLC[2:0]: VGL clamp voltage selection in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1"> <thead> <tr> <th>VGL_CLAMP[A:3:0] / VGL_CLAMP[B:3:0] / VGL_CLAMP[C:3:0]</th> <th>VGL Clamp Voltage</th> </tr> </thead> <tbody> <tr><td>0000</td><td>-17V</td></tr> <tr><td>0001</td><td>-16.5V</td></tr> <tr><td>0010</td><td>-16V</td></tr> <tr><td>0011</td><td>-15.5V</td></tr> <tr><td>0100</td><td>-15V</td></tr> <tr><td>0101</td><td>-14.5V</td></tr> <tr><td>0110</td><td>-14V</td></tr> <tr><td>0111</td><td>-13.5V</td></tr> <tr><td>1000</td><td>-13V</td></tr> <tr><td>1001</td><td>-12.5V</td></tr> <tr><td>1010</td><td>-12V</td></tr> <tr><td>1011</td><td>-11.5V</td></tr> <tr><td>1100</td><td>-11V</td></tr> <tr><td>1101</td><td>-10.5V</td></tr> <tr><td>1110</td><td>-10V</td></tr> <tr><td>1111</td><td>-9.5V</td></tr> </tbody> </table> <p>VGHA[2:0]: VGH clamp voltage selection in full colors normal mode.(Normal mode on) VGHB[2:0]: VGH clamp voltage selection in idle mode.(Idle mode on) VGHC[2:0]: VGH clamp voltage selection in full colors partial mode.(Partial mode on / Idle mode off)</p> <table border="1"> <thead> <tr> <th>VGH_CLAMP[A:3:0] / VGH_CLAMP[B:3:0] / VGH_CLAMP[C:3:0]</th> <th>VGH Clamp Voltage</th> </tr> </thead> <tbody> <tr><td>0000</td><td>17V</td></tr> <tr><td>0001</td><td>16.5V</td></tr> <tr><td>0010</td><td>16V</td></tr> <tr><td>0011</td><td>15.5V</td></tr> <tr><td>0100</td><td>15V</td></tr> <tr><td>0101</td><td>14.5V</td></tr> <tr><td>0110</td><td>14V</td></tr> <tr><td>0111</td><td>13.5V</td></tr> <tr><td>1000</td><td>13V</td></tr> <tr><td>1001</td><td>12.5V</td></tr> <tr><td>1010</td><td>12V</td></tr> <tr><td>1011</td><td>Reserved</td></tr> <tr><td>1100</td><td>Reserved</td></tr> <tr><td>1101</td><td>Reserved</td></tr> <tr><td>1110</td><td>Reserved</td></tr> <tr><td>1111</td><td>Reserved</td></tr> </tbody> </table>	VGL_CLAMP[A:3:0] / VGL_CLAMP[B:3:0] / VGL_CLAMP[C:3:0]	VGL Clamp Voltage	0000	-17V	0001	-16.5V	0010	-16V	0011	-15.5V	0100	-15V	0101	-14.5V	0110	-14V	0111	-13.5V	1000	-13V	1001	-12.5V	1010	-12V	1011	-11.5V	1100	-11V	1101	-10.5V	1110	-10V	1111	-9.5V	VGH_CLAMP[A:3:0] / VGH_CLAMP[B:3:0] / VGH_CLAMP[C:3:0]	VGH Clamp Voltage	0000	17V	0001	16.5V	0010	16V	0011	15.5V	0100	15V	0101	14.5V	0110	14V	0111	13.5V	1000	13V	1001	12.5V	1010	12V	1011	Reserved	1100	Reserved	1101	Reserved	1110	Reserved	1111	Reserved
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	<p>VGHCL_OFF/VGLCL_OFF: To enable or disable the VGH and VGL</p> <table border="1"> <thead> <tr> <th>VGHCL_OFF/VGLCL_OFF</th> <th>VGH Clamp Voltage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CLAMP ON</td> </tr> <tr> <td>1</td> <td>CLAMP OFF</td> </tr> </tbody> </table>	VGHCL_OFF/VGLCL_OFF	VGH Clamp Voltage	0	CLAMP ON	1	CLAMP OFF														
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WID_CTRL1 (D1h): WID1

Address (MDDI I/F)		D100h					Access Attribute				W
Address (Other I/F)		D1h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D100h	Parameter 1	0	WID1[7]	WID1[6]	WID1[5]	WID1[4]	WID1[3]	WID1[2]	WID1[1]	WID1[0]	-

Description	Write 8-bit project ID to save it to NV memory. WID1[7:0]: LCD module's manufacturer ID. (specified by handset company).												
Restriction	Write only												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	D100h												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												

WID_CTRL2 (D2h): WID2

Address (Mddl I/F)		D200h					Access Attribute				W
Address (Other I/F)		D2h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D200h	Parameter 1	0	1	WID2[6]	WID2[5]	WID2[4]	WID2[3]	WID2[2]	WID2[1]	WID2[0]	-

Description	Write 7-bit LCD module/driver version ID to save it to NV memory. WID2[6:0]: LCD module/driver version ID(specified by module supplier).												
Restriction	Write only												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
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Status	D200h												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												

WID_CTRL3 (D3h): WID3

Address (MDDI I/F)		D300h					Access Attribute				W
Address (Other I/F)		D3h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D300h	Parameter 1	0	WID3[7]	WID3[6]	WID3[5]	WID3[4]	WID3[3]	WID3[2]	WID3[1]	WID3[0]	-

Description	Write 8-bit project ID to save it to NV memory. WID3[7:0]: project ID (specified by handset company).												
Restriction	Write only												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	D300h												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												

READID4 (D4h): Read ID4

Address (MDDI I/F)		D400h ~ D403h					Access Attribute				R
Address (Other I/F)		D4h					Number of Parameter(s)				4
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D400h	Parameter 1	0	0	0	0	0	0	0	0	1	01h
D401h	Parameter 2	0	0	1	0	1	0	0	1	1	53h
D402h	Parameter 3	0	0	0	0	1	0	0	0	1	10h
D403h	Parameter 4	0	0	0	0	0	ID43[3 : 0]				00h

Description	<p>1st parameter: Vender ID code. "01" means <i>Novatek</i>.</p> <p>2nd and 3rd parameter: Chip ID code. "5310" means NT35310.</p> <p>4th parameter: ID43-ID40: Chip version code.</p>																				
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Status	D400h	D401h	D402h	D403h																	
Power On Sequence	01h	53h	11h	-																	
S/W Reset	01h	53h	11h	-																	
H/W Reset	01h	53h	11h	-																	

DDB_CTRL (D5h) : Write DDB Info

Address (MDDI I/F)			D500h ~ D505h				Access Attribute				R/W
Address (Other I/F)			D5h				Number of Parameter(s)				4
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
D500h	Parameter 1	00h	SID [7 : 0]								00h
D501h	Parameter 2	00h	SID[15 : 8]								00h
D502h	Parameter 3	00h	MRID[7 : 0]								00h
D503h	Parameter 4	00h	MRID[15 : 8]								00h

Description	<p>This command is use to store supplier identification and display module model / revision information for MTP programming.</p> <p><i>Notes :</i></p> <p>Parameter 1 : SID[7 : 0] ~ LS byte of Supplier ID Parameter 2 : SID[15 : 8] ~ MS byte of Supplier ID Parameter 3 : MRID[7 : 0] ~ LS byte of Supplier Elective Data Parameter 4 : MRID[15 : 8] ~ MS byte of Supplier Elective Data such as model number</p>																								
Restriction	-																								
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Default Value	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="4">Default Value</th> </tr> <tr> <th>D500h</th> <th>D501h</th> <th>D502h</th> <th>D503h</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> <td>00h</td> <td>00h</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value				D500h	D501h	D502h	D503h	Power On Sequence	00h	00h	00h	00h	S/W Reset	00h	00h	00h	00h	H/W Reset	00h	00h	00h	00h
Status	Default Value																								
	D500h	D501h	D502h	D503h																					
Power On Sequence	00h	00h	00h	00h																					
S/W Reset	00h	00h	00h	00h																					
H/W Reset	00h	00h	00h	00h																					

RDVNT (DDh): Read NV Memory Flag Status

Address (MDDI I/F)		DD00h					Access Attribute				R
Address (Other I/F)		DDh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DD00h	Parameter 1	0	NV_N3	NV_N2	NV_N1	NV_N0	NV_GMA	0	NVP_F	NV_P	-

Description	<p>NV_P:</p> <p>- Both commands indicate the current status of the NV memory as shown below:</p> <table border="1"> <thead> <tr> <th>Flag</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>NV_P</td> <td>NV Memory Program Finish Status</td> <td>'0' = NV Memory Program Unready, '1' = NV Memory Program Finish.</td> </tr> </tbody> </table>	Flag	Description	Value	NV_P	NV Memory Program Finish Status	'0' = NV Memory Program Unready, '1' = NV Memory Program Finish.																							
	Flag	Description	Value																											
NV_P	NV Memory Program Finish Status	'0' = NV Memory Program Unready, '1' = NV Memory Program Finish.																												
<p>NVP_F: NV Memory Power Flag Status '0' = NV Memory External Power unready. '1' = NV Memory External Power ready.</p> <p>NV_GMA: To detect GAMMA be program or not. If NV_GMA=1,GAMMA was program already. If NV_GMA=0,GAMMA Program Unready.</p> <p>NV_N[3 : 0]: The NV_N represent the Record NV Memory Program Times</p> <table border="1"> <thead> <tr> <th>NV_N3</th> <th>NV_N2</th> <th>NV_N1</th> <th>NV_N0</th> <th>NV Memory Program Times</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 time (Default)</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1 time</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>2 times</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>3 times</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>4 times</td> </tr> </tbody> </table>	NV_N3	NV_N2	NV_N1	NV_N0	NV Memory Program Times	0	0	0	0	0 time (Default)	0	0	0	1	1 time	0	0	1	1	2 times	0	1	1	1	3 times	1	1	1	1	4 times
NV_N3	NV_N2	NV_N1	NV_N0	NV Memory Program Times																										
0	0	0	0	0 time (Default)																										
0	0	0	1	1 time																										
0	0	1	1	2 times																										
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1	1	1	1	4 times																										
Restriction	Read only																													
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Status	DD00h																													
Power On Sequence	-																													
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EPWRITE (DEh): NV Memory Write Command

Address (MDDI I/F)		DE00h					Access Attribute				W
Address (Other I/F)		DEh					Number of Parameter(s)				3
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DE00h	Parameter 1	0	0	1	0	1	0	1	0	1	55h
DE01h	Parameter 2	0	1	0	1	0	1	0	1	0	AAh
DE02h	Parameter 3	0	0	1	1	0	0	1	1	0	66h

Description	EPWRITE1-2-3: <ul style="list-style-type: none"> - These are NV memory write command. - The NV memory writing sequence: <ol style="list-style-type: none"> (1) For MDDI: (DE00h=0X0055)→(DE01h=0X00AA)→(DE02h=0X0066) (2) For other interface: DEh →0X55 → 0XAA → 0X66 																
Restriction	Write only																
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
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Status	DE00h	DE01h	DE02h														
Power On Sequence	-	-	-														
S/W Reset	-	-	-														
H/W Reset	-	-	-														

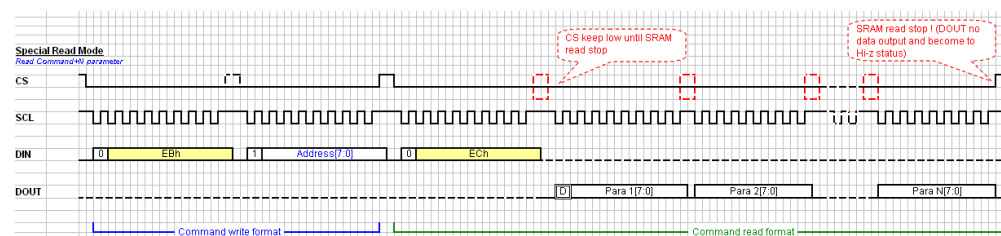
MTPPW (DFh): MTP Write function enable

Address (MIPI I/F)		DF00h					Access Attribute				R/W
Address (Other I/F)		DFh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
DF00h	Parameter 1	0	0	0	0	nROM	0	0	0	MTP_W	00h

Description	<p>MTP_W: This instruction is used to enable the MTP write function.</p> <table border="1"> <thead> <tr> <th>MTP_W</th> <th>MTP Write Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table>	MTP_W	MTP Write Function	0	Disable	1	Enable						
	MTP_W	MTP Write Function											
0	Disable												
1	Enable												
<p>nROM: The nROM is used to set MTP reload or not after SLPOUT.</p> <table border="1"> <thead> <tr> <th>nROM</th> <th>MTP Source</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Reload MTP after SLPOUT (Default)</td> </tr> <tr> <td>1</td> <td>Don't Reload MTP after SLPOUT</td> </tr> </tbody> </table>	nROM	MTP Source	0	Reload MTP after SLPOUT (Default)	1	Don't Reload MTP after SLPOUT							
nROM	MTP Source												
0	Reload MTP after SLPOUT (Default)												
1	Don't Reload MTP after SLPOUT												
Restriction	Write only												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	DF00h												
Power On Sequence	00h												
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H/W Reset	00h												

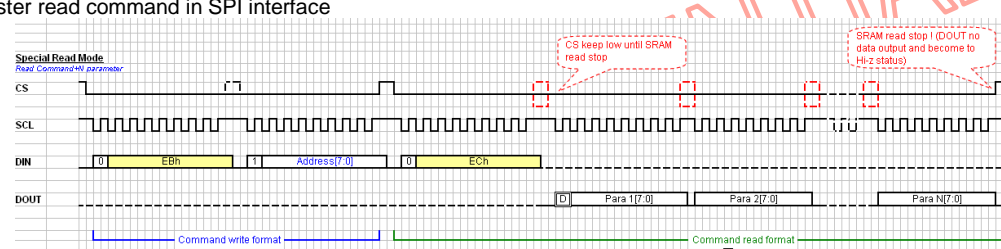
RDREGEXT1 (EBh) : Register read command in SPI interface

Address (MDDI I/F)	Not Support				Access Attribute				R/W
Address (Other I/F)	EBh				Number of Parameter(s)				1
Parameter (SPI I/F)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	Add7	Add6	Add5	Add4	Add3	Add2	Add1	Add0	-

Description	<p>Register read command in SPI interface</p> 												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value D[15 : 0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> </tr> </tbody> </table>	Status	Default Value D[15 : 0]	Power On Sequence	0000h	S/W Reset	0000h	H/W Reset	0000h				
Status	Default Value D[15 : 0]												
Power On Sequence	0000h												
S/W Reset	0000h												
H/W Reset	0000h												

RDREGEXT2 (ECh) : Register read command in SPI interface

Address (MDDI I/F)	Not Support				Access Attribute				R
Address (Other I/F)	ECh				Number of Parameter(s)				N
Parameter (SPI I/F)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
Parameter 1	Para17	Para16	Para15	Para14	Para13	Para12	Para11	Para10	-
Parameter 2	Para27	Para26	Para25	Para24	Para23	Para22	Para21	Para20	-
:	:	:	:	:	:	:	:	:	-
Parameter N	ParaN7	ParaN6	ParaN5	ParaN4	ParaN3	ParaN2	ParaN1	ParaN0	-

Description	<p>Register read command in SPI interface</p> 												
	Restriction												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value D[15 : 0]												
Power On Sequence	0000h												
S/W Reset	0000h												
H/W Reset	0000h												

PAGE_LOCK (EFh) : Set the Register to command1

Address (MDDI I/F)		EF00h					Access Attribute				W
Address (Other I/F)		EFh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
EF00h	Parameter 1	0	1	0	1	0	1	0	1	0	AAh

Description	This command is used for LOCK of CMD2 register access.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value D[15 : 0]													
Power On Sequence	-													
S/W Reset	-													
H/W Reset	-													

PAGE_LOCK (BFh) : Set the Register to command2 Page 1

Address (MDDI I/F)		BF00h					Access Attribute				W
Address (Other I/F)		BFh					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
BF00h	Parameter 1	0	1	0	1	0	1	0	1	0	AAh

Description	This command is used for goto CMD2_P1 register access.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value D[15 : 0]													
Power On Sequence	-													
S/W Reset	-													
H/W Reset	-													

6.3 CMD2_P1 register list

Inst / Para	Addr.	R/W	Parameter	D7	D6	D5	D4	D3	D2	D1	D0	Code	MTP
GMACTRL1 (Must set reg APR2_EN = 1)	E0h	R/W	1	VP0[7]	VP0[6]	VP0[5]	VP0[4]	VP0[3]	VP0[2]	VP0[1]	VP0[0]	01h	V
			2	0	0	0	0	0	0	0	0		
		R/W	3	VP1[7]	VP1[6]	VP1[5]	VP1[4]	VP1[3]	VP1[2]	VP1[1]	VP1[0]	19h	
			4	0	0	0	0	0	0	0	0		
		R/W	5	VP2[7]	VP2[6]	VP2[5]	VP2[4]	VP2[3]	VP2[2]	VP2[1]	VP2[0]	25h	
			6	0	0	0	0	0	0	0	0		
		R/W	7	VP4[7]	VP4[6]	VP4[5]	VP4[4]	VP4[3]	VP4[2]	VP4[1]	VP4[0]	3Eh	
			8	0	0	0	0	0	0	0	0		
		R/W	9	VP6[7]	VP6[6]	VP6[5]	VP6[4]	VP6[3]	VP6[2]	VP6[1]	VP6[0]	4Ah	
			10	0	0	0	0	0	0	0	0		
		R/W	11	VP8[7]	VP8[6]	VP8[5]	VP8[4]	VP8[3]	VP8[2]	VP8[1]	VP8[0]	55h	
			12	0	0	0	0	0	0	0	0		
		R/W	13	VP12[7]	VP12[6]	VP12[5]	VP12[4]	VP12[3]	VP12[2]	VP12[1]	VP12[0]	66h	
			14	0	0	0	0	0	0	0	0		
		R/W	15	VP20[7]	VP20[6]	VP20[5]	VP20[4]	VP20[3]	VP20[2]	VP20[1]	VP20[0]	7Ch	
			16	0	0	0	0	0	0	0	0		
		R/W	17	VP28[7]	VP28[6]	VP28[5]	VP28[4]	VP28[3]	VP28[2]	VP28[1]	VP28[0]	8Dh	
			18	0	0	0	0	0	0	0	0		
		R/W	19	VP36 [7]	VP36 [6]	VP36 [5]	VP36 [4]	VP36 [3]	VP36 [2]	VP36 [1]	VP36 [0]	9Eh	
			20	0	0	0	0	0	0	0	0		
		R/W	21	VP44[7]	VP44[6]	VP44[5]	VP44[4]	VP44[3]	VP44[2]	VP44[1]	VP44[0]	ACH	
			22	0	0	0	0	0	0	0	0		
		R/W	23	VP52[7]	VP52[6]	VP52[5]	VP52[4]	VP52[3]	VP52[2]	VP52[1]	VP52[0]	Bfh	
			24	0	0	0	0	0	0	0	0		
		R/W	25	VP56[7]	VP56[6]	VP56[5]	VP56[4]	VP56[3]	VP56[2]	VP56[1]	VP56[0]	CAh	
			26	0	0	0	0	0	0	0	0		
		R/W	27	VP58[7]	VP58[6]	VP58[5]	VP58[4]	VP58[3]	VP58[2]	VP58[1]	VP58[0]	D3h	
			28	0	0	0	0	0	0	0	0		
		R/W	29	VP60[7]	VP60[6]	VP60[5]	VP60[4]	VP60[3]	VP60[2]	VP60[1]	VP60[0]	DDh	
			30	0	0	0	0	0	0	0	0		
		R/W	31	VP61[7]	VP61[6]	VP61[5]	VP61[4]	VP61[3]	VP61[2]	VP61[1]	VP61[0]	E2h	
			32	0	0	0	0	0	0	0	0		
		R/W	33	VP62[7]	VP62[6]	VP62[5]	VP62[4]	VP62[3]	VP62[2]	VP62[1]	VP62[0]	E9h	
			34	0	0	0	0	0	0	0	0		
		R/W	35	VP63[7]	VP63[6]	VP63[5]	VP63[4]	VP63[3]	VP63[2]	VP63[1]	VP63[0]	F3h	
			36	0	0	0	0	0	0	0	0		
GMACTRL2 (Must set reg APR2_EN = 1)	E1h	R/W	1	VN0[7]	VN0[6]	VN0[5]	VN0[4]	VN0[3]	VN0[2]	VN0[1]	VN0[0]	00h	V
			2	0	0	0	0	0	0	0	0		
		R/W	3	VN1[7]	VN1[6]	VN1[5]	VN1[4]	VN1[3]	VN1[2]	VN1[1]	VN1[0]	19h	
			4	0	0	0	0	0	0	0	0		
		R/W	5	VN2[7]	VN2[6]	VN2[5]	VN2[4]	VN2[3]	VN2[2]	VN2[1]	VN2[0]	25h	
			6	0	0	0	0	0	0	0	0		
		R/W	7	VN4[7]	VN4[6]	VN4[5]	VN4[4]	VN4[3]	VN4[2]	VN4[1]	VN4[0]	3Eh	
			8	0	0	0	0	0	0	0	0		

	R/W	9	VN6[7]	VN6[6]	VN6[5]	VN6[4]	VN6[3]	VN6[2]	VN6[1]	VN6[0]	4Ah			
		10	0	0	0	0	0	0	0	0				
	R/W	11	VN8[7]	VN8[6]	VN8[5]	VN8[4]	VN8[3]	VN8[2]	VN8[1]	VN8[0]	55h			
		12	0	0	0	0	0	0	0	0				
	R/W	13	VN12[7]	VN12[6]	VN12[5]	VN12[4]	VN12[3]	VN12[2]	VN12[1]	VN12[0]	66h			
		14	0	0	0	0	0	0	0	0				
	R/W	15	VN20[7]	VN20[6]	VN20[5]	VN20[4]	VN20[3]	VN20[2]	VN20[1]	VN20[0]	7Ch			
		16	0	0	0	0	0	0	0	0				
	R/W	17	VN28[7]	VN28[6]	VN28[5]	VN28[4]	VN28[3]	VN28[2]	VN28[1]	VN28[0]	8Dh			
		18	0	0	0	0	0	0	0	0				
	R/W	19	VN36 [7]	VN36 [6]	VN36 [5]	VN36 [4]	VN36 [3]	VN36 [2]	VN36 [1]	VN36 [0]	9Eh			
		20	0	0	0	0	0	0	0	0				
	R/W	21	VN44[7]	VN44[6]	VN44[5]	VN44[4]	VN44[3]	VN44[2]	VN44[1]	VN44[0]	ACh			
		22	0	0	0	0	0	0	0	0				
	R/W	23	VN52[7]	VN52[6]	VN52[5]	VN52[4]	VN52[3]	VN52[2]	VN52[1]	VN52[0]	BFh			
		24	0	0	0	0	0	0	0	0				
	R/W	25	VN56[7]	VN56[6]	VN56[5]	VN56[4]	VN56[3]	VN56[2]	VN56[1]	VN56[0]	CAh			
		26	0	0	0	0	0	0	0	0				
	R/W	27	VN58[7]	VN58[6]	VN58[5]	VN58[4]	VN58[3]	VN58[2]	VN58[1]	VN58[0]	D3h			
		28	0	0	0	0	0	0	0	0				
	R/W	29	VN60[7]	VN60[6]	VN60[5]	VN60[4]	VN60[3]	VN60[2]	VN60[1]	VN60[0]	DDh			
		30	0	0	0	0	0	0	0	0				
	R/W	31	VN61[7]	VN61[6]	VN61[5]	VN61[4]	VN61[3]	VN61[2]	VN61[1]	VN61[0]	E2h			
		32	0	0	0	0	0	0	0	0				
	R/W	33	VN62[7]	VN62[6]	VN62[5]	VN62[4]	VN62[3]	VN62[2]	VN62[1]	VN62[0]	E9h			
		34	0	0	0	0	0	0	0	0				
	R/W	35	VN63[7]	VN63[6]	VN63[5]	VN63[4]	VN63[3]	VN63[2]	VN63[1]	VN63[0]	F3h			
		36	0	0	0	0	0	0	0	0				
GMACTRL3 (Must set reg APR2_EN = 1)	E2h	R/W	1	VP0[7]	VP0[6]	VP0[5]	VP0[4]	VP0[3]	VP0[2]	VP0[1]	VP0[0]	01h	V	
			2	0	0	0	0	0	0	0	0			
		R/W	3	VP1[7]	VP1[6]	VP1[5]	VP1[4]	VP1[3]	VP1[2]	VP1[1]	VP1[0]	19h		
			4	0	0	0	0	0	0	0	0			
		R/W	5	VP2[7]	VP2[6]	VP2[5]	VP2[4]	VP2[3]	VP2[2]	VP2[1]	VP2[0]	25h		
			6	0	0	0	0	0	0	0	0			
		R/W	7	VP4[7]	VP4[6]	VP4[5]	VP4[4]	VP4[3]	VP4[2]	VP4[1]	VP4[0]	3Eh		
			8	0	0	0	0	0	0	0	0			
		R/W	9	VP6[7]	VP6[6]	VP6[5]	VP6[4]	VP6[3]	VP6[2]	VP6[1]	VP6[0]	4Ah		
			10	0	0	0	0	0	0	0	0			
		R/W	11	VP8[7]	VP8[6]	VP8[5]	VP8[4]	VP8[3]	VP8[2]	VP8[1]	VP8[0]	55h		
			12	0	0	0	0	0	0	0	0			
		R/W	13	VP12[7]	VP12[6]	VP12[5]	VP12[4]	VP12[3]	VP12[2]	VP12[1]	VP12[0]	66h		
			14	0	0	0	0	0	0	0	0			
		R/W	15	VP20[7]	VP20[6]	VP20[5]	VP20[4]	VP20[3]	VP20[2]	VP20[1]	VP20[0]	7Ch		
			16	0	0	0	0	0	0	0	0			
		R/W	17	VP28[7]	VP28[6]	VP28[5]	VP28[4]	VP28[3]	VP28[2]	VP28[1]	VP28[0]	8Dh		
			18	0	0	0	0	0	0	0	0			

	R/W	19	VP36 [7]	VP36 [6]	VP36 [5]	VP36 [4]	VP36 [3]	VP36 [2]	VP36 [1]	VP36 [0]	9Eh			
		20	0	0	0	0	0	0	0	0				
	R/W	21	VP44[7]	VP44[6]	VP44[5]	VP44[4]	VP44[3]	VP44[2]	VP44[1]	VP44[0]	ACh			
		22	0	0	0	0	0	0	0	0				
	R/W	23	VP52[7]	VP52[6]	VP52[5]	VP52[4]	VP52[3]	VP52[2]	VP52[1]	VP52[0]	BFh			
		24	0	0	0	0	0	0	0	0				
	R/W	25	VP56[7]	VP56[6]	VP56[5]	VP56[4]	VP56[3]	VP56[2]	VP56[1]	VP56[0]	CAh			
		26	0	0	0	0	0	0	0	0				
	R/W	27	VP58[7]	VP58[6]	VP58[5]	VP58[4]	VP58[3]	VP58[2]	VP58[1]	VP58[0]	D3h			
		28	0	0	0	0	0	0	0	0				
	R/W	29	VP60[7]	VP60[6]	VP60[5]	VP60[4]	VP60[3]	VP60[2]	VP60[1]	VP60[0]	DDh			
		30	0	0	0	0	0	0	0	0				
	R/W	31	VP61[7]	VP61[6]	VP61[5]	VP61[4]	VP61[3]	VP61[2]	VP61[1]	VP61[0]	E2h			
		32	0	0	0	0	0	0	0	0				
	R/W	33	VP62[7]	VP62[6]	VP62[5]	VP62[4]	VP62[3]	VP62[2]	VP62[1]	VP62[0]	E9h			
		34	0	0	0	0	0	0	0	0				
	R/W	35	VP63[7]	VP63[6]	VP63[5]	VP63[4]	VP63[3]	VP63[2]	VP63[1]	VP63[0]	F3h			
		36	0	0	0	0	0	0	0	0				
GMACTRL4 (Must set reg APR2_EN = 1)	E3h	R/W	1	VN0[7]	VN0[6]	VN0[5]	VN0[4]	VN0[3]	VN0[2]	VN0[1]	VN0[0]	00h	V	
			2	0	0	0	0	0	0	0	0			
		R/W	3	VN1[7]	VN1[6]	VN1[5]	VN1[4]	VN1[3]	VN1[2]	VN1[1]	VN1[0]	19h		
			4	0	0	0	0	0	0	0	0			
		R/W	5	VN2[7]	VN2[6]	VN2[5]	VN2[4]	VN2[3]	VN2[2]	VN2[1]	VN2[0]	25h		
			6	0	0	0	0	0	0	0	0			
		R/W	7	VN4[7]	VN4[6]	VN4[5]	VN4[4]	VN4[3]	VN4[2]	VN4[1]	VN4[0]	3Eh		
			8	0	0	0	0	0	0	0	0			
		R/W	9	VN6[7]	VN6[6]	VN6[5]	VN6[4]	VN6[3]	VN6[2]	VN6[1]	VN6[0]	4Ah		
			10	0	0	0	0	0	0	0	0			
		R/W	11	VN8[7]	VN8[6]	VN8[5]	VN8[4]	VN8[3]	VN8[2]	VN8[1]	VN8[0]	55h		
			12	0	0	0	0	0	0	0	0			
		R/W	13	VN12[7]	VN12[6]	VN12[5]	VN12[4]	VN12[3]	VN12[2]	VN12[1]	VN12[0]	66h		
			14	0	0	0	0	0	0	0	0			
		R/W	15	VN20[7]	VN20[6]	VN20[5]	VN20[4]	VN20[3]	VN20[2]	VN20[1]	VN20[0]	7Ch		
			16	0	0	0	0	0	0	0	0			
		R/W	17	VN28[7]	VN28[6]	VN28[5]	VN28[4]	VN28[3]	VN28[2]	VN28[1]	VN28[0]	8Dh		
			18	0	0	0	0	0	0	0	0			
		R/W	19	VN36 [7]	VN36 [6]	VN36 [5]	VN36 [4]	VN36 [3]	VN36 [2]	VN36 [1]	VN36 [0]	9Eh		
			20	0	0	0	0	0	0	0	0			
		R/W	21	VN44[7]	VN44[6]	VN44[5]	VN44[4]	VN44[3]	VN44[2]	VN44[1]	VN44[0]	ACh		
			22	0	0	0	0	0	0	0	0			
		R/W	23	VN52[7]	VN52[6]	VN52[5]	VN52[4]	VN52[3]	VN52[2]	VN52[1]	VN52[0]	BFh		
			24	0	0	0	0	0	0	0	0			
		R/W	25	VN56[7]	VN56[6]	VN56[5]	VN56[4]	VN56[3]	VN56[2]	VN56[1]	VN56[0]	CAh		
			26	0	0	0	0	0	0	0	0			
		R/W	27	VN58[7]	VN58[6]	VN58[5]	VN58[4]	VN58[3]	VN58[2]	VN58[1]	VN58[0]	D3h		
			28	0	0	0	0	0	0	0	0			

	R/W	29	VN60[7]	VN60[6]	VN60[5]	VN60[4]	VN60[3]	VN60[2]	VN60[1]	VN60[0]	DDh		
		30	0	0	0	0	0	0	0	0			
	R/W	31	VN61[7]	VN61[6]	VN61[5]	VN61[4]	VN61[3]	VN61[2]	VN61[1]	VN61[0]	E2h		
		32	0	0	0	0	0	0	0	0			
	R/W	33	VN62[7]	VN62[6]	VN62[5]	VN62[4]	VN62[3]	VN62[2]	VN62[1]	VN62[0]	E9h		
		34	0	0	0	0	0	0	0	0			
	R/W	35	VN63[7]	VN63[6]	VN63[5]	VN63[4]	VN63[3]	VN63[2]	VN63[1]	VN63[0]	F3h		
	36	0	0	0	0	0	0	0	0				
GMACTRL5 (Must set reg APR2_EN = 1)	E4h	R/W	1	VP0[7]	VP0[6]	VP0[5]	VP0[4]	VP0[3]	VP0[2]	VP0[1]	VP0[0]	01h	V
			2	0	0	0	0	0	0	0	0		
		R/W	3	VP1[7]	VP1[6]	VP1[5]	VP1[4]	VP1[3]	VP1[2]	VP1[1]	VP1[0]	19h	
			4	0	0	0	0	0	0	0	0		
		R/W	5	VP2[7]	VP2[6]	VP2[5]	VP2[4]	VP2[3]	VP2[2]	VP2[1]	VP2[0]	25h	
			6	0	0	0	0	0	0	0	0		
		R/W	7	VP4[7]	VP4[6]	VP4[5]	VP4[4]	VP4[3]	VP4[2]	VP4[1]	VP4[0]	3Eh	
			8	0	0	0	0	0	0	0	0		
		R/W	9	VP6[7]	VP6[6]	VP6[5]	VP6[4]	VP6[3]	VP6[2]	VP6[1]	VP6[0]	4Ah	
			10	0	0	0	0	0	0	0	0		
		R/W	11	VP8[7]	VP8[6]	VP8[5]	VP8[4]	VP8[3]	VP8[2]	VP8[1]	VP8[0]	55h	
			12	0	0	0	0	0	0	0	0		
		R/W	13	VP12[7]	VP12[6]	VP12[5]	VP12[4]	VP12[3]	VP12[2]	VP12[1]	VP12[0]	66h	
			14	0	0	0	0	0	0	0	0		
		R/W	15	VP20[7]	VP20[6]	VP20[5]	VP20[4]	VP20[3]	VP20[2]	VP20[1]	VP20[0]	7Ch	
			16	0	0	0	0	0	0	0	0		
		R/W	17	VP28[7]	VP28[6]	VP28[5]	VP28[4]	VP28[3]	VP28[2]	VP28[1]	VP28[0]	8Dh	
			18	0	0	0	0	0	0	0	0		
		R/W	19	VP36 [7]	VP36 [6]	VP36 [5]	VP36 [4]	VP36 [3]	VP36 [2]	VP36 [1]	VP36 [0]	9Eh	
			20	0	0	0	0	0	0	0	0		
		R/W	21	VP44[7]	VP44[6]	VP44[5]	VP44[4]	VP44[3]	VP44[2]	VP44[1]	VP44[0]	ACCh	
			22	0	0	0	0	0	0	0	0		
		R/W	23	VP52[7]	VP52[6]	VP52[5]	VP52[4]	VP52[3]	VP52[2]	VP52[1]	VP52[0]	BFh	
			24	0	0	0	0	0	0	0	0		
		R/W	25	VP56[7]	VP56[6]	VP56[5]	VP56[4]	VP56[3]	VP56[2]	VP56[1]	VP56[0]	CAh	
			26	0	0	0	0	0	0	0	0		
		R/W	27	VP58[7]	VP58[6]	VP58[5]	VP58[4]	VP58[3]	VP58[2]	VP58[1]	VP58[0]	D3h	
			28	0	0	0	0	0	0	0	0		
		R/W	29	VP60[7]	VP60[6]	VP60[5]	VP60[4]	VP60[3]	VP60[2]	VP60[1]	VP60[0]	DDh	
			30	0	0	0	0	0	0	0	0		
		R/W	31	VP61[7]	VP61[6]	VP61[5]	VP61[4]	VP61[3]	VP61[2]	VP61[1]	VP61[0]	E2h	
			32	0	0	0	0	0	0	0	0		
		R/W	33	VP62[7]	VP62[6]	VP62[5]	VP62[4]	VP62[3]	VP62[2]	VP62[1]	VP62[0]	E9h	
			34	0	0	0	0	0	0	0	0		
		R/W	35	VP63[7]	VP63[6]	VP63[5]	VP63[4]	VP63[3]	VP63[2]	VP63[1]	VP63[0]	F3h	
			36	0	0	0	0	0	0	0	0		
GMACTRL6 (Must set reg APR2_EN = 1)	E5h	R/W	1	VN0[7]	VN0[6]	VN0[5]	VN0[4]	VN0[3]	VN0[2]	VN0[1]	VN0[0]	00h	V
			2	0	0	0	0	0	0	0	0		

	R/W	3	VN1[7]	VN1[6]	VN1[5]	VN1[4]	VN1[3]	VN1[2]	VN1[1]	VN1[0]	19h		
		4	0	0	0	0	0	0	0	0			
	R/W	5	VN2[7]	VN2[6]	VN2[5]	VN2[4]	VN2[3]	VN2[2]	VN2[1]	VN2[0]	25h		
		6	0	0	0	0	0	0	0	0			
	R/W	7	VN4[7]	VN4[6]	VN4[5]	VN4[4]	VN4[3]	VN4[2]	VN4[1]	VN4[0]	3Eh		
		8	0	0	0	0	0	0	0	0			
	R/W	9	VN6[7]	VN6[6]	VN6[5]	VN6[4]	VN6[3]	VN6[2]	VN6[1]	VN6[0]	4Ah		
		10	0	0	0	0	0	0	0	0			
	R/W	11	VN8[7]	VN8[6]	VN8[5]	VN8[4]	VN8[3]	VN8[2]	VN8[1]	VN8[0]	55h		
		12	0	0	0	0	0	0	0	0			
	R/W	13	VN12[7]	VN12[6]	VN12[5]	VN12[4]	VN12[3]	VN12[2]	VN12[1]	VN12[0]	66h		
		14	0	0	0	0	0	0	0	0			
	R/W	15	VN20[7]	VN20[6]	VN20[5]	VN20[4]	VN20[3]	VN20[2]	VN20[1]	VN20[0]	7Ch		
		16	0	0	0	0	0	0	0	0			
	R/W	17	VN28[7]	VN28[6]	VN28[5]	VN28[4]	VN28[3]	VN28[2]	VN28[1]	VN28[0]	8Dh		
		18	0	0	0	0	0	0	0	0			
	R/W	19	VN36 [7]	VN36 [6]	VN36 [5]	VN36 [4]	VN36 [3]	VN36 [2]	VN36 [1]	VN36 [0]	9Eh		
		20	0	0	0	0	0	0	0	0			
	R/W	21	VN44[7]	VN44[6]	VN44[5]	VN44[4]	VN44[3]	VN44[2]	VN44[1]	VN44[0]	ACh		
		22	0	0	0	0	0	0	0	0			
	R/W	23	VN52[7]	VN52[6]	VN52[5]	VN52[4]	VN52[3]	VN52[2]	VN52[1]	VN52[0]	BFh		
		24	0	0	0	0	0	0	0	0			
	R/W	25	VN56[7]	VN56[6]	VN56[5]	VN56[4]	VN56[3]	VN56[2]	VN56[1]	VN56[0]	CAh		
		26	0	0	0	0	0	0	0	0			
	R/W	27	VN58[7]	VN58[6]	VN58[5]	VN58[4]	VN58[3]	VN58[2]	VN58[1]	VN58[0]	D3h		
		28	0	0	0	0	0	0	0	0			
	R/W	29	VN60[7]	VN60[6]	VN60[5]	VN60[4]	VN60[3]	VN60[2]	VN60[1]	VN60[0]	DDh		
		30	0	0	0	0	0	0	0	0			
	R/W	31	VN61[7]	VN61[6]	VN61[5]	VN61[4]	VN61[3]	VN61[2]	VN61[1]	VN61[0]	E2h		
		32	0	0	0	0	0	0	0	0			
	R/W	33	VN62[7]	VN62[6]	VN62[5]	VN62[4]	VN62[3]	VN62[2]	VN62[1]	VN62[0]	E9h		
		34	0	0	0	0	0	0	0	0			
	R/W	35	VN63[7]	VN63[6]	VN63[5]	VN63[4]	VN63[3]	VN63[2]	VN63[1]	VN63[0]	F3h		
		36	0	0	0	0	0	0	0	0			
CABC Gamma offset (R+/R-) (Must set reg APR2_EN = 1)	E6h	R/W	1	VN_OFF1[3]	VN_OFF1[2]	VN_OFF1[1]	VN_OFF1[0]	VP_OFF1[3]	VP_OFF1[2]	VP_OFF1[1]	VP_OFF1[0]	22h	V
			2	0	0	0	0	0	0	0	0		
		R/W	3	VN_OFF2[3]	VN_OFF2[2]	VN_OFF2[1]	VN_OFF2[0]	VP_OFF2[3]	VP_OFF2[2]	VP_OFF2[1]	VP_OFF2[0]	44h	
			4	0	0	0	0	0	0	0	0		
		R/W	5	VN_OFF4[3]	VN_OFF4[2]	VN_OFF4[1]	VN_OFF4[0]	VP_OFF4[3]	VP_OFF4[2]	VP_OFF4[1]	VP_OFF4[0]	44h	
			6	0	0	0	0	0	0	0	0		
		R/W	7	VN_OFF6[3]	VN_OFF6[2]	VN_OFF6[1]	VN_OFF6[0]	VP_OFF6[3]	VP_OFF6[2]	VP_OFF6[1]	VP_OFF6[0]	66h	
			8	0	0	0	0	0	0	0	0		
		R/W	9	VN_OFF8[3]	VN_OFF8[2]	VN_OFF8[1]	VN_OFF8[0]	VP_OFF8[3]	VP_OFF8[2]	VP_OFF8[1]	VP_OFF8[0]	66h	
			10	0	0	0	0	0	0	0	0		
		R/W	11	VN_OFF12[3]	VN_OFF12[2]	VN_OFF12[1]	VN_OFF12[0]	VP_OFF12[3]	VP_OFF12[2]	VP_OFF12[1]	VP_OFF12[0]	77h	
			12	0	0	0	0	0	0	0	0		

	R/W	13	VN_OFF20[3]	VN_OFF20[2]	VN_OFF20[1]	VN_OFF20[0]	VP_OFF20[3]	VP_OFF20[2]	VP_OFF20[1]	VP_OFF20[0]	77h			
		14	0	0	0	0	0	0	0	0				
	R/W	15	VN_OFF28[3]	VN_OFF28[2]	VN_OFF28[1]	VN_OFF28[0]	VP_OFF28[3]	VP_OFF28[2]	VP_OFF28[1]	VP_OFF28[0]	AAh			
		16												
	R/W	17	VN_OFF36[3]	VN_OFF36[2]	VN_OFF36[1]	VN_OFF36[0]	VP_OFF36[3]	VP_OFF36[2]	VP_OFF36[1]	VP_OFF36[0]	BBh			
		18	0	0	0	0	0	0	0	0				
	R/W	19	VN_OFF44[3]	VN_OFF44[2]	VN_OFF44[1]	VN_OFF44[0]	VP_OFF44[3]	VP_OFF44[2]	VP_OFF44[1]	VP_OFF44[0]	99h			
		20												
	R/W	21	VN_OFF52[3]	VN_OFF52[2]	VN_OFF52[1]	VN_OFF52[0]	VP_OFF52[3]	VP_OFF52[2]	VP_OFF52[1]	VP_OFF52[0]	76h			
		22	0	0	0	0	0	0	0	0				
	R/W	23	VN_OFF56[3]	VN_OFF56[2]	VN_OFF56[1]	VN_OFF56[0]	VP_OFF56[3]	VP_OFF56[2]	VP_OFF56[1]	VP_OFF56[0]	87h			
		24												
	R/W	25	VN_OFF58[3]	VN_OFF58[2]	VN_OFF58[1]	VN_OFF58[0]	VP_OFF58[3]	VP_OFF58[2]	VP_OFF58[1]	VP_OFF58[0]	45h			
		26	0	0	0	0	0	0	0	0				
	R/W	27	VN_OFF60[3]	VN_OFF60[2]	VN_OFF60[1]	VN_OFF60[0]	VP_OFF60[3]	VP_OFF60[2]	VP_OFF60[1]	VP_OFF60[0]	43h			
		28												
	R/W	29	VN_OFF61[3]	VN_OFF61[2]	VN_OFF61[1]	VN_OFF61[0]	VP_OFF61[3]	VP_OFF61[2]	VP_OFF61[1]	VP_OFF61[0]	33h			
		30	0	0	0	0	0	0	0	0				
	R/W	31	VN_OFF62[3]	VN_OFF62[2]	VN_OFF62[1]	VN_OFF62[0]	VP_OFF62[3]	VP_OFF62[2]	VP_OFF62[1]	VP_OFF62[0]	32h			
		32	0	0	0	0	0	0	0	0				
CABC Gamma offset (R+/R-) (Must set reg APR2_EN = 1)	E7h	R/W	1	VN_OFF1[3]	VN_OFF1[2]	VN_OFF1[1]	VN_OFF1[0]	VP_OFF1[3]	VP_OFF1[2]	VP_OFF1[1]	VP_OFF1[0]	22h	V	
			2	0	0	0	0	0	0	0	0			
			R/W	3	VN_OFF2[3]	VN_OFF2[2]	VN_OFF2[1]	VN_OFF2[0]	VP_OFF2[3]	VP_OFF2[2]	VP_OFF2[1]	VP_OFF2[0]		44h
				4	0	0	0	0	0	0	0			
			R/W	5	VN_OFF4[3]	VN_OFF4[2]	VN_OFF4[1]	VN_OFF4[0]	VP_OFF4[3]	VP_OFF4[2]	VP_OFF4[1]	VP_OFF4[0]		44h
				6	0	0	0	0	0	0	0			
			R/W	7	VN_OFF6[3]	VN_OFF6[2]	VN_OFF6[1]	VN_OFF6[0]	VP_OFF6[3]	VP_OFF6[2]	VP_OFF6[1]	VP_OFF6[0]		66h
				8	0	0	0	0	0	0	0			
			R/W	9	VN_OFF8[3]	VN_OFF8[2]	VN_OFF8[1]	VN_OFF8[0]	VP_OFF8[3]	VP_OFF8[2]	VP_OFF8[1]	VP_OFF8[0]		66h
				10	0	0	0	0	0	0	0			
			R/W	11	VN_OFF12[3]	VN_OFF12[2]	VN_OFF12[1]	VN_OFF12[0]	VP_OFF12[3]	VP_OFF12[2]	VP_OFF12[1]	VP_OFF12[0]		77h
				12	0	0	0	0	0	0	0			
			R/W	13	VN_OFF20[3]	VN_OFF20[2]	VN_OFF20[1]	VN_OFF20[0]	VP_OFF20[3]	VP_OFF20[2]	VP_OFF20[1]	VP_OFF20[0]		77h
				14	0	0	0	0	0	0	0			
			R/W	15	VN_OFF28[3]	VN_OFF28[2]	VN_OFF28[1]	VN_OFF28[0]	VP_OFF28[3]	VP_OFF28[2]	VP_OFF28[1]	VP_OFF28[0]		AAh
				16										
			R/W	17	VN_OFF36[3]	VN_OFF36[2]	VN_OFF36[1]	VN_OFF36[0]	VP_OFF36[3]	VP_OFF36[2]	VP_OFF36[1]	VP_OFF36[0]		BBh
				18	0	0	0	0	0	0	0			
			R/W	19	VN_OFF44[3]	VN_OFF44[2]	VN_OFF44[1]	VN_OFF44[0]	VP_OFF44[3]	VP_OFF44[2]	VP_OFF44[1]	VP_OFF44[0]		99h
				20										
			R/W	21	VN_OFF52[3]	VN_OFF52[2]	VN_OFF52[1]	VN_OFF52[0]	VP_OFF52[3]	VP_OFF52[2]	VP_OFF52[1]	VP_OFF52[0]		76h
				22	0	0	0	0	0	0	0			
			R/W	23	VN_OFF56[3]	VN_OFF56[2]	VN_OFF56[1]	VN_OFF56[0]	VP_OFF56[3]	VP_OFF56[2]	VP_OFF56[1]	VP_OFF56[0]		87h
				24										
			R/W	25	VN_OFF58[3]	VN_OFF58[2]	VN_OFF58[1]	VN_OFF58[0]	VP_OFF58[3]	VP_OFF58[2]	VP_OFF58[1]	VP_OFF58[0]		45h
				26	0	0	0	0	0	0	0			

CABC Gamma offset (R+/R-) (Must set reg APR2_EN = 1)	E8h	R/W	27	VN_OFF60[3]	VN_OFF60[2]	VN_OFF60[1]	VN_OFF60[0]	VP_OFF60[3]	VP_OFF60[2]	VP_OFF60[1]	VP_OFF60[0]	43h	V	
			28											
		R/W	29	VN_OFF61[3]	VN_OFF61[2]	VN_OFF61[1]	VN_OFF61[0]	VP_OFF61[3]	VP_OFF61[2]	VP_OFF61[1]	VP_OFF61[0]	33h		
			30	0	0	0	0	0	0	0	0	0		
		R/W	31	VN_OFF62[3]	VN_OFF62[2]	VN_OFF62[1]	VN_OFF62[0]	VP_OFF62[3]	VP_OFF62[2]	VP_OFF62[1]	VP_OFF62[0]	32h		
			32	0	0	0	0	0	0	0	0	0		
		R/W	1	VN_OFF1[3]	VN_OFF1[2]	VN_OFF1[1]	VN_OFF1[0]	VP_OFF1[3]	VP_OFF1[2]	VP_OFF1[1]	VP_OFF1[0]	22h		
			2	0	0	0	0	0	0	0	0	0		
		R/W	3	VN_OFF2[3]	VN_OFF2[2]	VN_OFF2[1]	VN_OFF2[0]	VP_OFF2[3]	VP_OFF2[2]	VP_OFF2[1]	VP_OFF2[0]	44h		
			4	0	0	0	0	0	0	0	0	0		
		R/W	5	VN_OFF4[3]	VN_OFF4[2]	VN_OFF4[1]	VN_OFF4[0]	VP_OFF4[3]	VP_OFF4[2]	VP_OFF4[1]	VP_OFF4[0]	44h		
			6	0	0	0	0	0	0	0	0	0		
		R/W	7	VN_OFF6[3]	VN_OFF6[2]	VN_OFF6[1]	VN_OFF6[0]	VP_OFF6[3]	VP_OFF6[2]	VP_OFF6[1]	VP_OFF6[0]	66h		
			8	0	0	0	0	0	0	0	0	0		
		R/W	9	VN_OFF8[3]	VN_OFF8[2]	VN_OFF8[1]	VN_OFF8[0]	VP_OFF8[3]	VP_OFF8[2]	VP_OFF8[1]	VP_OFF8[0]	66h		
			10	0	0	0	0	0	0	0	0	0		
		R/W	11	VN_OFF12[3]	VN_OFF12[2]	VN_OFF12[1]	VN_OFF12[0]	VP_OFF12[3]	VP_OFF12[2]	VP_OFF12[1]	VP_OFF12[0]	77h		
			12	0	0	0	0	0	0	0	0	0		
		R/W	13	VN_OFF20[3]	VN_OFF20[2]	VN_OFF20[1]	VN_OFF20[0]	VP_OFF20[3]	VP_OFF20[2]	VP_OFF20[1]	VP_OFF20[0]	77h		
			14	0	0	0	0	0	0	0	0	0		
		R/W	15	VN_OFF28[3]	VN_OFF28[2]	VN_OFF28[1]	VN_OFF28[0]	VP_OFF28[3]	VP_OFF28[2]	VP_OFF28[1]	VP_OFF28[0]	AAh		
			16											
		R/W	17	VN_OFF36[3]	VN_OFF36[2]	VN_OFF36[1]	VN_OFF36[0]	VP_OFF36[3]	VP_OFF36[2]	VP_OFF36[1]	VP_OFF36[0]	BBh		
			18	0	0	0	0	0	0	0	0	0		
		R/W	19	VN_OFF44[3]	VN_OFF44[2]	VN_OFF44[1]	VN_OFF44[0]	VP_OFF44[3]	VP_OFF44[2]	VP_OFF44[1]	VP_OFF44[0]	99h		
			20											
		R/W	21	VN_OFF52[3]	VN_OFF52[2]	VN_OFF52[1]	VN_OFF52[0]	VP_OFF52[3]	VP_OFF52[2]	VP_OFF52[1]	VP_OFF52[0]	76h		
			22	0	0	0	0	0	0	0	0	0		
		R/W	23	VN_OFF56[3]	VN_OFF56[2]	VN_OFF56[1]	VN_OFF56[0]	VP_OFF56[3]	VP_OFF56[2]	VP_OFF56[1]	VP_OFF56[0]	87h		
			24											
		R/W	25	VN_OFF58[3]	VN_OFF58[2]	VN_OFF58[1]	VN_OFF58[0]	VP_OFF58[3]	VP_OFF58[2]	VP_OFF58[1]	VP_OFF58[0]	45h		
			26	0	0	0	0	0	0	0	0	0		
R/W	27	VN_OFF60[3]	VN_OFF60[2]	VN_OFF60[1]	VN_OFF60[0]	VP_OFF60[3]	VP_OFF60[2]	VP_OFF60[1]	VP_OFF60[0]	43h				
	28													
R/W	29	VN_OFF61[3]	VN_OFF61[2]	VN_OFF61[1]	VN_OFF61[0]	VP_OFF61[3]	VP_OFF61[2]	VP_OFF61[1]	VP_OFF61[0]	33h				
	30	0	0	0	0	0	0	0	0	0				
R/W	31	VN_OFF62[3]	VN_OFF62[2]	VN_OFF62[1]	VN_OFF62[0]	VP_OFF62[3]	VP_OFF62[2]	VP_OFF62[1]	VP_OFF62[0]	32h				
	32	0	0	0	0	0	0	0	0	0				
PAGE_CTRL Into CMD2 PAGE0	00h	W	1	1	1	0	1	1	1	1	0	DEh		
PAGE_CTRL Into CMD1	EFh	W	1	1	0	1	0	1	0	1	0	AAh		

3GAMMAR_CTRL_RED_P (E0h)

Address (MDDI I/F)			E080h ~ E0A3h				Access Attribute				R/W
Address (Other I/F)			E0h				Number of Parameter(s)				36
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E080h	Parameter 1	0	VP0[7:0]								01h
E081h	Parameter 2	0	0		0	0	0	0	0	0	0
E082h	Parameter 3	0	VP1[7:0]								19h
E083h	Parameter 4	0	0		0	0	0	0	0	0	0
E084h	Parameter 5	0	VP2[7:0]								25h
E085h	Parameter 6	0	0		0	0	0	0	0	0	0
E086h	Parameter 7	0	VP4[7:0]								3Eh
E087h	Parameter 8	0	0		0	0	0	0	0	0	0
E088h	Parameter 9	0	VP6[7:0]								4Ah
E089h	Parameter 10	0	0		0	0	0	0	0	0	0
E08Ah	Parameter 11	0	VP8[7:0]								55h
E08Bh	Parameter 12	0	0		0	0	0	0	0	0	0
E08Ch	Parameter 13	0	VP12[7:0]								66h
E08Dh	Parameter 14	0	0		0	0	0	0	0	0	0
E08Eh	Parameter 15	0	VP20[7:0]								7Ch
E08Fh	Parameter 16	0	0		0	0	0	0	0	0	0
E090h	Parameter 17	0	VP28[7:0]								8Dh
E091h	Parameter 18	0	0		0	0	0	0	0	0	0
E092h	Parameter 19	0	VP36[7:0]								9Eh
E093h	Parameter 20	0	0		0	0	0	0	0	0	0
E094h	Parameter 21	0	VP44[7:0]								ACh
E095h	Parameter 22	0	0		0	0	0	0	0	0	0
E096h	Parameter 23	0	VP52[7:0]								BFh
E097h	Parameter 24	0	0		0	0	0	0	0	0	0
E098h	Parameter 25	0	VP56[7:0]								CAh
E099h	Parameter 26	0	0		0	0	0	0	0	0	0
E09Ah	Parameter 27	0	VP58[7:0]								D3h
E09Bh	Parameter 28	0	0		0	0	0	0	0	0	0
E09Ch	Parameter 29	0	VP60[7:0]								DDh
E09Dh	Parameter 30	0	0		0	0	0	0	0	0	0
E09Eh	Parameter 31	0	VP61[7:0]								E2h
E09Fh	Parameter 32	0	0		0	0	0	0	0	0	0
E0A0h	Parameter 33	0	VP62[7:0]								E9h
E0A1h	Parameter 34	0	0		0	0	0	0	0	0	0
E0A2h	Parameter 35	0	VP63[7:0]								F3h
E0A3h	Parameter 36	0	0		0	0	0	0	0	0	0

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid contection during register accessing, please make sure that the CABC functions are disabled.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #000080; color: white;"> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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3GAMAR_CTRL_RED_N (E1h)

Address (MDDI I/F)		E180h ~ E1A3h					Access Attribute				R/W	
Address (Other I/F)		E1h					Number of Parameter(s)				36	
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value	
E180h	Parameter 1	0	VN0[7:0]									00h
E181h	Parameter 2	0	0	0	0	0	0	0	0	0	0	
E182h	Parameter 3	0	VN1[7:0]									19h
E183h	Parameter 4	0	0	0	0	0	0	0	0	0	0	
E184h	Parameter 5	0	VN2[7:0]									25h
E185h	Parameter 6	0	0	0	0	0	0	0	0	0	0	
E186h	Parameter 7	0	VN4[7:0]									3Eh
E187h	Parameter 8	0	0	0	0	0	0	0	0	0	0	
E188h	Parameter 9	0	VN6[7:0]									4Ah
E189h	Parameter 10	0	0	0	0	0	0	0	0	0	0	
E18Ah	Parameter 11	0	VN8[7:0]									55h
E18Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0	
E18Ch	Parameter 13	0	VN12[7:0]									66h
E18Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0	
E18Eh	Parameter 15	0	VN20[7:0]									7Ch
E18Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0	
E190h	Parameter 17	0	VN28[7:0]									8Dh
E191h	Parameter 18	0	0	0	0	0	0	0	0	0	0	
E192h	Parameter 19	0	VN36[7:0]									9Eh
E193h	Parameter 20	0	0	0	0	0	0	0	0	0	0	
E194h	Parameter 21	0	VN44[7:0]									ACh
E195h	Parameter 22	0	0	0	0	0	0	0	0	0	0	
E196h	Parameter 23	0	VN52[7:0]									BFh
E197h	Parameter 24	0	0	0	0	0	0	0	0	0	0	
E198h	Parameter 25	0	VN56[7:0]									CAh
E199h	Parameter 26	0	0	0	0	0	0	0	0	0	0	
E19Ah	Parameter 27	0	VN58[7:0]									D4h
E19Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0	
E19Ch	Parameter 29	0	VN60[7:0]									DCh
E19Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0	
E19Eh	Parameter 31	0	VN61[7:0]									E2h
E19Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0	
E1A0h	Parameter 33	0	VN62[7:0]									E8h
E1A1h	Parameter 34	0	0	0	0	0	0	0	0	0	0	
E1A2h	Parameter 35	0	VN63[7:0]									F3h
E1A3h	Parameter 36	0	0	0	0	0	0	0	0	0	0	

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid contection during register accessing, please make sure that the CABC functions are disabled.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #000080; color: white;"> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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NO DISCLOSURE

3GAMMAR_CTRL_GREEN_P (E2h)

Address (MDDI I/F)		E280h ~ E2A3h					Access Attribute				R/W
Address (Other I/F)		E2h					Number of Parameter(s)				36
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E280h	Parameter 1	0	VP0[7:0]								01h
E281h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E282h	Parameter 3	0	VP1[7:0]								19h
E283h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E284h	Parameter 5	0	VP2[7:0]								25h
E285h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E286h	Parameter 7	0	VP4[7:0]								3Eh
E287h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E288h	Parameter 9	0	VP6[7:0]								4Ah
E289h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E28Ah	Parameter 11	0	VP8[7:0]								55h
E28Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E28Ch	Parameter 13	0	VP12[7:0]								66h
E28Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E28Eh	Parameter 15	0	VP20[7:0]								7Ch
E28Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E290h	Parameter 17	0	VP28[7:0]								8Dh
E291h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E292h	Parameter 19	0	VP36[7:0]								9Eh
E293h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E294h	Parameter 21	0	VP44[7:0]								ACh
E295h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E296h	Parameter 23	0	VP52[7:0]								BFh
E297h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E298h	Parameter 25	0	VP56[7:0]								CAh
E299h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E29Ah	Parameter 27	0	VP58[7:0]								D3h
E29Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E29Ch	Parameter 29	0	VP60[7:0]								DDh
E29Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E29Eh	Parameter 31	0	VP61[7:0]								E2h
E29Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0
E2A0h	Parameter 33	0	VP62[7:0]								E9h
E2A1h	Parameter 34	0	0	0	0	0	0	0	0	0	0
E2A2h	Parameter 35	0	VP63[7:0]								F3h
E2A3h	Parameter 36	0	0	0	0	0	0	0	0	0	0

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid conection during register accessing, please make sure that the CABC functions are disabled.												
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr style="background-color: #000080; color: white;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	N/A												

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NO DISCLOSURE

3GAMMAR_CTRL_GREEN_N (E3h)

Address (MDDI I/F)		E380h ~ E3A3h					Access Attribute				R/W
Address (Other I/F)		E3h					Number of Parameter(s)				36
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E380h	Parameter 1	0	VN0[7:0]								00h
E381h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E382h	Parameter 3	0	VN1[7:0]								19h
E383h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E384h	Parameter 5	0	VN2[7:0]								25h
E385h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E386h	Parameter 7	0	VN4[7:0]								3Eh
E387h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E388h	Parameter 9	0	VN6[7:0]								4Ah
E389h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E38Ah	Parameter 11	0	VN8[7:0]								55h
E38Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E38Ch	Parameter 13	0	VN12[7:0]								66h
E38Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E38Eh	Parameter 15	0	VN20[7:0]								7Ch
E38Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E390h	Parameter 17	0	VN28[7:0]								8Dh
E391h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E392h	Parameter 19	0	VN36[7:0]								9Eh
E393h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E394h	Parameter 21	0	VN44[7:0]								ACH
E395h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E396h	Parameter 23	0	VN52[7:0]								BFh
E397h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E398h	Parameter 25	0	VN56[7:0]								CAh
E399h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E39Ah	Parameter 27	0	VN58[7:0]								D4h
E39Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E39Ch	Parameter 29	0	VN60[7:0]								DCh
E39Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E39Eh	Parameter 31	0	VN61[7:0]								E2h
E39Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0
E3A0h	Parameter 33	0	VN62[7:0]								E8h
E3A1h	Parameter 34	0	0	0	0	0	0	0	0	0	0
E3A2h	Parameter 35	0	VN63[7:0]								F3h
E3A3h	Parameter 36	0	0	0	0	0	0	0	0	0	0

Description	These registers are used for gamma correction.													
Restriction	To avoid contection during register accessing, please make sure that the CABC functions are disabled.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default Value														

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3GAMMAR_CTRL_BLUE_P (E4h)

Address (MDDI I/F)		E480h ~ E4A3h					Access Attribute				R/W
Address (Other I/F)		E4h					Number of Parameter(s)				36
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E480h	Parameter 1	0	VP0[7:0]								01h
E481h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E482h	Parameter 3	0	VP1[7:0]								19h
E483h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E484h	Parameter 5	0	VP2[7:0]								25h
E485h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E486h	Parameter 7	0	VP4[7:0]								3Eh
E487h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E488h	Parameter 9	0	VP6[7:0]								4Ah
E489h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E48Ah	Parameter 11	0	VP8[7:0]								55h
E48Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E48Ch	Parameter 13	0	VP12[7:0]								66h
E48Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E48Eh	Parameter 15	0	VP20[7:0]								7Ch
E48Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E490h	Parameter 17	0	VP28[7:0]								8Dh
E491h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E492h	Parameter 19	0	VP36[7:0]								9Eh
E493h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E494h	Parameter 21	0	VP44[7:0]								ACH
E495h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E496h	Parameter 23	0	VP52[7:0]								BFh
E497h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E498h	Parameter 25	0	VP56[7:0]								CAh
E499h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E49Ah	Parameter 27	0	VP58[7:0]								D4h
E49Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E49Ch	Parameter 29	0	VP60[7:0]								DCh
E49Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E49Eh	Parameter 31	0	VP61[7:0]								E2h
E49Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0
E4A0h	Parameter 33	0	VP62[7:0]								E8h
E4A1h	Parameter 34	0	0	0	0	0	0	0	0	0	0
E4A2h	Parameter 35	0	VP63[7:0]								F3h
E4A3h	Parameter 36	0	0	0	0	0	0	0	0	0	0

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid conection during register accessing, please make sure that the CABG functions are disabled.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #000080; color: white;"> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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3GAMMAR_CTRL_BLUE_N (E5h)

Address (MDDI I/F)		E580h ~ E5A3h					Access Attribute				R/W
Address (Other I/F)		E5h					Number of Parameter(s)				36
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E580h	Parameter 1	0	VN0[7:0]								00h
E581h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E582h	Parameter 3	0	VN1[7:0]								19h
E583h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E584h	Parameter 5	0	VN2[7:0]								25h
E585h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E586h	Parameter 7	0	VN4[7:0]								3Eh
E587h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E588h	Parameter 9	0	VN6[7:0]								4Ah
E589h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E58Ah	Parameter 11	0	VN8[7:0]								55h
E58Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E58Ch	Parameter 13	0	VN12[7:0]								66h
E58Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E58Eh	Parameter 15	0	VN20[7:0]								7Ch
E58Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E590h	Parameter 17	0	VN28[7:0]								8Dh
E591h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E592h	Parameter 19	0	VN36[7:0]								9Eh
E593h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E594h	Parameter 21	0	VN44[7:0]								ACh
E595h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E596h	Parameter 23	0	VN52[7:0]								BFh
E597h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E598h	Parameter 25	0	VN56[7:0]								CAh
E599h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E59Ah	Parameter 27	0	VN58[7:0]								D4h
E59Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E59Ch	Parameter 29	0	VN60[7:0]								DCh
E59Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E59Eh	Parameter 31	0	VN61[7:0]								E2h
E59Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0
E5A0h	Parameter 33	0	VN62[7:0]								E8h
E5A1h	Parameter 34	0	0	0	0	0	0	0	0	0	0
E5A2h	Parameter 35	0	VN63[7:0]								F3h
E5A3h	Parameter 36	0	0	0	0	0	0	0	0	0	0

Description	These registers are used for gamma correction.												
Restriction	To avoid conection during register accessing, please make sure that the CABG functions are disabled.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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CABC GAMMA offset (E6h)

Address (MDDI I/F)		E680h ~ E6A3h					Access Attribute				R/W
Address (Other I/F)		E6h					Number of Parameter(s)				32
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E680h	Parameter 1	0	VN_OFF1[3:0]				VP_OFF1[3:0]				22h
E681h	Parameter 2	0	0	0		0	0	0	0	0	0
E682h	Parameter 3	0	VN_OFF2[3:0]				VP_OFF2[3:0]				44h
E683h	Parameter 4	0	0	0		0	0	0	0	0	0
E684h	Parameter 5	0	VN_OFF4[3:0]				VP_OFF4[3:0]				44h
E685h	Parameter 6	0	0	0		0	0	0	0	0	0
E686h	Parameter 7	0	VN_OFF6[3:0]				VP_OFF6[3:0]				66h
E687h	Parameter 8	0	0	0		0	0	0	0	0	0
E688h	Parameter 9	0	VN_OFF8[3:0]				VP_OFF8[3:0]				66h
E689h	Parameter 10	0	0	0		0	0	0	0	0	0
E68Ah	Parameter 11	0	VN_OFF12[3:0]				VP_OFF12[3:0]				77h
E68Bh	Parameter 12	0	0	0		0	0	0	0	0	0
E68Ch	Parameter 13	0	VN_OFF20[3:0]				VP_OFF20[3:0]				77h
E68Dh	Parameter 14	0	0	0		0	0	0	0	0	0
E68Eh	Parameter 15	0	VN_OFF28[3:0]				VP_OFF28[3:0]				AAh
E68Fh	Parameter 16	0	0	0		0	0	0	0	0	0
E690h	Parameter 17	0	VN_OFF36[3:0]				VP_OF36[3:0]				BBh
E691h	Parameter 18	0	0	0		0	0	0	0	0	0
E692h	Parameter 19	0	VN_OFF44[3:0]				VP_OFF44[3:0]				99h
E693h	Parameter 20	0	0	0		0	0	0	0	0	0
E694h	Parameter 21	0	VN_OFF52[3:0]				VP_OFF52[3:0]				76h
E695h	Parameter 22	0	0	0		0	0	0	0	0	0
E696h	Parameter 23	0	VN_OFF56[3:0]				VP_OFF56[3:0]				87h
E697h	Parameter 24	0	0	0		0	0	0	0	0	0
E698h	Parameter 25	0	VN_OFF58[3:0]				VP_OFF58[3:0]				45h
E699h	Parameter 26	0	0	0		0	0	0	0	0	0
E69Ah	Parameter 27	0	VN_OFF60:0]				VP_OFF60[3:0]				43h
E69Bh	Parameter 28	0	0	0		0	0	0	0	0	0
E69Ch	Parameter 29	0	VN_OFF61[3:0]				VP_OFF61[3:0]				33h
E69Dh	Parameter 30	0	0	0		0	0	0	0	0	0
E69Eh	Parameter 31	0	VN_OFF62[3:0]				VP_OFF62[3:0]				32h
E69Fh	Parameter 32	0	0	0		0	0	0	0	0	0

Description	These registers are used for gamma correction. ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time.
	Restriction

Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default Value				

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CABC GAMMA offset (E7h)

Address (MDDI I/F)		E780h ~ E7A3h					Access Attribute				R/W
Address (Other I/F)		E7h					Number of Parameter(s)				32
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E780h	Parameter 1	0	VN_OFF1[3:0]				VP_OFF1[3:0]				22h
E781h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E782h	Parameter 3	0	VN_OFF2[3:0]				VP_OFF2[3:0]				44h
E783h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E784h	Parameter 5	0	VN_OFF4[3:0]				VP_OFF4[3:0]				44h
E785h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E786h	Parameter 7	0	VN_OFF6[3:0]				VP_OFF6[3:0]				66h
E787h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E788h	Parameter 9	0	VN_OFF8[3:0]				VP_OFF8[3:0]				66h
E789h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E78Ah	Parameter 11	0	VN_OFF12[3:0]				VP_OFF12[3:0]				77h
E78Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E78Ch	Parameter 13	0	VN_OFF20[3:0]				VP_OFF20[3:0]				77h
E78Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E78Eh	Parameter 15	0	VN_OFF28[3:0]				VP_OFF28[3:0]				AAh
E78Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E790h	Parameter 17	0	VN_OFF36[3:0]				VP_OF36[3:0]				BBh
E791h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E792h	Parameter 19	0	VN_OFF44[3:0]				VP_OFF44[3:0]				99h
E793h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E794h	Parameter 21	0	VN_OFF52[3:0]				VP_OFF52[3:0]				76h
E795h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E796h	Parameter 23	0	VN_OFF56[3:0]				VP_OFF56[3:0]				87h
E797h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E798h	Parameter 25	0	VN_OFF58[3:0]				VP_OFF58[3:0]				45h
E799h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E79Ah	Parameter 27	0	VN_OFF60[3:0]				VP_OFF60[3:0]				43h
E79Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E79Ch	Parameter 29	0	VN_OFF61[3:0]				VP_OFF61[3:0]				33h
E79Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E79Eh	Parameter 31	0	VN_OFF62[3:0]				VP_OFF62[3:0]				32h
E79Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid conection during register accessing, please make sure that the CABc functions are disabled.												
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr style="background-color: #000080; color: white;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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CABC GAMMA offset (E8h)

Address (MDDI I/F)		E880h ~ E8A3h					Access Attribute				R/W
Address (Other I/F)		E8h					Number of Parameter(s)				32
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
E880h	Parameter 1	0	VN_OFF1[3:0]				VP_OFF1[3:0]				22h
E881h	Parameter 2	0	0	0	0	0	0	0	0	0	0
E882h	Parameter 3	0	VN_OFF2[3:0]				VP_OFF2[3:0]				44h
E883h	Parameter 4	0	0	0	0	0	0	0	0	0	0
E884h	Parameter 5	0	VN_OFF4[3:0]				VP_OFF4[3:0]				44h
E885h	Parameter 6	0	0	0	0	0	0	0	0	0	0
E886h	Parameter 7	0	VN_OFF6[3:0]				VP_OFF6[3:0]				66h
E887h	Parameter 8	0	0	0	0	0	0	0	0	0	0
E888h	Parameter 9	0	VN_OFF8[3:0]				VP_OFF8[3:0]				66h
E889h	Parameter 10	0	0	0	0	0	0	0	0	0	0
E88Ah	Parameter 11	0	VN_OFF12[3:0]				VP_OFF12[3:0]				77h
E88Bh	Parameter 12	0	0	0	0	0	0	0	0	0	0
E88Ch	Parameter 13	0	VN_OFF20[3:0]				VP_OFF20[3:0]				77h
E88Dh	Parameter 14	0	0	0	0	0	0	0	0	0	0
E88Eh	Parameter 15	0	VN_OFF28[3:0]				VP_OFF28[3:0]				AAh
E88Fh	Parameter 16	0	0	0	0	0	0	0	0	0	0
E890h	Parameter 17	0	VN_OFF36[3:0]				VP_OF36[3:0]				BBh
E891h	Parameter 18	0	0	0	0	0	0	0	0	0	0
E892h	Parameter 19	0	VN_OFF44[3:0]				VP_OFF44[3:0]				99h
E893h	Parameter 20	0	0	0	0	0	0	0	0	0	0
E894h	Parameter 21	0	VN_OFF52[3:0]				VP_OFF52[3:0]				76h
E895h	Parameter 22	0	0	0	0	0	0	0	0	0	0
E896h	Parameter 23	0	VN_OFF56[3:0]				VP_OFF56[3:0]				87h
E897h	Parameter 24	0	0	0	0	0	0	0	0	0	0
E898h	Parameter 25	0	VN_OFF58[3:0]				VP_OFF58[3:0]				45h
E899h	Parameter 26	0	0	0	0	0	0	0	0	0	0
E89Ah	Parameter 27	0	VN_OFF60[3:0]				VP_OFF60[3:0]				43h
E89Bh	Parameter 28	0	0	0	0	0	0	0	0	0	0
E89Ch	Parameter 29	0	VN_OFF61[3:0]				VP_OFF61[3:0]				33h
E89Dh	Parameter 30	0	0	0	0	0	0	0	0	0	0
E89Eh	Parameter 31	0	VN_OFF62[3:0]				VP_OFF62[3:0]				32h
E89Fh	Parameter 32	0	0	0	0	0	0	0	0	0	0

Description	<p>These registers are used for gamma correction.</p> <ul style="list-style-type: none"> ※ Note1: Please access this command in command2_P1. ※ Note2: This command only can be read on display off. ※ Note3: Please access all gamma table at 1 time. 												
Restriction	To avoid conection during register accessing, please make sure that the CABC functions are disabled.												
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr style="background-color: #000080; color: white;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value													

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PAGE_LOCK (00h) : Set the Register to command2 Page 0

Address (MDDI I/F)		0080h					Access Attribute				W
Address (Other I/F)		00h					Number of Parameter(s)				1
Address (MDDI I/F)	Parameter (Other I/F)	D[15 : 8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Default Value
0080h	Parameter 1	0	1	0	1	0	1	0	1	0	AAh

Description	This command is used for goto CMD2_P0 register access.												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default Value	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value D[15 : 0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>-</td> </tr> <tr> <td>S/W Reset</td> <td>-</td> </tr> <tr> <td>H/W Reset</td> <td>-</td> </tr> </tbody> </table>	Status	Default Value D[15 : 0]	Power On Sequence	-	S/W Reset	-	H/W Reset	-				
Status	Default Value D[15 : 0]												
Power On Sequence	-												
S/W Reset	-												
H/W Reset	-												

7. Electrical Characteristics
7.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	VDDI	-0.3~+5.5	V
Supply voltage	VCI-AVSS	-0.3~+5.5	V
Driver supply Voltage	AVDD-AVSS	-0.3 ~ +6.5	V
Operating temperature range	TOPR	-30 ~ +75	°C
Storage Temperature range	TSTG	-30 ~ +85	°C
Logic Input voltage range	V _{IN}	-0.3~+3.6	V
Logic Output voltage range	V _O	-0.3~+3.6	V
Supply voltage (MTP)	MTP_PWR - AVSS	-0.3~7.8	V
Max Voltage of VGH-VGL	VGH-VGL	< 32	V
Differential Input Voltage	DSI-CLK+, DSI-CLK+ DSI-D0+,DSI-D0-	-0.3~+1.8	V
Humidity		5% to 95%	%

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2 DC CHARACTERISTICS
7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage MDDI/MIPI Operating voltage Digital Operating voltage	VCI	Operating Voltage MDDI/MIPI Supply voltage	2.3	2.8	3.3	V	Note 1, 10
I/O operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V	Note 1, 10
Input / Output							
Logic High level input voltage	VIH		0.7*VDDI	-	VDDI	V	Note 2, 3, 4
Logic Low level input voltage	VIL	-	VSS	-	0.3*VDDI	V	Note 2, 3, 4
Logic High level output voltage	VOH	IOH = -1mA	0.8VDDI	-	VDDI	V	Note 2, 3, 4
Logic Low level output voltage	VOL	IOL = +1mA	VSS	-	0.2VDDI	V	Note 2, 3, 4
Logic High level leakage (Except MDDI / MIPI)	ILIH1	Vin = 0 to VDDI			1	μA	Note 2, 3, 4
Logic Low level leakage (Except MDDI / MIPI)	ILIL1	Vin = 0 to VDDI	-1			μA	Note 2, 3, 4
Logic High level leakage (MDDI / MIPI)	ILIH2 (MDDI)	Vin = 0 to VDDI			10	μA	Note 2,10
	ILIH2 (MIPI)	Vin = 0 to VDDI					
Logic Low level leakage (MDDI / MIPI)	ILIL2 (MDDI)	Vin = 0 to 1.3V	-10			μA	Note 2,10
	ILIL2 (MIPI)	Vin = 0 to 1.3V					
VCOM Operation							
VCOM voltage	VCOM	Operating Voltage	-3	-	0	V	
Source Driver							
Gamma reference voltage	GVDDP	GVMP <AVDDP1-0.3	3.0	-	5.5	V	Note 8
	GVDDN	GVMN >AVEE+0.3	-5.5	-	-3.0	V	Note 8
Output deviation voltage (Source Positive output)	V,dev1	Sout >= +4.2V, Sout <= +0.8V	-	-	35	mV	Note 5
	V,dev2	+0.8V < Sout < +4.2V	-	-	25	mV	
Output deviation voltage (Source Negative output)	V,dev3	Sout >= -0.8V, Sout <= -4.2V	-	-	35	mV	
	V,dev4	-4.2V < Sout < -0.8V	-	-	25	mV	
Output offset voltage	VOFSET				35	mv	Note 8
Booster Operation							
Internal reference voltage	VREF	Operating Voltage	-1	-	1	%	Note 3
1 st Booster voltage	AVDD	Operating Voltage	4.7	-	6.0	V	Note 9
2 nd Booster voltage	VGH	Operating Voltage	2xAVDD	-	3xAVDD	V	Note 6
3 rd Booster voltage	VGL	Operating Voltage	-3xAVDD	-	VCI-2AVDD	V	Note 6
4 th Booster voltage	VCL	Operating Voltage	-VCI	-	-	V	Note 6
5 th Booster voltage	AVEE	Operating Voltage	-AVDD		-	V	Note 9
Oscillator tolerance	OSC	25°C	-5	-	5	%	
Oscillator tolerance	OSC	-30°C ~75°C	-8	-	8	%	

Note 1: VDDI=1.65 to 3.3V, VCI=2.3 to 3.3 V, AVSS=VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

Note 2, 3, 4: When the measurements are performed with LCD module, Measurement Points are like below.
CSX, RDX, WRX, D[17:0], DCX, RESX, SCL, IM[3:0] and Test pins

Note 5: Source channel loading= 40pF/channel

Note 6: VCI=2.85V, Ta=25 °C, No load on the panel, Iload1 = -1[mA]; |Output voltage -Target voltage| < 100mv;

Note 7,8: VCI=2.85V, Ta=25 °C, No load on the panel, |Output voltage -Target voltage| < 25mv;

Note 9: VCI=2.85V, Ta=-25 °C, Charge pump Load current = 6mA, Charge pump frequency = TBD hz, power pad serial resistor is smaller than maximum value, Default value=5.8V

Note 10: VCI=2.3V to 3.3 V, VDDI=1.65 to 3.3V, AVSS=VSS=0V, Ta=-30 to 70 °C (to +85 °C no damage)

7.2.2 Current Consumption

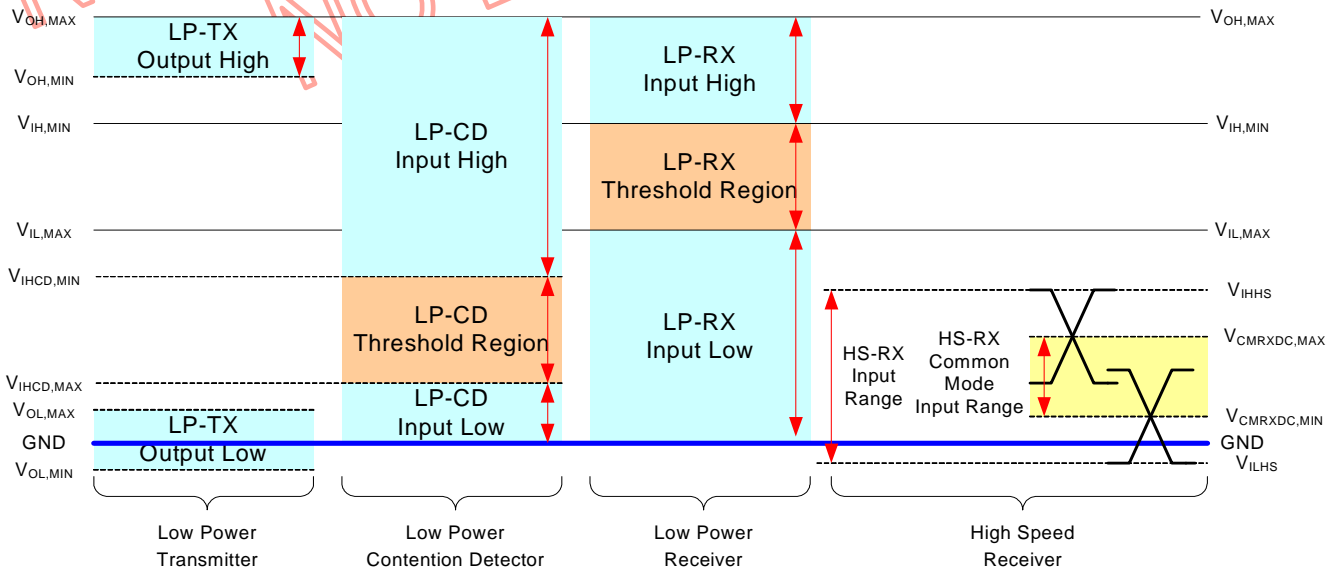
16.7Mcolors, HVGA, Normally Black, Ta=25°C, VDDI=1.8V, VCI=2.8V, MCU interface, No Access				
Mode Of Operation	Inversion	Image	Power Consumption	
			IDD(uA)	ICI(mA)
Normal Mode on Partial Mode off Idle Mode off Sleep out mode	Dot inversion 60Hz	White	TBD	TBD
		Black	TBD	TBD
		Check 4x4	TBD	TBD
		Gray Scale(Top to Bottom)	TBD	TBD
		Worst case Pattern	TBD	TBD
Normal Mode off Partial Mode off Idle Mode on Sleep out mode	Dot inversion 60Hz	White	TBD	TBD
		Black	TBD	TBD
		Check 4x4	TBD	TBD
		Gray Scale(Top to Bottom)	TBD	TBD
		Worst case Pattern	TBD	TBD
Sleep in mode	RAM Power Keep	Worst case Pattern	0.01	0.03
Sleep in mode	RAM Power Off	-	0.01	0.01

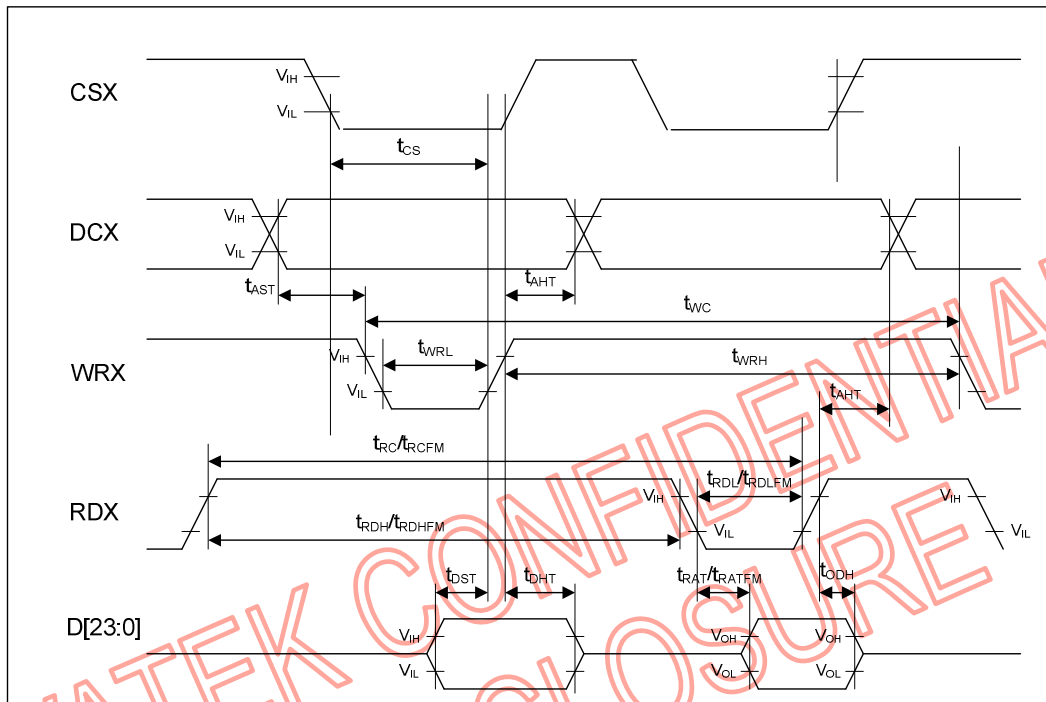
7.2.3 MDDI DC Characteristics

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Differential input "High" level voltage (VT=125mV) (MDDI_DATA_P/M)	VIT+off		—	125	175	mV
Differential input "Low" level voltage (VT=125mV) (MDDI_DATA_P/M)	VIT-off		75	125	—	mV
Differential input "High" level voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	VIT+		—	0	50	mV
Differential input "Low" level voltage (VT=0) (MDDI_DATA_P/M, MDDI_STB_P/M)	VIT+		-50	0	—	mV
Terminator impedance for MDDI interface	Zt		80	100	125	ohm

7.2.4 MIPI DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VCI	Power supply voltage for MIPI RX	2.3	2.8	3.3	V
VLPH	Low power mode operating voltage	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40			mV
VIHHS	Single-ended input high voltage			460	mV
VCMRXDC	Common-mode voltage	70		330	mV
ZID	Differential input impedance	80	100	125	ohm
V _{OD}	HS transmit differential voltage (V _{OD} =V _{DP} -V _{DN})	140	200	250	mV
V _{IDTH}	Differential input high threshold			70	mV
V _{IDTL}	Differential input low threshold	-70			mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50		1350	mV
V _{GND} SH	Ground shift	-50		50	mV
VIL	Logic 0 input threshold	0.0		550	mV
VIH	Logic 1 input threshold	880		1350	mV
V _{ILLPRXULP}	LP-RX(CLK ULP mode)	0.0		300	mV
V _{HYST}	Input hysteresis	25			mV
VOL	Output low level	-50		50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
V _{IHCD,MAX}	Logic 0 contention threshold	0.0		200	mV
V _{ILCD,MIN}	Logic 1 contention threshold	450		1350	mV
I _{IH}	LP-CD,LP-RX			10	uA
I _{IL}	LP-CD,LP-RX	-10			uA
Other					
V _{TERM-EN}	Single-Ended Thershold Voltage for Termination Enable			450	mV
C _{TERM}	Termination Capacitor			60	pF



7.3 AC CHARACTERISTICS
7.3.1 80-System Bus Interface Timing Characteristics (16-/8-bits Transfer Mode)

Figure 7.3.1 80-System Bus Interface Operation
Table 7.3.1 VCI=2.3 V to 3.3, VDDI = 1.65 V to 3.3 V (Register Access)

Item	Symbol	Timing Diagram	Min	Typ	Max	Unit
Write cycle time	t_{WC}	Figure 7.3.1	40	-	-	ns
Read cycle time	t_{RC}	Figure 7.3.1	160	-	-	ns
Write control pulse "Low" duration	t_{WRL}	Figure 7.3.1	19	-	-	ns
Read control pulse "Low" duration	t_{RDL}	Figure 7.3.1	45	-	-	ns
Write control pulse "High" duration	t_{WRH}	Figure 7.3.1	19	-	-	ns
Read control pulse "High" duration	t_{RDH}	Figure 7.3.1	90	-	-	ns
Write setup time (DCX to CSX, WRX)	t_{AST}	Figure 7.3.1	0	-	-	ns
Read setup time (DCX to CSX, RDX)	t_{AST}	Figure 7.3.1	10	-	-	ns
Address hold time	t_{AHT}	Figure 7.3.1	2	-	-	ns
Write data setup time	t_{DST}	Figure 7.3.1	15	-	-	ns
Write data hold time	t_{DHT}	Figure 7.3.1	10	-	-	ns
Read data access time	t_{RAT}	Figure 7.3.1	-	-	40	ns
Read data hold time	t_{ODH}	Figure 7.3.1	5	-	-	ns
Chip select setup time	t_{CS}	Figure 7.3.1	15	-	-	ns

7.3.2 80-System Bus Interface Timing Characteristics (1 transfer per pixel)

VCI=2.3 V to 3.3, VDDI = 1.65 V to 3.3 V (RAM Data Access)

Item	Symbol	Timing Diagram	Min.	Typ.	Max.	Unit
Write cycle time	tWC	Figure 7.3.1	40	-	-	ns
Read cycle time	tRCFM	Figure 7.3.1	400	-	-	ns
Write low-level pulse width	tWRL	Figure 7.3.1	19	-	-	ns
Read low-level pulse width	tRDLFM	Figure 7.3.1	150	-	-	ns
Write high-level pulse width	tWRH	Figure 7.3.1	19	-	-	ns
Read high-level pulse width	tRDHFM	Figure 7.3.1	250	-	-	ns
Write setup time (DCX to CSX, WRX)	tAST	Figure 7.3.1	0	-	-	ns
Read setup time (DCX to CSX, RDX)	tAST	Figure 7.3.1	10	-	-	ns
Address hold time	tAHT	Figure 7.3.1	2	-	-	ns
Write data setup time	tDST	Figure 7.3.1	10	-	-	ns
Write data hold time	tDHT	Figure 7.3.1	10	-	-	ns
Read data delay time	tRATFM	Figure 7.3.1	-	-	150	ns
Read data hold time	tODH	Figure 7.3.1	5	-	-	ns
Chip select setup time	tCS	Figure 7.3.1	15	-	-	ns

7.3.3 80-System Bus Interface Timing Characteristics (2 or 3 transfer per pixel)

VCI=2.3 V to 3.3, VDDI = 1.65 V to 3.3 V (RAM Data Access)

Item	Symbol	Timing Diagram	Min.	Typ.	Max.	Unit
Write cycle time	tWC	Figure 7.3.1	25	-	-	ns
Read cycle time	tRCFM	Figure 7.3.1	400	-	-	ns
Write low-level pulse width	tWRL	Figure 7.3.1	-	-	-	ns
Read low-level pulse width	tRDLFM	Figure 7.3.1	150	-	-	ns
Write high-level pulse width	tWRH	Figure 7.3.1	-	-	-	ns
Read high-level pulse width	tRDHFM	Figure 7.3.1	250	-	-	ns
Write setup time (DCX to CSX, WRX)	tAST	Figure 7.3.1	0	-	-	ns
Read setup time (DCX to CSX, RDX)	tAST	Figure 7.3.1	10	-	-	ns
Address hold time	tAHT	Figure 7.3.1	2	-	-	ns
Write data setup time	tDST	Figure 7.3.1	10	-	-	ns
Write data hold time	tDHT	Figure 7.3.1	10	-	-	ns
Read data delay time	tRATFM	Figure 7.3.1	-	-	150	ns
Read data hold time	tODH	Figure 7.3.1	5	-	-	ns
Chip select setup time	tCS	Figure 7.3.1	15	-	-	ns

VCI=2.3 V to 3.3, VDDI = 1.65 V to 3.3 V (RAM Data Access)

Item	Symbol	Timing Diagram	Min.	Typ.	Max.	Unit
Write cycle time	tWC	Figure 7.3.1	40	-	-	ns
Read cycle time	tRCFM	Figure 7.3.1	400	-	-	ns
Write low-level pulse width	tWRL	Figure 7.3.1	19	-	-	ns
Read low-level pulse width	tRDLFM	Figure 7.3.1	150	-	-	ns
Write high-level pulse width	tWRH	Figure 7.3.1	19	-	-	ns
Read high-level pulse width	tRDHFM	Figure 7.3.1	250	-	-	ns
Write setup time (DCX to CSX, WRX)	tAST	Figure 7.3.1	0	-	-	ns
Read setup time (DCX to CSX, RDX)	tAST	Figure 7.3.1	10	-	-	ns
Address hold time	tAHT	Figure 7.3.1	2	-	-	ns
Write data setup time	tDST	Figure 7.3.1	10	-	-	ns
Write data hold time	tDHT	Figure 7.3.1	10	-	-	ns
Read data delay time	tRATFM	Figure 7.3.1	-	-	150	ns
Read data hold time	tODH	Figure 7.3.1	5	-	-	ns
Chip select setup time	tCS	Figure 7.3.1	15	-	-	ns

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 NO DISCLOSURE

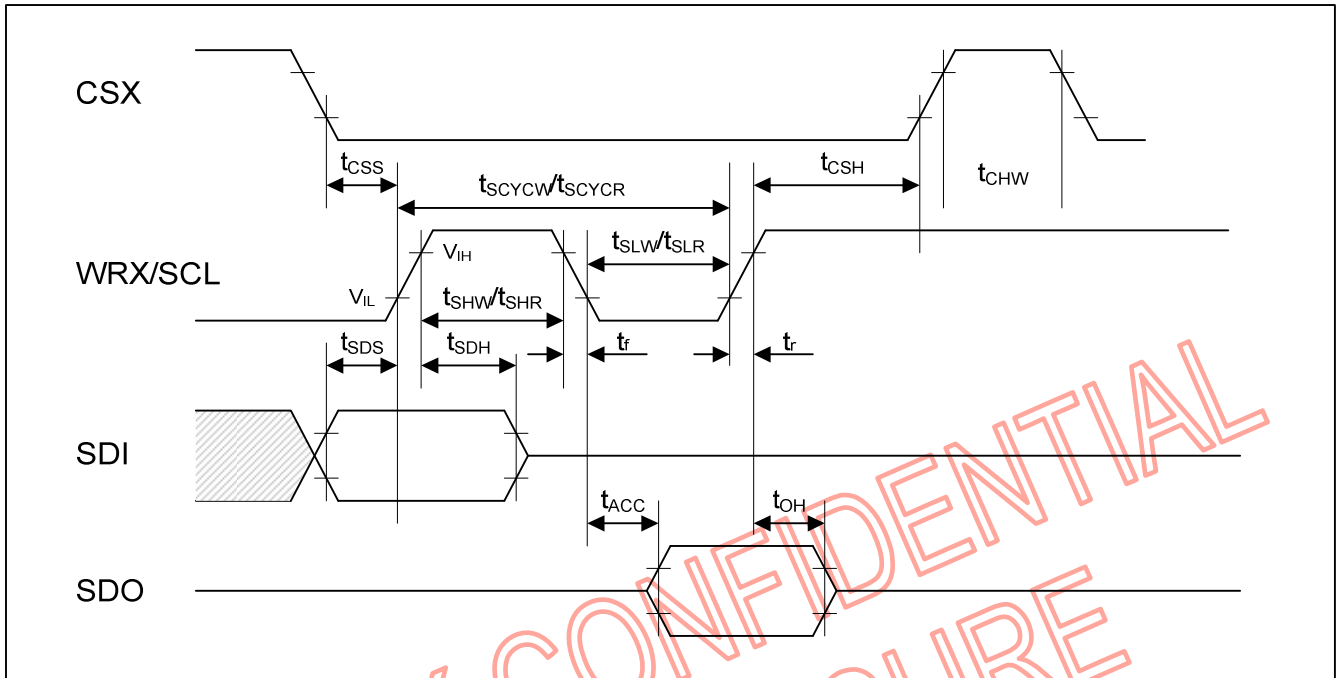
7.3.9 Serial Interface Timing Characteristics


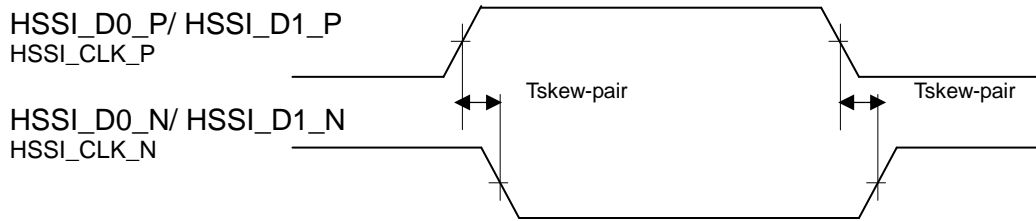
Figure 7.3.4 Serial Interface Operation

 Table 7.3.7 Normal Write Mode,
 $V_{CI}=2.3\text{ V to }3.3$, $V_{DDI}=1.65\text{ V to }3.3\text{ V}$

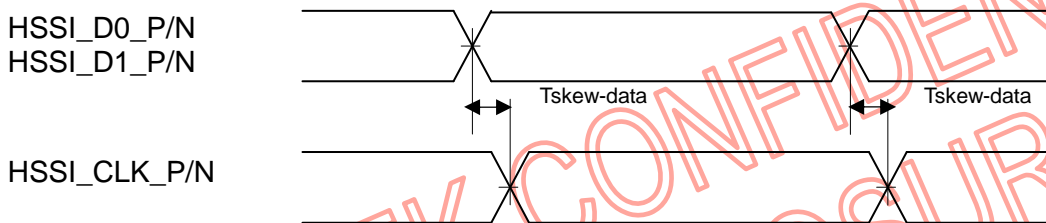
Item	Symbol	Timing Diagram	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	tSCYCW	Figure 7.3.4	100	-	20,000	ns
SCL clock cycle time Read (transmitted)	tSCYCR	Figure 7.3.4	300	-	20,000	ns
SCL "High" pulse width Write (received)	tSHW	Figure 7.3.4	40	-	-	ns
SCL "High" pulse width Read (transmitted)	tSHR	Figure 7.3.4	140	-	-	ns
SCL "Low" pulse width Write (received)	tSLW	Figure 7.3.4	40	-	-	ns
SCL "Low" pulse width Read (transmitted)	tSLR	Figure 7.3.4	140	-	-	ns
SCL clock rise/fall time	tr, tr	Figure 7.3.4	-	-	10	ns
Chip select setup time	tCSS	Figure 7.3.4	20	-	-	ns
Chip select hold time	tCSH	Figure 7.3.4	50	-	-	ns
Input data setup time	tSDS	Figure 7.3.4	20	-	-	ns
Input data hold time	tSDH	Figure 7.3.4	20	-	-	ns
Output data access time	tACC	Figure 7.3.4	-	-	120	ns
Output data hold time	tOH	Figure 7.3.4	5	-	-	ns
Chip deselect "High" pulse width	tCHW	Figure 7.3.4	45	-	-	ns

7.3.4 MDDI Interface Characteristics

MDDI: Skew between HSSI Signal Pair.



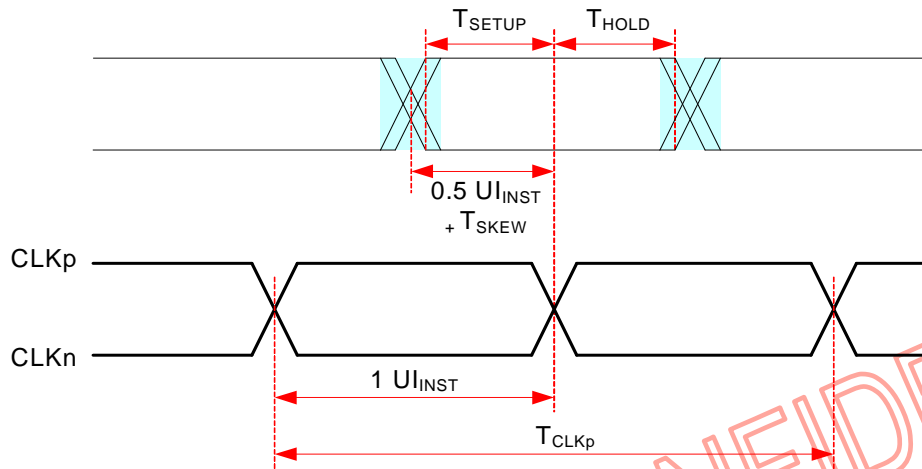
MDDI: Skew between HSSI_D0_P/N , HSSI_D1_P/N and HSSI_CLK_P/N signal


Fig. 7.3.8 MDDI Interface characteristics
VCI= 2.3V to 3.3, VDDI = 1.65 V to 3.3 V, Ta = -30 to 70°C

Symbol	Parameter	Timing diagram	Min	Typ	Max	Unit
1/tBIT	Data transfer rate	Figure 7.3.5	—	384	400	Mbps (Per lane)
Tskew-pair	Differential transfer input skew	Figure 7.3.5	—	—	0.25	ns
Tskew-data	Data_Stb input skew	Figure 7.3.5	—	—	0.3	ns

7.3.5 MIPI Interface Characteristics

High Speed Data transmission: Data-Clock Timing

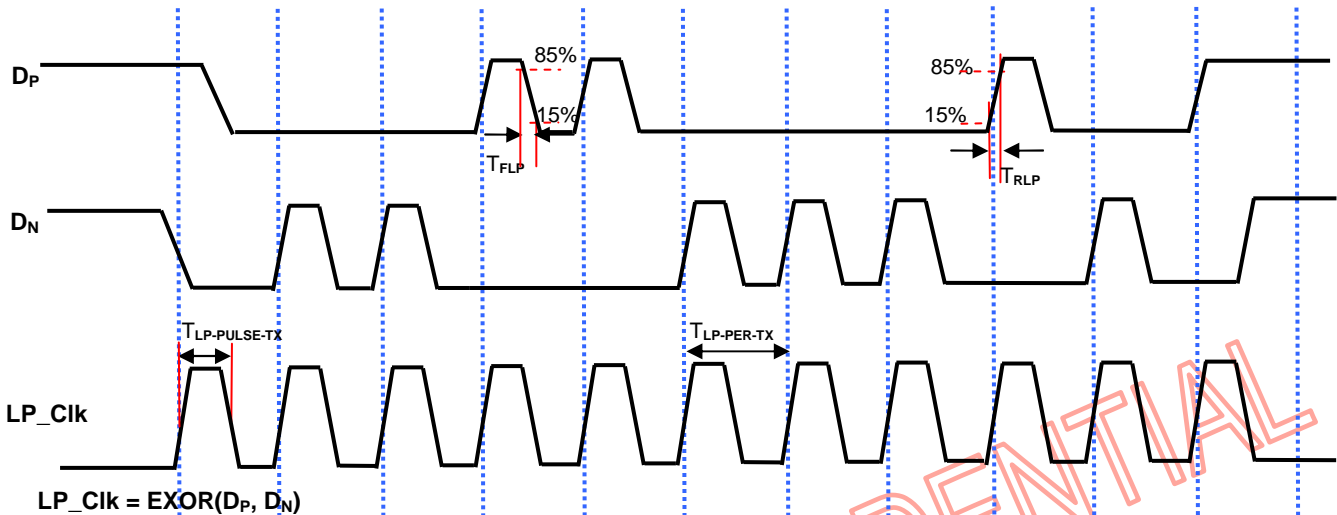


Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	TBD		12.5	ns	1,2
Data to Clock Skew [measured at transmitter]	$T_{SKEW(TX)}$	-0.15		0.15	UI_{INST}	3
Data to Clock Setup Time [measured at receiver]	$T_{SETUP(RX)}$	0.15			UI_{INST}	4
Data to Clock Hold Time [measured at receiver]	$T_{HOLD(RX)}$	0.15			UI_{INST}	4
20% - 80% rise time and fall time	t_R / t_F	150			ps	
				0.3	UI_{INST}	

Note:

1. This value corresponds to a minimum 80 MHz data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
3. Total silicon and package delay budget of $0.3 * UI_{INST}$.
4. Total setup and hold window for receiver of $0.3 * UI_{INST}$.

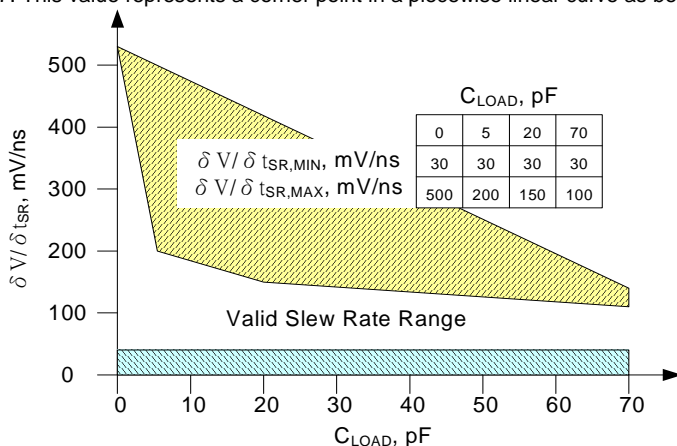
LP Transmission AC Specification



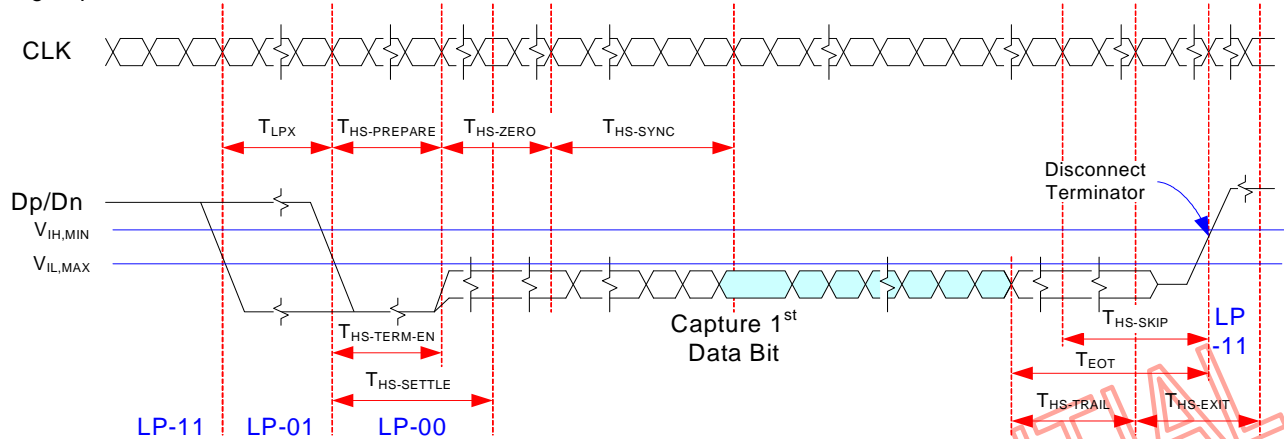
Parameter	Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time	T_{RLP} / T_{FLP}			25	ns	1
30%-85% rise time and fall time	T_{REOT}			35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	40			ns	4
	All other pulses	20			ns	4
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	90			ns	
Slew Rate@ $C_{LOAD} = 0pF$	$\delta V / \delta t_{SR}$	30		500	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 5pF$		30		200	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 20pF$		30		150	mV/ns	1,2,3,7
Slew Rate@ $C_{LOAD} = 70pF$		30		100	mV/ns	1,2,3,7
Load Capacitance	C_{LOAD}			70	pF	1

Note:

- C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
- When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
- Measured as average across any 50 mV segment of the output signal transition.
- This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between D_p and D_n LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.
- The rise-time of TREET starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
- With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.
- This value represents a corner point in a piecewise linear curve as bellowed.



High-Speed Data Transmission in Bursts

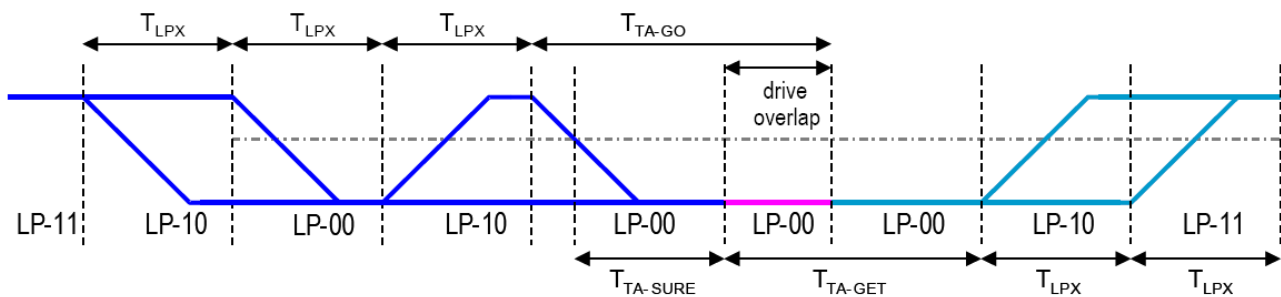


Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	$40+4UI$		$85+6UI$	ns
Time from start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ period to start of LP-11 state	T_{EOT}			$105+12UI$	ns
Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$			$35+4UI$	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	$60+4UI$			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		$55+4UI$	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	$105+6UI$			ns

Note:

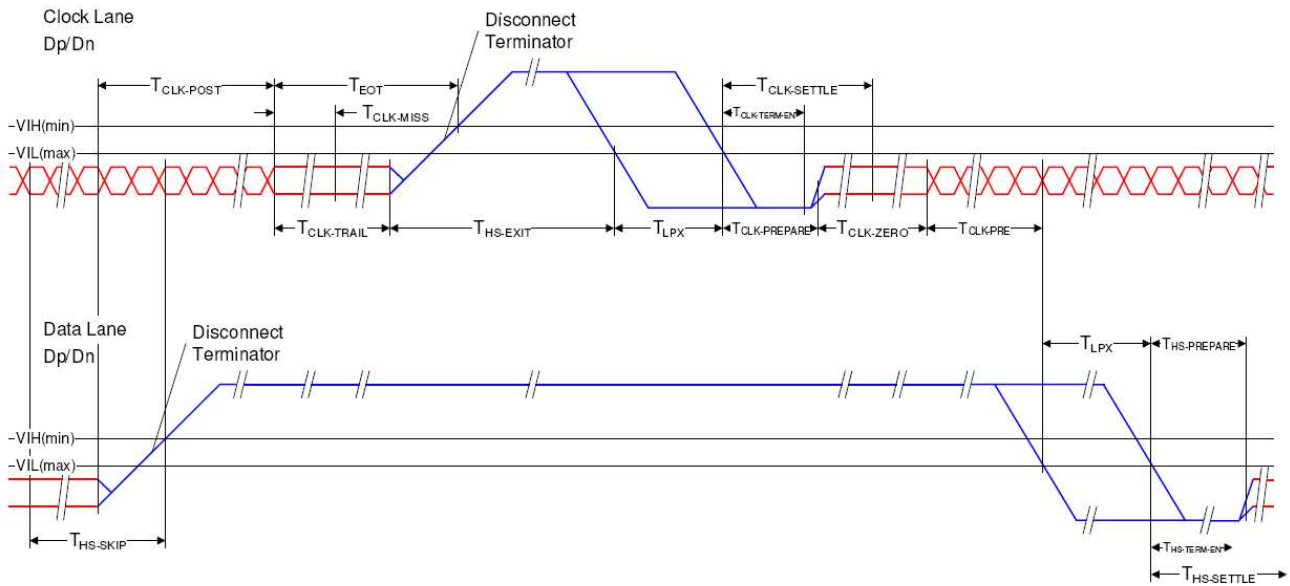
- 1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
- 2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
- 3: T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure

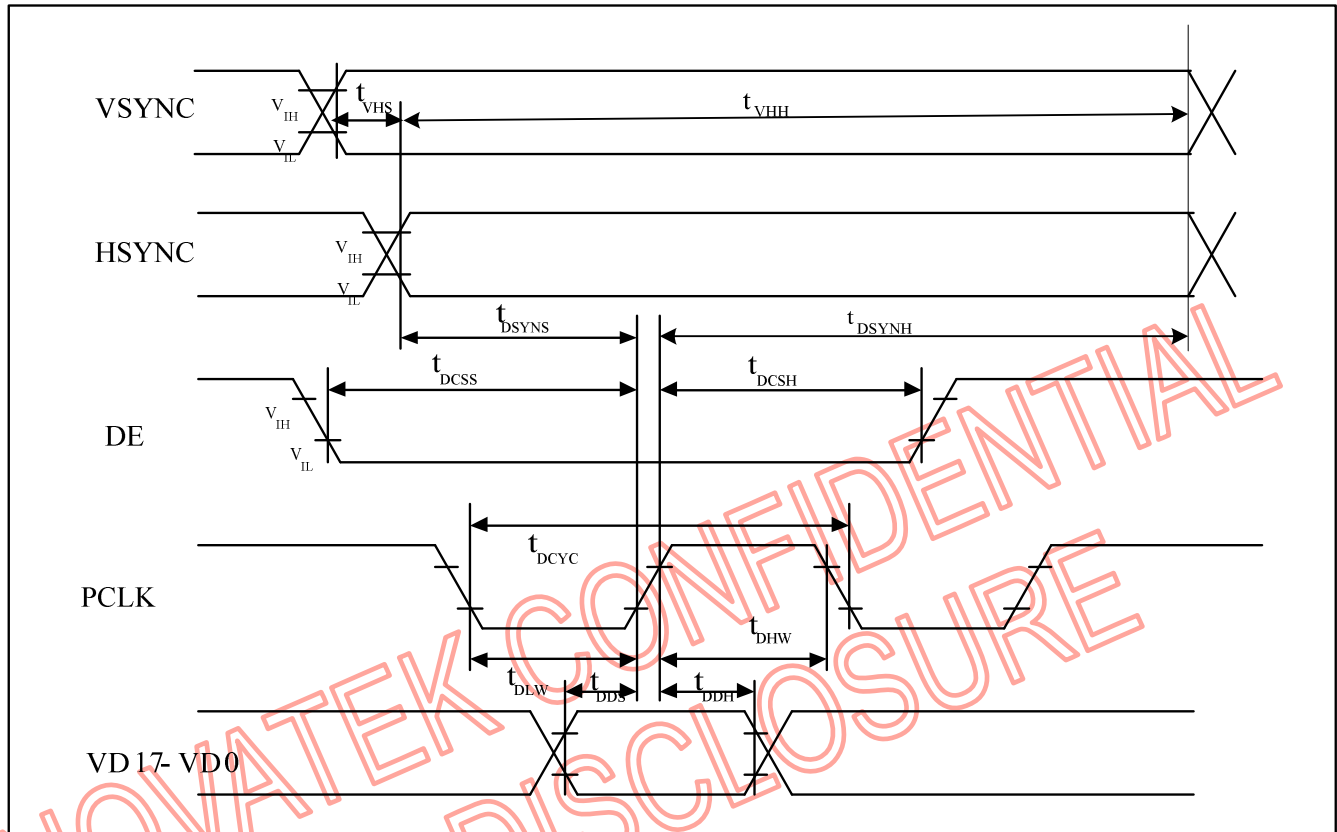


Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of $T_{LPX}(MASTER)/T_{LPX}(SLAVE)$ between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode

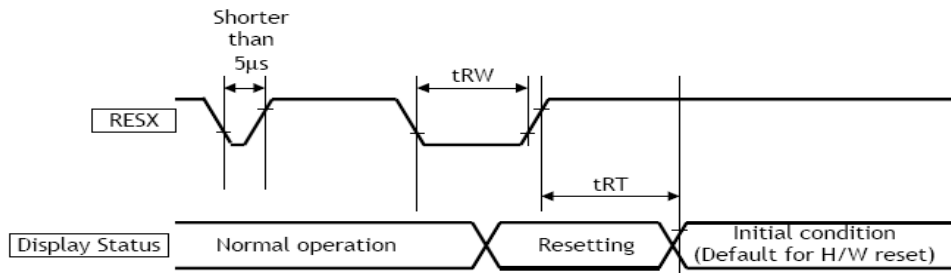


Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	$60+52UI$			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

7.3.6 RGB Interface Characteristics

Fig. 7.3.10 RGB Interface characteristics
AGND=0V, DGND=0V, VCI=2.3V~3.3, VDDI=1.65V to 3.3V, Ta = -30 to 70°C

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{DCYC}	PCLK cycle time	-	PCLK	60	-	-	
t_{DLW}	PCLK Low time	-	PCLK	20	-	-	ns
t_{DHS}	PCLK High time	-	PCLK	20	-	-	
t_{DDS}	RGB Data setup time	-	PCLK, D17-D0	5	-	-	ns
t_{DDH}	RGB Data hold time	-	PCLK, D17-D0	5	-	-	ns
t_{DCSS}	DE setup time	-	DE	5	-	-	ns
t_{DCSH}	DE hold Time	-	DE	5	-	-	ns
t_{DSYNS}	SYNC hold time	-	PCLK, HSYNC, VSYNC	5	-	-	ns
t_{VHH}	VSYNC hold time	-	PCLK, HSYNC, VSYNC	5	-	-	ns
t_{VHS}	VS leading time	-	VSYNC, HSYNC	400	-	-	ns

7.3.7 Reset Timing Characteristics



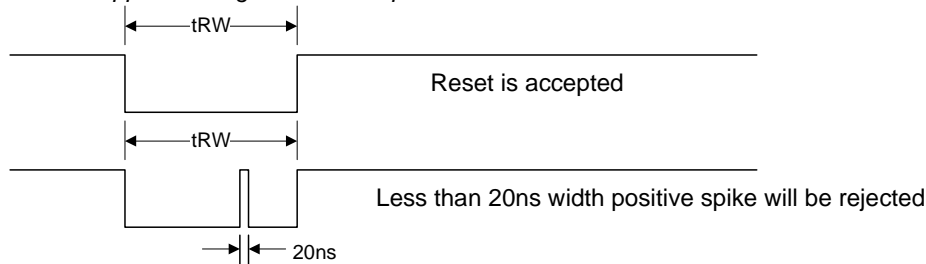
SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT
RESX	tRW	Reset pulse duration	10 (Note)		us
	tRT	Reset cancel		5 (Note) 120 (Note)	ms

Note :

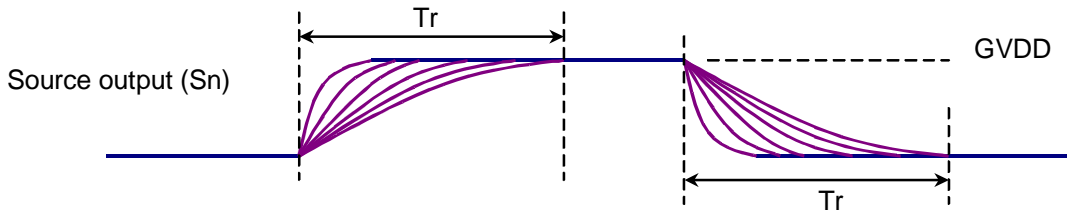
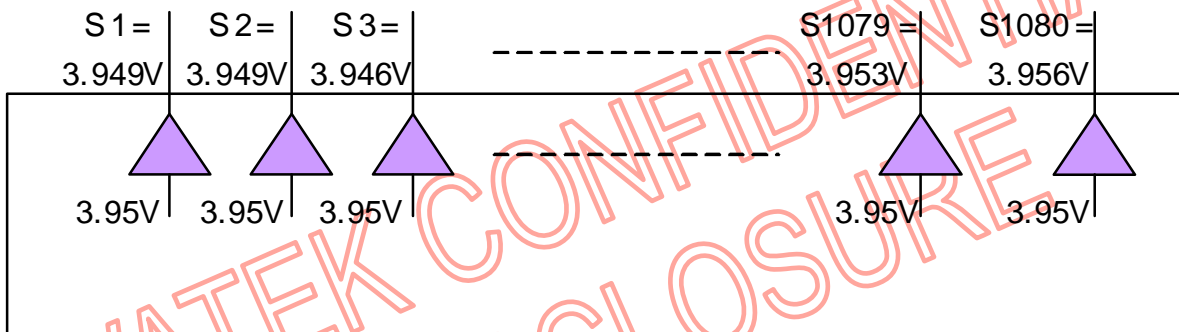
- The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

– RESX	– PULSE ACTION
– Shorter than 5us	– Reset Rejected
– Longer than 9us	– Reset
– Between 5us and 9us	– Reset starts

- During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep-Out mode. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.
- Spike Rejection also applies during a valid reset pulse as shown below :



- When Reset applied during Sleep-In Mode.
- When Reset applied during Sleep-Out Mode.
- It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

7.3.15 Liquid Crystal Driver Output Characteristics

Table 7.3.13 Liquid Crystal Driver Output Characteristics

Fig. 7.3.14 Source output deviation (Channel by Channel)

-When $S_{out} \geq 4.2V$, $S_{out} \leq 0.8V$

$$\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) \leq 35\text{mV}$$

-When $4.2V > S_{out} > 0.8V$

$$\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) \leq 25\text{mV}$$

-Example

When S_{out} level is 3.95V (Gray scale voltage)

$$\text{Max}(S1, S2, S3, \dots, S1080) = 3.969\text{V}$$

$$\text{Min}(S1, S2, S3, \dots, S1080) = 3.943\text{V}$$

S_{out} deviation =

$$\text{Max}(S1, S2, S3, \dots, S1080) - \text{Min}(S1, S2, S3, \dots, S1080) = 26\text{mV} \leftarrow \text{Out Spec}$$

8. REFERENCE APPLICATIONS
External Components Table1 :
Case1 : Appropriate for light panel loading
(1) CP1_MODE = 0, PUMP_MODE[1:0] = 01 (AVDD = VCI X 2)

Pad Name	Connection	Typical Value
VDDI	Interface Power VDDI ----- ----- GND (Option)	2.2μF
VCI	DC-DC, Analog and Regulator Power VCI ----- ----- GND (Option)	2.2μF
VSS,AVSS	Connect to GND	
VDD	Connect to Capacitor (Max 10V): VDD ----- ----- GND	1.0μF
VCOM	Connect to Capacitor (Max 10V): VCOM ----- ----- GND (Option)	2.2μF
VLPH	Connect to Capacitor (Max 10V): VLPH ----- ----- GND (Option)	1.0μF (Note 1)
C11P, C11M	Connect to Capacitor (Max 10V): C11P ----- ----- C11M	1.0μF
C12P, C12M	Connect to Capacitor (Max 10V): C12P ----- ----- C12M	1.0μF
C13P, C13M	Connect to Capacitor (Max 16V): C13P ----- ----- C13M	1.0μF
C21P, C21M	Connect to Capacitor (Max 10V): C21P ----- ----- C21M	1.0μF
C22P, C22M	Connect to Capacitor (Max 10V): C22P ----- ----- C22M	1.0μF
AVDD	Connect to Capacitor (Max 10V): AVDD ----- ----- GND (Option)	1.0μF ~ 2.2μF
AVEE	Connect to Capacitor (Max 10V): AVEE ----- ----- GND (Option)	1.0μF ~ 2.2μF
VCL	Connect to Capacitor (Max 10V): VCL ----- ----- GND (Option)	2.2μF
VGH	Connect to Capacitor (Max 26V): VGH ----- ----- GND	1.0μF
VGL	Connect to Capacitor (Max 26V): VGL ----- ----- GND	1.0μF

Note: 1. The capacitor of VLPH can be removed when MIPI DSI and MDDI is not applied.
Total : 8 Cap.
Note2: In case1, AVDD/AVEE/VCL can't be adjust.
*Note3: AVDD = 2 * VCI.*

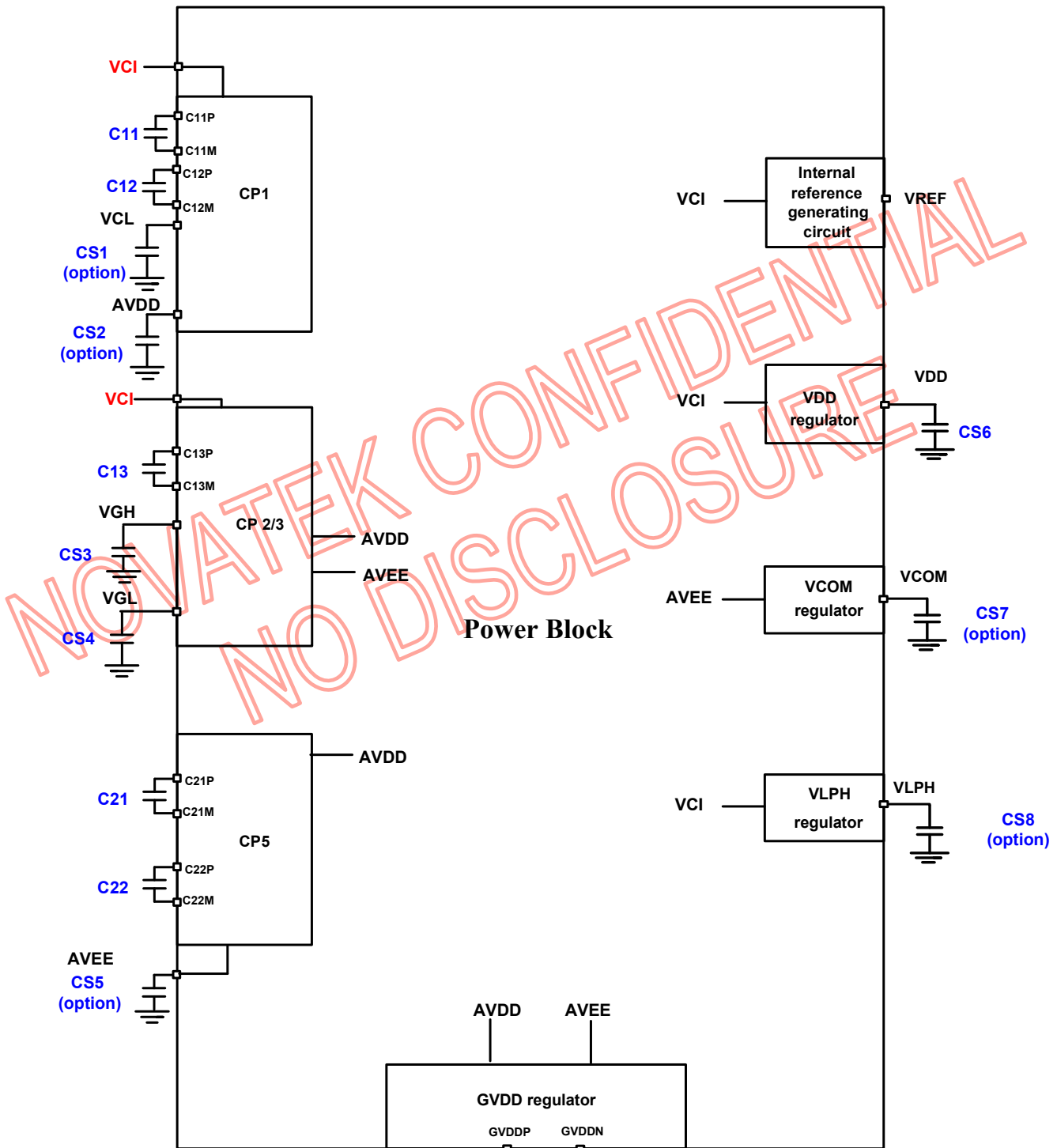
External Components Table2 :
Case2 : Appropriate for heavier panel loading
(1) CP1_MODE = 1, PUMP_MODE[1:0] = 01 or 10 (AVDD = VCI x 2 or VCI X 3)

Pad Name	Connection	Typical Value
VDDI	Interface Power VDDI ----- ----- GND (Option)	2.2μF
VCI	DC-DC, Analog and Regulator Power VCI ----- ----- GND (Option)	2.2μF
VSS,AVSS	Connect to GND	
VDD	Connect to Capacitor (Max 10V): VDD ----- ----- GND	1.0μF
VCOM	Connect to Capacitor (Max 10V): VCOM ----- ----- GND (Option)	2.2μF
VLPH	Connect to Capacitor (Max 10V): VLPH ----- ----- GND (Option)	1.0μF (Note 1)
C11P, C11M	Connect to Capacitor (Max 10V): C11P ----- ----- C11M	1.0μF
C12P, C12M	Connect to Capacitor (Max 10V): C12P ----- ----- C12M	1.0μF
C13P, C13M	Connect to Capacitor (Max 16V): C13P ----- ----- C13M	1.0μF
C21P, C21M	Connect to Capacitor (Max 10V): C21P ----- ----- C21M	1.0μF
C22P, C22M	Connect to Capacitor (Max 10V): C22P ----- ----- C22M	1.0μF
AVDD	Connect to Capacitor (Max 10V): AVDD ----- ----- GND	1.0μF ~ 2.2μF
AVEE	Connect to Capacitor (Max 10V): AVEE ----- ----- GND (Option)	1.0μF ~ 2.2μF
VCL	Connect to Capacitor (Max 10V): VCL ----- ----- GND	2.2μF
VGH	Connect to Capacitor (Max 26V): VGH ----- ----- GND	1.0μF
VGL	Connect to Capacitor (Max 26V): VGL ----- ----- GND	1.0μF

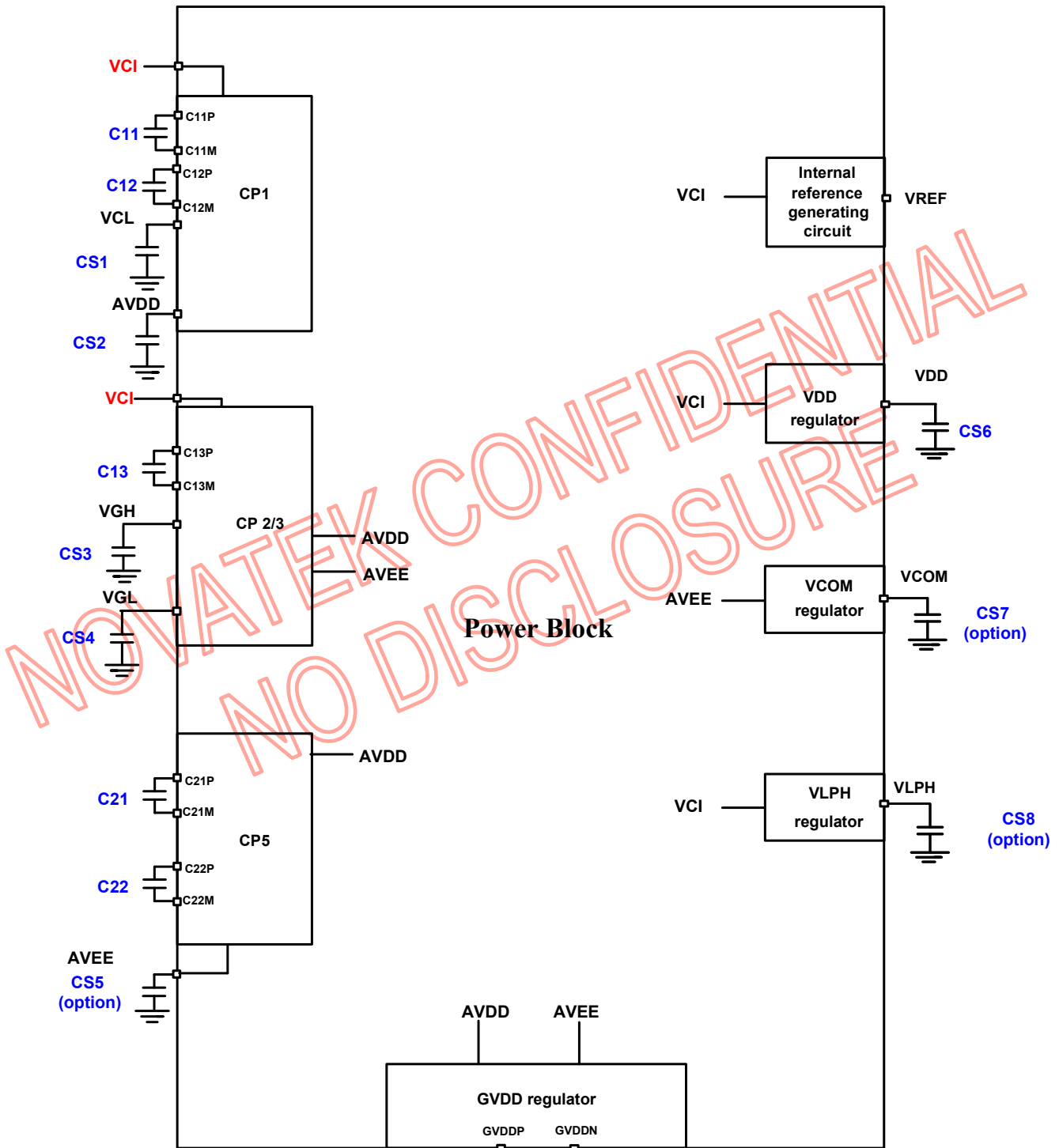
Note: 1. The capacitor of VLPH can be removed when MIPI DSI and MDDI is not applied.
Total : 10 Cap.
Note2: In case2,AVDD/AVEE/VCL/VGH/VGL can fine tune Pump CLK.
*Note3: AVDD = 2 * VCI or 3*VCI.*

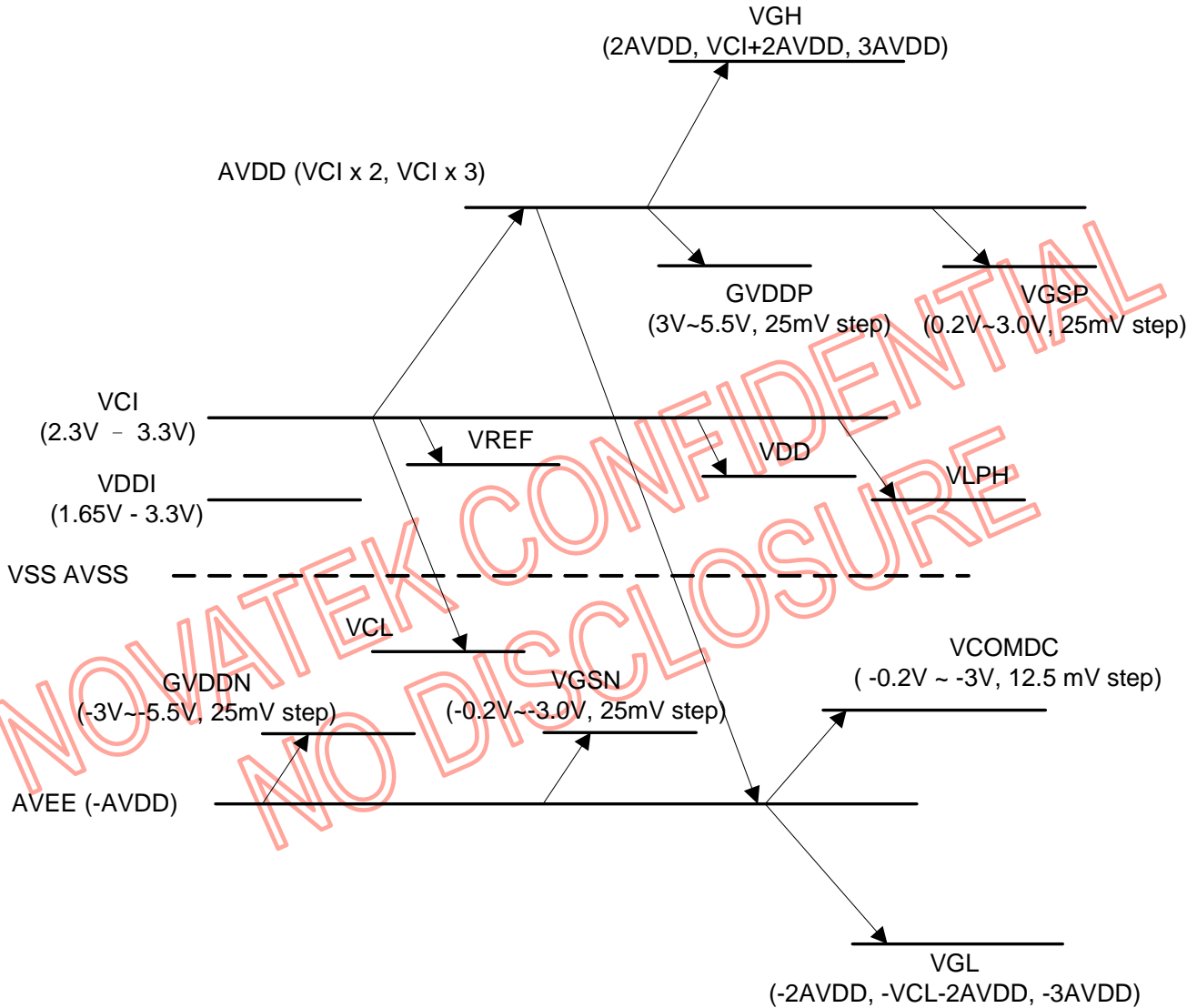
8.1 Connect example with external components

Case 1: CP1_MODE = 0, PUMP_MODE[1:0] = 01 (AVDD = VCI X 2)



Case 2 : (1) CP1_MODE = 0, PUMP_MODE[1:0] = 10 (AVDD = VCI X 3)
 (2) CP1_MODE = 1, PUMP_MODE[1:0] = 01 or 10 (AVDD = VCI x 2 or VCI X 3)



8.2 Power Scheme


8.3 Maximum Series Resistance

The driver will operate in 'Chip on Glass' applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Maximum series resistance on module

Name	Type	Maximum Series Resistance	Unit
MTP_PWR	Power supply	10	Ω
VDDI	Power supply	3	Ω
VCI	Power supply	3	Ω
AVSS	Power supply	3	Ω
VSS	Power supply	3	Ω
IM[2:0]	Input	100	Ω
RDX, WRX_SCL, DCX, CSX, DIN_SDA, DOUT	Input	100	Ω
RESX	Input	100	Ω
TE, LEDPWM1, LEDPWM2, TE1/IDLE_ON	Output	100	Ω
DB[17:0]	I/O	100	Ω
HSSI_CLK_P, HSSI_CLK_N HSSI_D0_P, HSSI_D0_N	I/O	10	Ω
PCLK, DE, VSYNC, HSYNC	Input	100	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
VLPH	Capacitor connection	20	Ω
VCOM	Capacitor connection	5	Ω
AVDD	Capacitor connection	3	Ω
AVEE	Capacitor connection	3	Ω
VDD	Capacitor connection	5	Ω
VCL	Capacitor connection	5	Ω
GVDDP, GVDDN, VREF	Output	10	Ω
C13P, C13M,	Capacitor connection	5	Ω
C11P, C11M, C12P, C12M C21P, C21M, C22P, C22M	Capacitor connection	3	Ω

9. CHIP INFORMATION

9.1 CHIP INFORMATION

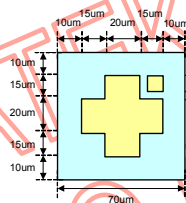
9.1.1 CHIP OVERVIEW

Chip size: 22780um x 761um

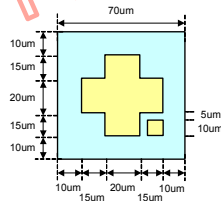
Coordinate origin: Chip center

Bump size: Input PAD = 81um(height) x 50um(width)
Output PAD = 99um(height) x 15um(width)

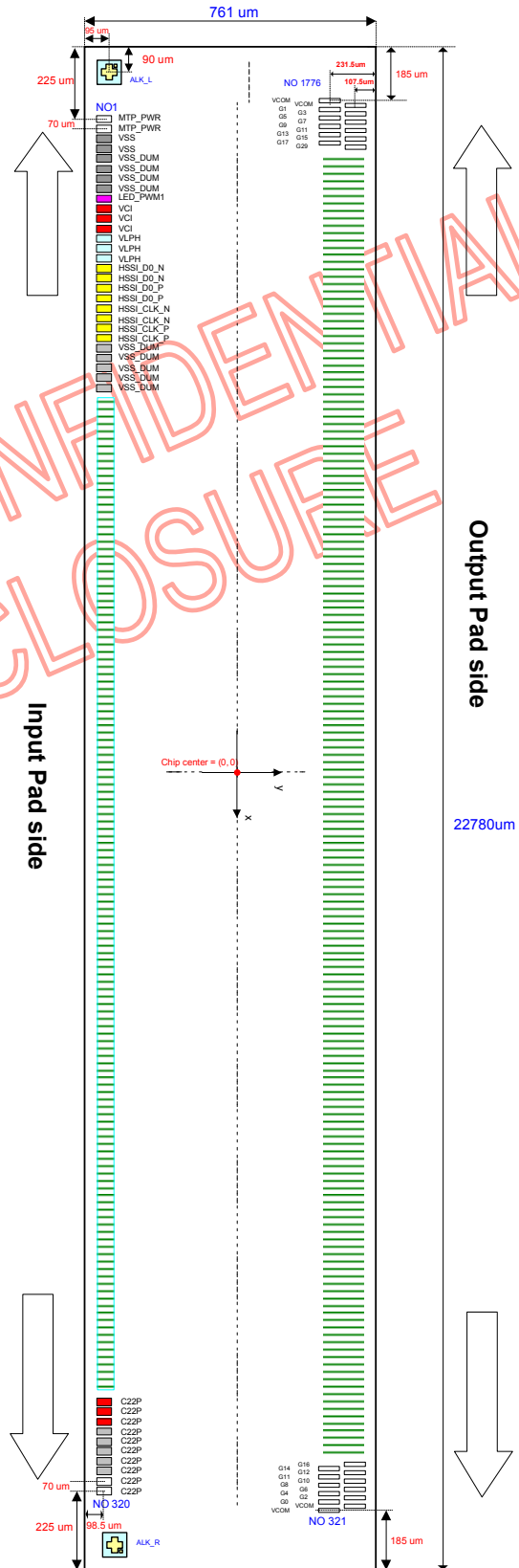
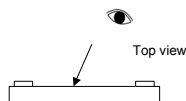
ALK_L



ALK_R

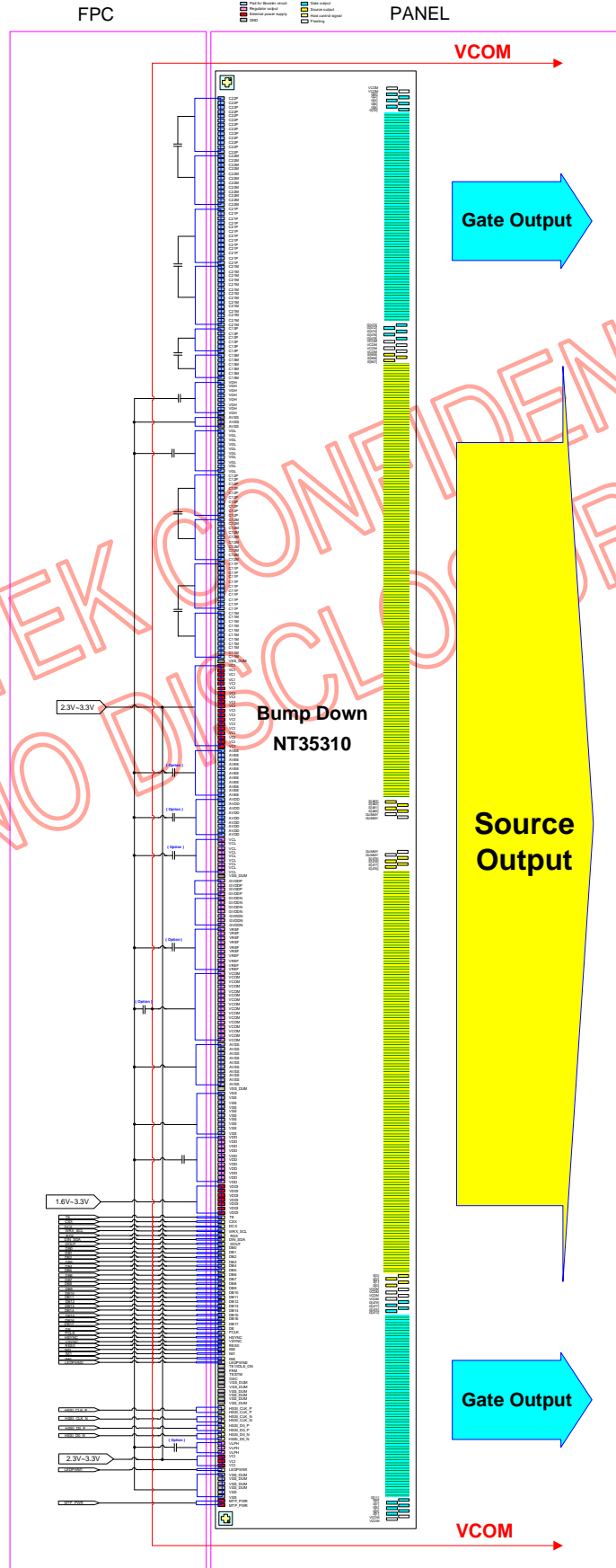


View point



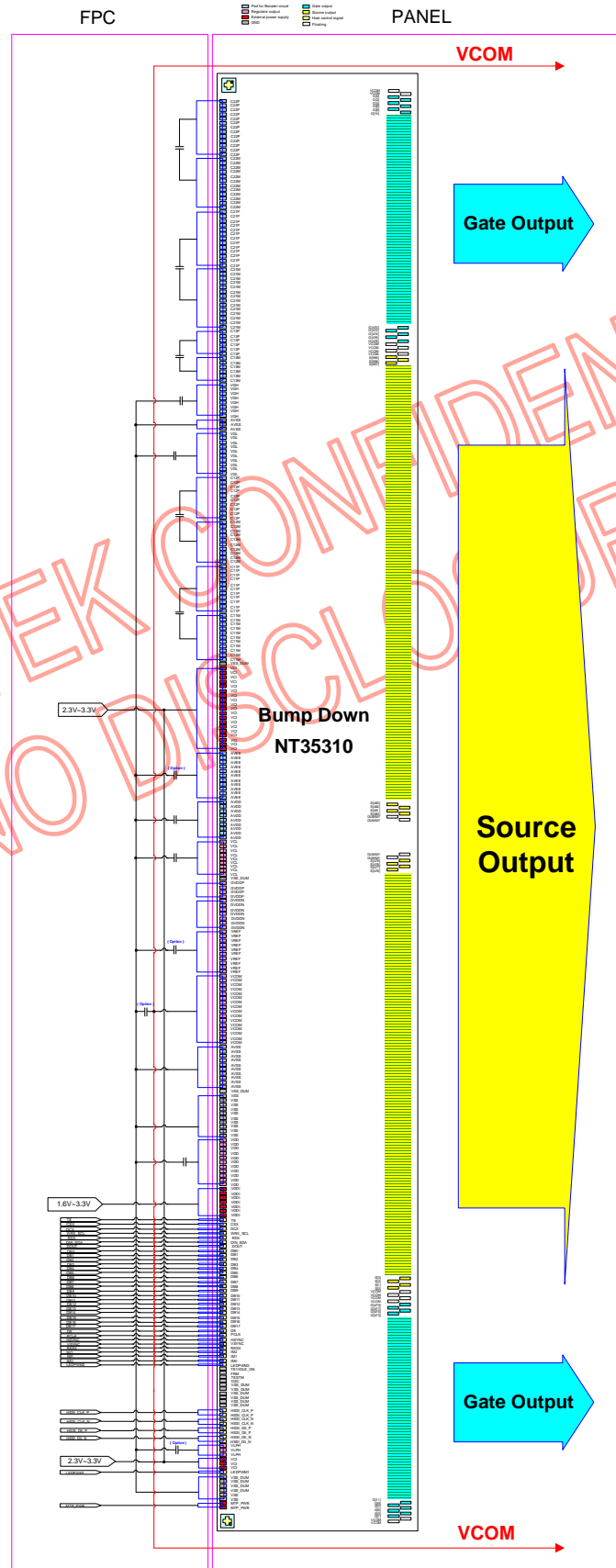
9.1.2 Application Circuit

Case1: CP1_MODE = 0, PUMP_MODE[1:0] = 01 (AVDD = VCI X 2)



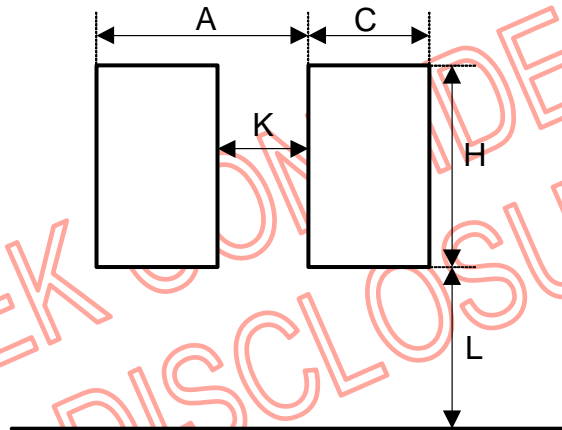
Case 2:

- (1) CP1_MODE = 0, PUMP_MODE[1:0] = 10 (AVDD = VCI X 3)
- (2) CP1_MODE = 1, PUMP_MODE[1:0] = 01 or 10 (AVDD = VCI x 2 or VCI X 3)



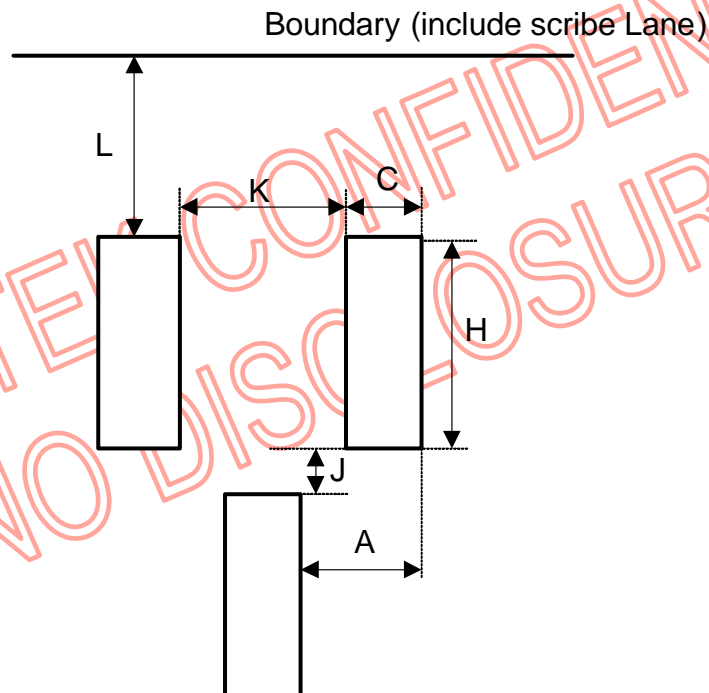
9.2 BUMP INFORMATION
9.2.1 Input PAD Format

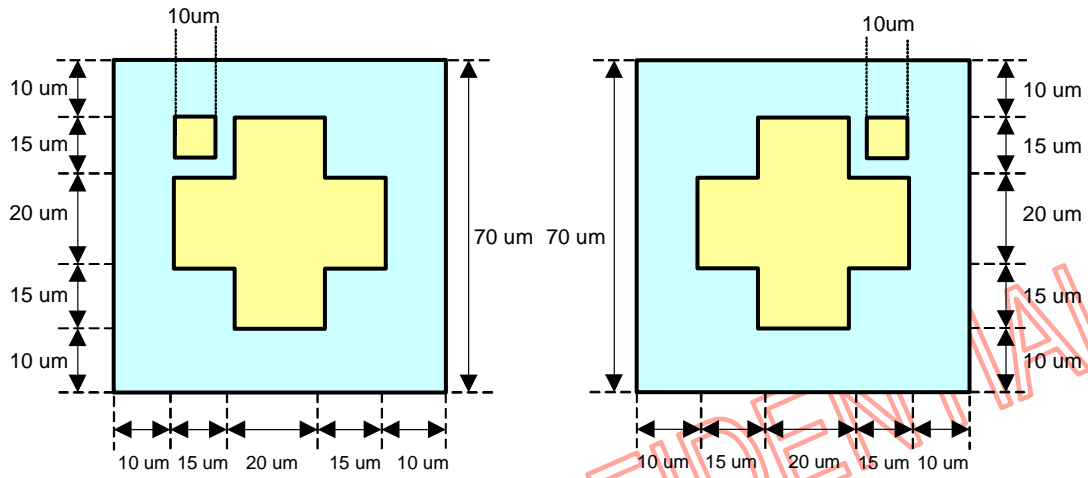
Item	Symbol	Size
Pad pitch	A	70 um
Bump width	C	50 um
Bump height	H	81 um
Bump to bump gap	K	20 um
Bump area	C*H	4050 um ²
Chip boundary to bump edge	L	58 um



9.2.2 Output PAD Fotmat

Item	Symbol	Size
Pad pitch	A	15 um
Bump width	C	15 um
Bump height	H	99 um
Bump to bump gap (Vertical)	J	25 um
Bump to bump gap (Horizontal)	K	15 um
Bump area	C*H	1485um ²
Chip boundary to bump edge	L	58 um



9.2.3 Alignment Mark Information


NOVATEK CONFIDENTIAL
NO DISCLOSURE

9.3 PAD COORDINATES

9.3.1 For Panel Resolution: 320(RGB)*480

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1	MTP_PWR	-11165	-282	53	D7	-7525	-282	105	AVSS	-3885	-282
2	MTP_PWR	-11095	-282	54	D6	-7455	-282	106	AVSS	-3815	-282
3	VSS	-11025	-282	55	D5	-7385	-282	107	VCOM	-3745	-282
4	VSS	-10955	-282	56	D4	-7315	-282	108	VCOM	-3675	-282
5	VSS_DUM	-10885	-282	57	D3	-7245	-282	109	VCOM	-3605	-282
6	VSS_DUM	-10815	-282	58	D2	-7175	-282	110	VCOM	-3535	-282
7	VSS_DUM	-10745	-282	59	D1	-7105	-282	111	VCOM	-3465	-282
8	VSS_DUM	-10675	-282	60	D0	-7035	-282	112	VCOM	-3395	-282
9	LEDPWM1	-10605	-282	61	DOUT	-6965	-282	113	VCOM	-3325	-282
10	VCI	-10535	-282	62	DIN_SDA	-6895	-282	114	VCOM	-3255	-282
11	VCI	-10465	-282	63	RDX	-6825	-282	115	VCOM	-3185	-282
12	VCI	-10395	-282	64	WRX_SCL	-6755	-282	116	VCOM	-3115	-282
13	VLPH	-10325	-282	65	DCX	-6685	-282	117	VCOM	-3045	-282
14	VLPH	-10255	-282	66	CSX	-6615	-282	118	VCOM	-2975	-282
15	VLPH	-10185	-282	67	TE	-6545	-282	119	VCOM	-2905	-282
16	HSSI_D0_N	-10115	-282	68	VDDI	-6475	-282	120	VCOM	-2835	-282
17	HSSI_D0_N	-10045	-282	69	VDDI	-6405	-282	121	VCOM	-2765	-282
18	HSSI_D0_P	-9975	-282	70	VDDI	-6335	-282	122	VCOM	-2695	-282
19	HSSI_D0_P	-9905	-282	71	VDDI	-6265	-282	123	VREF	-2625	-282
20	HSSI_CLK_N	-9835	-282	72	VDDI	-6195	-282	124	VREF	-2555	-282
21	HSSI_CLK_N	-9765	-282	73	VDDI	-6125	-282	125	VREF	-2485	-282
22	HSSI_CLK_P	-9695	-282	74	VDDI	-6055	-282	126	VREF	-2415	-282
23	HSSI_CLK_P	-9625	-282	75	VDD	-5985	-282	127	VREF	-2345	-282
24	VSS_DUM	-9555	-282	76	VDD	-5915	-282	128	VREF	-2275	-282
25	VSS_DUM	-9485	-282	77	VDD	-5845	-282	129	VREF	-2205	-282
26	VSS_DUM	-9415	-282	78	VDD	-5775	-282	130	VREF	-2135	-282
27	VSS_DUM	-9345	-282	79	VDD	-5705	-282	131	VREF	-2065	-282
28	VSS_DUM	-9275	-282	80	VDD	-5635	-282	132	VREF	-1995	-282
29	VSS_DUM	-9205	-282	81	VDD	-5565	-282	133	GVDDN	-1925	-282
30	OSC	-9135	-282	82	VDD	-5495	-282	134	GVDDN	-1855	-282
31	TESTM	-9065	-282	83	VDD	-5425	-282	135	GVDDN	-1785	-282
32	FRM	-8995	-282	84	VDD	-5355	-282	136	GVDDN	-1715	-282
33	TE1/IDLE_ON	-8925	-282	85	VDD	-5285	-282	137	GVDDN	-1645	-282
34	LEDPWM2	-8855	-282	86	VSS	-5215	-282	138	GVDDN	-1575	-282
35	IM0	-8785	-282	87	VSS	-5145	-282	139	GVDDN	-1505	-282
36	IM1	-8715	-282	88	VSS	-5075	-282	140	GVDDP	-1435	-282
37	IM2	-8645	-282	89	VSS	-5005	-282	141	GVDDP	-1365	-282
38	RESX	-8575	-282	90	VSS	-4935	-282	142	GVDDP	-1295	-282
39	VS	-8505	-282	91	VSS	-4865	-282	143	GVDDP	-1225	-282
40	HS	-8435	-282	92	VSS	-4795	-282	144	VSS_DUM	-1155	-282
41	PCLK	-8365	-282	93	VSS	-4725	-282	145	VCL	-1085	-282
42	DE	-8295	-282	94	VSS	-4655	-282	146	VCL	-1015	-282
43	D17	-8225	-282	95	VSS	-4585	-282	147	VCL	-945	-282
44	D16	-8155	-282	96	VSS_DUM	-4515	-282	148	VCL	-875	-282
45	D15	-8085	-282	97	AVSS	-4445	-282	149	VCL	-805	-282
46	D14	-8015	-282	98	AVSS	-4375	-282	150	VCL	-735	-282
47	D13	-7945	-282	99	AVSS	-4305	-282	151	VCL	-665	-282
48	D12	-7875	-282	100	AVSS	-4235	-282	152	VCL	-595	-282
49	D11	-7805	-282	101	AVSS	-4165	-282	153	VCL	-525	-282
50	D10	-7735	-282	102	AVSS	-4095	-282	154	AVDD	-455	-282
51	D9	-7665	-282	103	AVSS	-4025	-282	155	AVDD	-385	-282
52	D8	-7595	-282	104	AVSS	-3955	-282	156	AVDD	-315	-282

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
157	AVDD	-245	-282	209	C11P	3395	-282	261	C13M	7035	-282
158	AVDD	-175	-282	210	C11P	3465	-282	262	C13M	7105	-282
159	AVDD	-105	-282	211	C11P	3535	-282	263	C13P	7175	-282
160	AVDD	-35	-282	212	C11P	3605	-282	264	C13P	7245	-282
161	AVDD	35	-282	213	C11P	3675	-282	265	C13P	7315	-282
162	AVDD	105	-282	214	C11P	3745	-282	266	C13P	7385	-282
163	AVEE	175	-282	215	C11P	3815	-282	267	C13P	7455	-282
164	AVEE	245	-282	216	C12M	3885	-282	268	C13P	7525	-282
165	AVEE	315	-282	217	C12M	3955	-282	269	C21M	7595	-282
166	AVEE	385	-282	218	C12M	4025	-282	270	C21M	7665	-282
167	AVEE	455	-282	219	C12M	4095	-282	271	C21M	7735	-282
168	AVEE	525	-282	220	C12M	4165	-282	272	C21M	7805	-282
169	AVEE	595	-282	221	C12M	4235	-282	273	C21M	7875	-282
170	AVEE	665	-282	222	C12M	4305	-282	274	C21M	7945	-282
171	AVEE	735	-282	223	C12M	4375	-282	275	C21M	8015	-282
172	AVEE	805	-282	224	C12M	4445	-282	276	C21M	8085	-282
173	AVEE	875	-282	225	C12M	4515	-282	277	C21M	8155	-282
174	VCI	945	-282	226	C12P	4585	-282	278	C21M	8225	-282
175	VCI	1015	-282	227	C12P	4655	-282	279	C21M	8295	-282
176	VCI	1085	-282	228	C12P	4725	-282	280	C21M	8365	-282
177	VCI	1155	-282	229	C12P	4795	-282	281	C21M	8435	-282
178	VCI	1225	-282	230	C12P	4865	-282	282	C21M	8505	-282
179	VCI	1295	-282	231	C12P	4935	-282	283	C21P	8575	-282
180	VCI	1365	-282	232	C12P	5005	-282	284	C21P	8645	-282
181	VCI	1435	-282	233	C12P	5075	-282	285	C21P	8715	-282
182	VCI	1505	-282	234	C12P	5145	-282	286	C21P	8785	-282
183	VCI	1575	-282	235	C12P	5215	-282	287	C21P	8855	-282
184	VCI	1645	-282	236	VGL	5285	-282	288	C21P	8925	-282
185	VCI	1715	-282	237	VGL	5355	-282	289	C21P	8995	-282
186	VCI	1785	-282	238	VGL	5425	-282	290	C21P	9065	-282
187	VCI	1855	-282	239	VGL	5495	-282	291	C21P	9135	-282
188	VCI	1925	-282	240	VGL	5565	-282	292	C21P	9205	-282
189	VCI	1995	-282	241	VGLO	5635	-282	293	C21P	9275	-282
190	VCI	2065	-282	242	VGLO	5705	-282	294	C21P	9345	-282
191	VCI	2135	-282	243	VGLO	5775	-282	295	C21P	9415	-282
192	VCI	2205	-282	244	VGLO	5845	-282	296	C22M	9485	-282
193	VSS_DUM	2275	-282	245	VGLO	5915	-282	297	C22M	9555	-282
194	C11M	2345	-282	246	CVSS	5985	-282	298	C22M	9625	-282
195	C11M	2415	-282	247	CVSS	6055	-282	299	C22M	9695	-282
196	C11M	2485	-282	248	CVSS	6125	-282	300	C22M	9765	-282
197	C11M	2555	-282	249	VGH	6195	-282	301	C22M	9835	-282
198	C11M	2625	-282	250	VGH	6265	-282	302	C22M	9905	-282
199	C11M	2695	-282	251	VGH	6335	-282	303	C22M	9975	-282
200	C11M	2765	-282	252	VGH	6405	-282	304	C22M	10045	-282
201	C11M	2835	-282	253	VGH	6475	-282	305	C22M	10115	-282
202	C11M	2905	-282	254	VGH	6545	-282	306	C22M	10185	-282
203	C11M	2975	-282	255	VGH	6615	-282	307	C22M	10255	-282
204	C11M	3045	-282	256	VGH	6685	-282	308	C22P	10325	-282
205	C11P	3115	-282	257	C13M	6755	-282	309	C22P	10395	-282
206	C11P	3185	-282	258	C13M	6825	-282	310	C22P	10465	-282
207	C11P	3255	-282	259	C13M	6895	-282	311	C22P	10535	-282
208	C11P	3325	-282	260	C13M	6965	-282	312	C22P	10605	-282

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
313	C22P	10675	-282	365	G84	10545	149	417	G188	9765	149
314	C22P	10745	-282	366	G86	10530	273	418	G190	9750	273
315	C22P	10815	-282	367	G88	10515	149	419	G192	9735	149
316	C22P	10885	-282	368	G90	10500	273	420	G194	9720	273
317	C22P	10955	-282	369	G92	10485	149	421	G196	9705	149
318	C22P	11025	-282	370	G94	10470	273	422	G198	9690	273
319	C22P	11095	-282	371	G96	10455	149	423	G200	9675	149
320	C22P	11165	-282	372	G98	10440	273	424	G202	9660	273
321	VCOM	11205	149	373	G100	10425	149	425	G204	9645	149
322	VCOM	11190	273	374	G102	10410	273	426	G206	9630	273
323	G0	11175	149	375	G104	10395	149	427	G208	9615	149
324	G2	11160	273	376	G106	10380	273	428	G210	9600	273
325	G4	11145	149	377	G108	10365	149	429	G212	9585	149
326	G6	11130	273	378	G110	10350	273	430	G214	9570	273
327	G8	11115	149	379	G112	10335	149	431	G216	9555	149
328	G10	11100	273	380	G114	10320	273	432	G218	9540	273
329	G12	11085	149	381	G116	10305	149	433	G220	9525	149
330	G14	11070	273	382	G118	10290	273	434	G222	9510	273
331	G16	11055	149	383	G120	10275	149	435	G224	9495	149
332	G18	11040	273	384	G122	10260	273	436	G226	9480	273
333	G20	11025	149	385	G124	10245	149	437	G228	9465	149
334	G22	11010	273	386	G126	10230	273	438	G230	9450	273
335	G24	10995	149	387	G128	10215	149	439	G232	9435	149
336	G26	10980	273	388	G130	10200	273	440	G234	9420	273
337	G28	10965	149	389	G132	10185	149	441	G236	9405	149
338	G30	10950	273	390	G134	10170	273	442	G238	9390	273
339	G32	10935	149	391	G136	10155	149	443	G240	9375	149
340	G34	10920	273	392	G138	10140	273	444	G242	9360	273
341	G36	10905	149	393	G140	10125	149	445	G244	9345	149
342	G38	10890	273	394	G142	10110	273	446	G246	9330	273
343	G40	10875	149	395	G144	10095	149	447	G248	9315	149
344	G42	10860	273	396	G146	10080	273	448	G250	9300	273
345	G44	10845	149	397	G148	10065	149	449	G252	9285	149
346	G46	10830	273	398	G150	10050	273	450	G254	9270	273
347	G48	10815	149	399	G152	10035	149	451	G256	9255	149
348	G50	10800	273	400	G154	10020	273	452	G258	9240	273
349	G52	10785	149	401	G156	10005	149	453	G260	9225	149
350	G54	10770	273	402	G158	9990	273	454	G262	9210	273
351	G56	10755	149	403	G160	9975	149	455	G264	9195	149
352	G58	10740	273	404	G162	9960	273	456	G266	9180	273
353	G60	10725	149	405	G164	9945	149	457	G268	9165	149
354	G62	10710	273	406	G166	9930	273	458	G270	9150	273
355	G64	10695	149	407	G168	9915	149	459	G272	9135	149
356	G66	10680	273	408	G170	9900	273	460	G274	9120	273
357	G68	10665	149	409	G172	9885	149	461	G276	9105	149
358	G70	10650	273	410	G174	9870	273	462	G278	9090	273
359	G72	10635	149	411	G176	9855	149	463	G280	9075	149
360	G74	10620	273	412	G178	9840	273	464	G282	9060	273
361	G76	10605	149	413	G180	9825	149	465	G284	9045	149
362	G78	10590	273	414	G182	9810	273	466	G286	9030	273
363	G80	10575	149	415	G184	9795	149	467	G288	9015	149
364	G82	10560	273	416	G186	9780	273	468	G290	9000	273

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
469	G292	8985	149	521	G396	8205	149	573	S953	7275	149
470	G294	8970	273	522	G398	8190	273	574	S952	7260	273
471	G296	8955	149	523	G400	8175	149	575	S951	7245	149
472	G298	8940	273	524	G402	8160	273	576	S950	7230	273
473	G300	8925	149	525	G404	8145	149	577	S949	7215	149
474	G302	8910	273	526	G406	8130	273	578	S948	7200	273
475	G304	8895	149	527	G408	8115	149	579	S947	7185	149
476	G306	8880	273	528	G410	8100	273	580	S946	7170	273
477	G308	8865	149	529	G412	8085	149	581	S945	7155	149
478	G310	8850	273	530	G414	8070	273	582	S944	7140	273
479	G312	8835	149	531	G416	8055	149	583	S943	7125	149
480	G314	8820	273	532	G418	8040	273	584	S942	7110	273
481	G316	8805	149	533	G420	8025	149	585	S941	7095	149
482	G318	8790	273	534	G422	8010	273	586	S940	7080	273
483	G320	8775	149	535	G424	7995	149	587	S939	7065	149
484	G322	8760	273	536	G426	7980	273	588	S938	7050	273
485	G324	8745	149	537	G428	7965	149	589	S937	7035	149
486	G326	8730	273	538	G430	7950	273	590	S936	7020	273
487	G328	8715	149	539	G432	7935	149	591	S935	7005	149
488	G330	8700	273	540	G434	7920	273	592	S934	6990	273
489	G332	8685	149	541	G436	7905	149	593	S933	6975	149
490	G334	8670	273	542	G438	7890	273	594	S932	6960	273
491	G336	8655	149	543	G440	7875	149	595	S931	6945	149
492	G338	8640	273	544	G442	7860	273	596	S930	6930	273
493	G340	8625	149	545	G444	7845	149	597	S929	6915	149
494	G342	8610	273	546	G446	7830	273	598	S928	6900	273
495	G344	8595	149	547	G448	7815	149	599	S927	6885	149
496	G346	8580	273	548	G450	7800	273	600	S926	6870	273
497	G348	8565	149	549	G452	7785	149	601	S925	6855	149
498	G350	8550	273	550	G454	7770	273	602	S924	6840	273
499	G352	8535	149	551	G456	7755	149	603	S923	6825	149
500	G354	8520	273	552	G458	7740	273	604	S922	6810	273
501	G356	8505	149	553	G460	7725	149	605	S921	6795	149
502	G358	8490	273	554	G462	7710	273	606	S920	6780	273
503	G360	8475	149	555	G464	7695	149	607	S919	6765	149
504	G362	8460	273	556	G466	7680	273	608	S918	6750	273
505	G364	8445	149	557	G468	7665	149	609	S917	6735	149
506	G366	8430	273	558	G470	7650	273	610	S916	6720	273
507	G368	8415	149	559	G472	7635	149	611	S915	6705	149
508	G370	8400	273	560	G474	7620	273	612	S914	6690	273
509	G372	8385	149	561	G476	7605	149	613	S913	6675	149
510	G374	8370	273	562	G478	7590	273	614	S912	6660	273
511	G376	8355	149	563	VCOM	7575	149	615	S911	6645	149
512	G378	8340	273	564	VCOM	7560	273	616	S910	6630	273
513	G380	8325	149	565	VCOM	7395	149	617	S909	6615	149
514	G382	8310	273	566	VCOM	7380	273	618	S908	6600	273
515	G384	8295	149	567	S959	7365	149	619	S907	6585	149
516	G386	8280	273	568	S958	7350	273	620	S906	6570	273
517	G388	8265	149	569	S957	7335	149	621	S905	6555	149
518	G390	8250	273	570	S956	7320	273	622	S904	6540	273
519	G392	8235	149	571	S955	7305	149	623	S903	6525	149
520	G394	8220	273	572	S954	7290	273	624	S902	6510	273

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
625	S901	6495	149	677	S849	5715	149	729	S797	4935	149
626	S900	6480	273	678	S848	5700	273	730	S796	4920	273
627	S899	6465	149	679	S847	5685	149	731	S795	4905	149
628	S898	6450	273	680	S846	5670	273	732	S794	4890	273
629	S897	6435	149	681	S845	5655	149	733	S793	4875	149
630	S896	6420	273	682	S844	5640	273	734	S792	4860	273
631	S895	6405	149	683	S843	5625	149	735	S791	4845	149
632	S894	6390	273	684	S842	5610	273	736	S790	4830	273
633	S893	6375	149	685	S841	5595	149	737	S789	4815	149
634	S892	6360	273	686	S840	5580	273	738	S788	4800	273
635	S891	6345	149	687	S839	5565	149	739	S787	4785	149
636	S890	6330	273	688	S838	5550	273	740	S786	4770	273
637	S889	6315	149	689	S837	5535	149	741	S785	4755	149
638	S888	6300	273	690	S836	5520	273	742	S784	4740	273
639	S887	6285	149	691	S835	5505	149	743	S783	4725	149
640	S886	6270	273	692	S834	5490	273	744	S782	4710	273
641	S885	6255	149	693	S833	5475	149	745	S781	4695	149
642	S884	6240	273	694	S832	5460	273	746	S780	4680	273
643	S883	6225	149	695	S831	5445	149	747	S779	4665	149
644	S882	6210	273	696	S830	5430	273	748	S778	4650	273
645	S881	6195	149	697	S829	5415	149	749	S777	4635	149
646	S880	6180	273	698	S828	5400	273	750	S776	4620	273
647	S879	6165	149	699	S827	5385	149	751	S775	4605	149
648	S878	6150	273	700	S826	5370	273	752	S774	4590	273
649	S877	6135	149	701	S825	5355	149	753	S773	4575	149
650	S876	6120	273	702	S824	5340	273	754	S772	4560	273
651	S875	6105	149	703	S823	5325	149	755	S771	4545	149
652	S874	6090	273	704	S822	5310	273	756	S770	4530	273
653	S873	6075	149	705	S821	5295	149	757	S769	4515	149
654	S872	6060	273	706	S820	5280	273	758	S768	4500	273
655	S871	6045	149	707	S819	5265	149	759	S767	4485	149
656	S870	6030	273	708	S818	5250	273	760	S766	4470	273
657	S869	6015	149	709	S817	5235	149	761	S765	4455	149
658	S868	6000	273	710	S816	5220	273	762	S764	4440	273
659	S867	5985	149	711	S815	5205	149	763	S763	4425	149
660	S866	5970	273	712	S814	5190	273	764	S762	4410	273
661	S865	5955	149	713	S813	5175	149	765	S761	4395	149
662	S864	5940	273	714	S812	5160	273	766	S760	4380	273
663	S863	5925	149	715	S811	5145	149	767	S759	4365	149
664	S862	5910	273	716	S810	5130	273	768	S758	4350	273
665	S861	5895	149	717	S809	5115	149	769	S757	4335	149
666	S860	5880	273	718	S808	5100	273	770	S756	4320	273
667	S859	5865	149	719	S807	5085	149	771	S755	4305	149
668	S858	5850	273	720	S806	5070	273	772	S754	4290	273
669	S857	5835	149	721	S805	5055	149	773	S753	4275	149
670	S856	5820	273	722	S804	5040	273	774	S752	4260	273
671	S855	5805	149	723	S803	5025	149	775	S751	4245	149
672	S854	5790	273	724	S802	5010	273	776	S750	4230	273
673	S853	5775	149	725	S801	4995	149	777	S749	4215	149
674	S852	5760	273	726	S800	4980	273	778	S748	4200	273
675	S851	5745	149	727	S799	4965	149	779	S747	4185	149
676	S850	5730	273	728	S798	4950	273	780	S746	4170	273

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
781	S745	4155	149	833	S693	3375	149	885	S641	2595	149
782	S744	4140	273	834	S692	3360	273	886	S640	2580	273
783	S743	4125	149	835	S691	3345	149	887	S639	2565	149
784	S742	4110	273	836	S690	3330	273	888	S638	2550	273
785	S741	4095	149	837	S689	3315	149	889	S637	2535	149
786	S740	4080	273	838	S688	3300	273	890	S636	2520	273
787	S739	4065	149	839	S687	3285	149	891	S635	2505	149
788	S738	4050	273	840	S686	3270	273	892	S634	2490	273
789	S737	4035	149	841	S685	3255	149	893	S633	2475	149
790	S736	4020	273	842	S684	3240	273	894	S632	2460	273
791	S735	4005	149	843	S683	3225	149	895	S631	2445	149
792	S734	3990	273	844	S682	3210	273	896	S630	2430	273
793	S733	3975	149	845	S681	3195	149	897	S629	2415	149
794	S732	3960	273	846	S680	3180	273	898	S628	2400	273
795	S731	3945	149	847	S679	3165	149	899	S627	2385	149
796	S730	3930	273	848	S678	3150	273	900	S626	2370	273
797	S729	3915	149	849	S677	3135	149	901	S625	2355	149
798	S728	3900	273	850	S676	3120	273	902	S624	2340	273
799	S727	3885	149	851	S675	3105	149	903	S623	2325	149
800	S726	3870	273	852	S674	3090	273	904	S622	2310	273
801	S725	3855	149	853	S673	3075	149	905	S621	2295	149
802	S724	3840	273	854	S672	3060	273	906	S620	2280	273
803	S723	3825	149	855	S671	3045	149	907	S619	2265	149
804	S722	3810	273	856	S670	3030	273	908	S618	2250	273
805	S721	3795	149	857	S669	3015	149	909	S617	2235	149
806	S720	3780	273	858	S668	3000	273	910	S616	2220	273
807	S719	3765	149	859	S667	2985	149	911	S615	2205	149
808	S718	3750	273	860	S666	2970	273	912	S614	2190	273
809	S717	3735	149	861	S665	2955	149	913	S613	2175	149
810	S716	3720	273	862	S664	2940	273	914	S612	2160	273
811	S715	3705	149	863	S663	2925	149	915	S611	2145	149
812	S714	3690	273	864	S662	2910	273	916	S610	2130	273
813	S713	3675	149	865	S661	2895	149	917	S609	2115	149
814	S712	3660	273	866	S660	2880	273	918	S608	2100	273
815	S711	3645	149	867	S659	2865	149	919	S607	2085	149
816	S710	3630	273	868	S658	2850	273	920	S606	2070	273
817	S709	3615	149	869	S657	2835	149	921	S605	2055	149
818	S708	3600	273	870	S656	2820	273	922	S604	2040	273
819	S707	3585	149	871	S655	2805	149	923	S603	2025	149
820	S706	3570	273	872	S654	2790	273	924	S602	2010	273
821	S705	3555	149	873	S653	2775	149	925	S601	1995	149
822	S704	3540	273	874	S652	2760	273	926	S600	1980	273
823	S703	3525	149	875	S651	2745	149	927	S599	1965	149
824	S702	3510	273	876	S650	2730	273	928	S598	1950	273
825	S701	3495	149	877	S649	2715	149	929	S597	1935	149
826	S700	3480	273	878	S648	2700	273	930	S596	1920	273
827	S699	3465	149	879	S647	2685	149	931	S595	1905	149
828	S698	3450	273	880	S646	2670	273	932	S594	1890	273
829	S697	3435	149	881	S645	2655	149	933	S593	1875	149
830	S696	3420	273	882	S644	2640	273	934	S592	1860	273
831	S695	3405	149	883	S643	2625	149	935	S591	1845	149
832	S694	3390	273	884	S642	2610	273	936	S590	1830	273

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
937	S589	1815	149	989	S537	1035	149	1041	S485	255	149
938	S588	1800	273	990	S536	1020	273	1042	S484	240	273
939	S587	1785	149	991	S535	1005	149	1043	S483	225	149
940	S586	1770	273	992	S534	990	273	1044	S482	210	273
941	S585	1755	149	993	S533	975	149	1045	S481	195	149
942	S584	1740	273	994	S532	960	273	1046	S480	180	273
943	S583	1725	149	995	S531	945	149	1047	DUMMY	165	149
944	S582	1710	273	996	S530	930	273	1048	DUMMY	150	273
945	S581	1695	149	997	S529	915	149	1049	DUMMY	-150	273
946	S580	1680	273	998	S528	900	273	1050	DUMMY	-165	149
947	S579	1665	149	999	S527	885	149	1051	S479	-180	273
948	S578	1650	273	1000	S526	870	273	1052	S478	-195	149
949	S577	1635	149	1001	S525	855	149	1053	S477	-210	273
950	S576	1620	273	1002	S524	840	273	1054	S476	-225	149
951	S575	1605	149	1003	S523	825	149	1055	S475	-240	273
952	S574	1590	273	1004	S522	810	273	1056	S474	-255	149
953	S573	1575	149	1005	S521	795	149	1057	S473	-270	273
954	S572	1560	273	1006	S520	780	273	1058	S472	-285	149
955	S571	1545	149	1007	S519	765	149	1059	S471	-300	273
956	S570	1530	273	1008	S518	750	273	1060	S470	-315	149
957	S569	1515	149	1009	S517	735	149	1061	S469	-330	273
958	S568	1500	273	1010	S516	720	273	1062	S468	-345	149
959	S567	1485	149	1011	S515	705	149	1063	S467	-360	273
960	S566	1470	273	1012	S514	690	273	1064	S466	-375	149
961	S565	1455	149	1013	S513	675	149	1065	S465	-390	273
962	S564	1440	273	1014	S512	660	273	1066	S464	-405	149
963	S563	1425	149	1015	S511	645	149	1067	S463	-420	273
964	S562	1410	273	1016	S510	630	273	1068	S462	-435	149
965	S561	1395	149	1017	S509	615	149	1069	S461	-450	273
966	S560	1380	273	1018	S508	600	273	1070	S460	-465	149
967	S559	1365	149	1019	S507	585	149	1071	S459	-480	273
968	S558	1350	273	1020	S506	570	273	1072	S458	-495	149
969	S557	1335	149	1021	S505	555	149	1073	S457	-510	273
970	S556	1320	273	1022	S504	540	273	1074	S456	-525	149
971	S555	1305	149	1023	S503	525	149	1075	S455	-540	273
972	S554	1290	273	1024	S502	510	273	1076	S454	-555	149
973	S553	1275	149	1025	S501	495	149	1077	S453	-570	273
974	S552	1260	273	1026	S500	480	273	1078	S452	-585	149
975	S551	1245	149	1027	S499	465	149	1079	S451	-600	273
976	S550	1230	273	1028	S498	450	273	1080	S450	-615	149
977	S549	1215	149	1029	S497	435	149	1081	S449	-630	273
978	S548	1200	273	1030	S496	420	273	1082	S448	-645	149
979	S547	1185	149	1031	S495	405	149	1083	S447	-660	273
980	S546	1170	273	1032	S494	390	273	1084	S446	-675	149
981	S545	1155	149	1033	S493	375	149	1085	S445	-690	273
982	S544	1140	273	1034	S492	360	273	1086	S444	-705	149
983	S543	1125	149	1035	S491	345	149	1087	S443	-720	273
984	S542	1110	273	1036	S490	330	273	1088	S442	-735	149
985	S541	1095	149	1037	S489	315	149	1089	S441	-750	273
986	S540	1080	273	1038	S488	300	273	1090	S440	-765	149
987	S539	1065	149	1039	S487	285	149	1091	S439	-780	273
988	S538	1050	273	1040	S486	270	273	1092	S438	-795	149

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1093	S437	-810	273	1145	S385	-1590	273	1197	S333	-2370	273
1094	S436	-825	149	1146	S384	-1605	149	1198	S332	-2385	149
1095	S435	-840	273	1147	S383	-1620	273	1199	S331	-2400	273
1096	S434	-855	149	1148	S382	-1635	149	1200	S330	-2415	149
1097	S433	-870	273	1149	S381	-1650	273	1201	S329	-2430	273
1098	S432	-885	149	1150	S380	-1665	149	1202	S328	-2445	149
1099	S431	-900	273	1151	S379	-1680	273	1203	S327	-2460	273
1100	S430	-915	149	1152	S378	-1695	149	1204	S326	-2475	149
1101	S429	-930	273	1153	S377	-1710	273	1205	S325	-2490	273
1102	S428	-945	149	1154	S376	-1725	149	1206	S324	-2505	149
1103	S427	-960	273	1155	S375	-1740	273	1207	S323	-2520	273
1104	S426	-975	149	1156	S374	-1755	149	1208	S322	-2535	149
1105	S425	-990	273	1157	S373	-1770	273	1209	S321	-2550	273
1106	S424	-1005	149	1158	S372	-1785	149	1210	S320	-2565	149
1107	S423	-1020	273	1159	S371	-1800	273	1211	S319	-2580	273
1108	S422	-1035	149	1160	S370	-1815	149	1212	S318	-2595	149
1109	S421	-1050	273	1161	S369	-1830	273	1213	S317	-2610	273
1110	S420	-1065	149	1162	S368	-1845	149	1214	S316	-2625	149
1111	S419	-1080	273	1163	S367	-1860	273	1215	S315	-2640	273
1112	S418	-1095	149	1164	S366	-1875	149	1216	S314	-2655	149
1113	S417	-1110	273	1165	S365	-1890	273	1217	S313	-2670	273
1114	S416	-1125	149	1166	S364	-1905	149	1218	S312	-2685	149
1115	S415	-1140	273	1167	S363	-1920	273	1219	S311	-2700	273
1116	S414	-1155	149	1168	S362	-1935	149	1220	S310	-2715	149
1117	S413	-1170	273	1169	S361	-1950	273	1221	S309	-2730	273
1118	S412	-1185	149	1170	S360	-1965	149	1222	S308	-2745	149
1119	S411	-1200	273	1171	S359	-1980	273	1223	S307	-2760	273
1120	S410	-1215	149	1172	S358	-1995	149	1224	S306	-2775	149
1121	S409	-1230	273	1173	S357	-2010	273	1225	S305	-2790	273
1122	S408	-1245	149	1174	S356	-2025	149	1226	S304	-2805	149
1123	S407	-1260	273	1175	S355	-2040	273	1227	S303	-2820	273
1124	S406	-1275	149	1176	S354	-2055	149	1228	S302	-2835	149
1125	S405	-1290	273	1177	S353	-2070	273	1229	S301	-2850	273
1126	S404	-1305	149	1178	S352	-2085	149	1230	S300	-2865	149
1127	S403	-1320	273	1179	S351	-2100	273	1231	S299	-2880	273
1128	S402	-1335	149	1180	S350	-2115	149	1232	S298	-2895	149
1129	S401	-1350	273	1181	S349	-2130	273	1233	S297	-2910	273
1130	S400	-1365	149	1182	S348	-2145	149	1234	S296	-2925	149
1131	S399	-1380	273	1183	S347	-2160	273	1235	S295	-2940	273
1132	S398	-1395	149	1184	S346	-2175	149	1236	S294	-2955	149
1133	S397	-1410	273	1185	S345	-2190	273	1237	S293	-2970	273
1134	S396	-1425	149	1186	S344	-2205	149	1238	S292	-2985	149
1135	S395	-1440	273	1187	S343	-2220	273	1239	S291	-3000	273
1136	S394	-1455	149	1188	S342	-2235	149	1240	S290	-3015	149
1137	S393	-1470	273	1189	S341	-2250	273	1241	S289	-3030	273
1138	S392	-1485	149	1190	S340	-2265	149	1242	S288	-3045	149
1139	S391	-1500	273	1191	S339	-2280	273	1243	S287	-3060	273
1140	S390	-1515	149	1192	S338	-2295	149	1244	S286	-3075	149
1141	S389	-1530	273	1193	S337	-2310	273	1245	S285	-3090	273
1142	S388	-1545	149	1194	S336	-2325	149	1246	S284	-3105	149
1143	S387	-1560	273	1195	S335	-2340	273	1247	S283	-3120	273
1144	S386	-1575	149	1196	S334	-2355	149	1248	S282	-3135	149

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1249	S281	-3150	273	1301	S229	-3930	273	1353	S177	-4710	273
1250	S280	-3165	149	1302	S228	-3945	149	1354	S176	-4725	149
1251	S279	-3180	273	1303	S227	-3960	273	1355	S175	-4740	273
1252	S278	-3195	149	1304	S226	-3975	149	1356	S174	-4755	149
1253	S277	-3210	273	1305	S225	-3990	273	1357	S173	-4770	273
1254	S276	-3225	149	1306	S224	-4005	149	1358	S172	-4785	149
1255	S275	-3240	273	1307	S223	-4020	273	1359	S171	-4800	273
1256	S274	-3255	149	1308	S222	-4035	149	1360	S170	-4815	149
1257	S273	-3270	273	1309	S221	-4050	273	1361	S169	-4830	273
1258	S272	-3285	149	1310	S220	-4065	149	1362	S168	-4845	149
1259	S271	-3300	273	1311	S219	-4080	273	1363	S167	-4860	273
1260	S270	-3315	149	1312	S218	-4095	149	1364	S166	-4875	149
1261	S269	-3330	273	1313	S217	-4110	273	1365	S165	-4890	273
1262	S268	-3345	149	1314	S216	-4125	149	1366	S164	-4905	149
1263	S267	-3360	273	1315	S215	-4140	273	1367	S163	-4920	273
1264	S266	-3375	149	1316	S214	-4155	149	1368	S162	-4935	149
1265	S265	-3390	273	1317	S213	-4170	273	1369	S161	-4950	273
1266	S264	-3405	149	1318	S212	-4185	149	1370	S160	-4965	149
1267	S263	-3420	273	1319	S211	-4200	273	1371	S159	-4980	273
1268	S262	-3435	149	1320	S210	-4215	149	1372	S158	-4995	149
1269	S261	-3450	273	1321	S209	-4230	273	1373	S157	-5010	273
1270	S260	-3465	149	1322	S208	-4245	149	1374	S156	-5025	149
1271	S259	-3480	273	1323	S207	-4260	273	1375	S155	-5040	273
1272	S258	-3495	149	1324	S206	-4275	149	1376	S154	-5055	149
1273	S257	-3510	273	1325	S205	-4290	273	1377	S153	-5070	273
1274	S256	-3525	149	1326	S204	-4305	149	1378	S152	-5085	149
1275	S255	-3540	273	1327	S203	-4320	273	1379	S151	-5100	273
1276	S254	-3555	149	1328	S202	-4335	149	1380	S150	-5115	149
1277	S253	-3570	273	1329	S201	-4350	273	1381	S149	-5130	273
1278	S252	-3585	149	1330	S200	-4365	149	1382	S148	-5145	149
1279	S251	-3600	273	1331	S199	-4380	273	1383	S147	-5160	273
1280	S250	-3615	149	1332	S198	-4395	149	1384	S146	-5175	149
1281	S249	-3630	273	1333	S197	-4410	273	1385	S145	-5190	273
1282	S248	-3645	149	1334	S196	-4425	149	1386	S144	-5205	149
1283	S247	-3660	273	1335	S195	-4440	273	1387	S143	-5220	273
1284	S246	-3675	149	1336	S194	-4455	149	1388	S142	-5235	149
1285	S245	-3690	273	1337	S193	-4470	273	1389	S141	-5250	273
1286	S244	-3705	149	1338	S192	-4485	149	1390	S140	-5265	149
1287	S243	-3720	273	1339	S191	-4500	273	1391	S139	-5280	273
1288	S242	-3735	149	1340	S190	-4515	149	1392	S138	-5295	149
1289	S241	-3750	273	1341	S189	-4530	273	1393	S137	-5310	273
1290	S240	-3765	149	1342	S188	-4545	149	1394	S136	-5325	149
1291	S239	-3780	273	1343	S187	-4560	273	1395	S135	-5340	273
1292	S238	-3795	149	1344	S186	-4575	149	1396	S134	-5355	149
1293	S237	-3810	273	1345	S185	-4590	273	1397	S133	-5370	273
1294	S236	-3825	149	1346	S184	-4605	149	1398	S132	-5385	149
1295	S235	-3840	273	1347	S183	-4620	273	1399	S131	-5400	273
1296	S234	-3855	149	1348	S182	-4635	149	1400	S130	-5415	149
1297	S233	-3870	273	1349	S181	-4650	273	1401	S129	-5430	273
1298	S232	-3885	149	1350	S180	-4665	149	1402	S128	-5445	149
1299	S231	-3900	273	1351	S179	-4680	273	1403	S127	-5460	273
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1406	S124	-5505	149	1458	S72	-6285	149	1510	S20	-7065	149
1407	S123	-5520	273	1459	S71	-6300	273	1511	S19	-7080	273
1408	S122	-5535	149	1460	S70	-6315	149	1512	S18	-7095	149
1409	S121	-5550	273	1461	S69	-6330	273	1513	S17	-7110	273
1410	S120	-5565	149	1462	S68	-6345	149	1514	S16	-7125	149
1411	S119	-5580	273	1463	S67	-6360	273	1515	S15	-7140	273
1412	S118	-5595	149	1464	S66	-6375	149	1516	S14	-7155	149
1413	S117	-5610	273	1465	S65	-6390	273	1517	S13	-7170	273
1414	S116	-5625	149	1466	S64	-6405	149	1518	S12	-7185	149
1415	S115	-5640	273	1467	S63	-6420	273	1519	S11	-7200	273
1416	S114	-5655	149	1468	S62	-6435	149	1520	S10	-7215	149
1417	S113	-5670	273	1469	S61	-6450	273	1521	S9	-7230	273
1418	S112	-5685	149	1470	S60	-6465	149	1522	S8	-7245	149
1419	S111	-5700	273	1471	S59	-6480	273	1523	S7	-7260	273
1420	S110	-5715	149	1472	S58	-6495	149	1524	S6	-7275	149
1421	S109	-5730	273	1473	S57	-6510	273	1525	S5	-7290	273
1422	S108	-5745	149	1474	S56	-6525	149	1526	S4	-7305	149
1423	S107	-5760	273	1475	S55	-6540	273	1527	S3	-7320	273
1424	S106	-5775	149	1476	S54	-6555	149	1528	S2	-7335	149
1425	S105	-5790	273	1477	S53	-6570	273	1529	S1	-7350	273
1426	S104	-5805	149	1478	S52	-6585	149	1530	S0	-7365	149
1427	S103	-5820	273	1479	S51	-6600	273	1531	VCOM	-7380	273
1428	S102	-5835	149	1480	S50	-6615	149	1532	VCOM	-7395	149
1429	S101	-5850	273	1481	S49	-6630	273	1533	VCOM	-7560	273
1430	S100	-5865	149	1482	S48	-6645	149	1534	VCOM	-7575	149
1431	S99	-5880	273	1483	S47	-6660	273	1535	G479	-7590	273
1432	S98	-5895	149	1484	S46	-6675	149	1536	G477	-7605	149
1433	S97	-5910	273	1485	S45	-6690	273	1537	G475	-7620	273
1434	S96	-5925	149	1486	S44	-6705	149	1538	G473	-7635	149
1435	S95	-5940	273	1487	S43	-6720	273	1539	G471	-7650	273
1436	S94	-5955	149	1488	S42	-6735	149	1540	G469	-7665	149
1437	S93	-5970	273	1489	S41	-6750	273	1541	G467	-7680	273
1438	S92	-5985	149	1490	S40	-6765	149	1542	G465	-7695	149
1439	S91	-6000	273	1491	S39	-6780	273	1543	G463	-7710	273
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1441	S89	-6030	273	1493	S37	-6810	273	1545	G459	-7740	273
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1443	S87	-6060	273	1495	S35	-6840	273	1547	G455	-7770	273
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1447	S83	-6120	273	1499	S31	-6900	273	1551	G447	-7830	273
1448	S82	-6135	149	1500	S30	-6915	149	1552	G445	-7845	149
1449	S81	-6150	273	1501	S29	-6930	273	1553	G443	-7860	273
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1451	S79	-6180	273	1503	S27	-6960	273	1555	G439	-7890	273
1452	S78	-6195	149	1504	S26	-6975	149	1556	G437	-7905	149
1453	S77	-6210	273	1505	S25	-6990	273	1557	G435	-7920	273
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1456	S74	-6255	149	1508	S22	-7035	149	1560	G429	-7965	149

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1562	G425	-7995	149	1614	G321	-8775	149	1666	G217	-9555	149
1563	G423	-8010	273	1615	G319	-8790	273	1667	G215	-9570	273
1564	G421	-8025	149	1616	G317	-8805	149	1668	G213	-9585	149
1565	G419	-8040	273	1617	G315	-8820	273	1669	G211	-9600	273
1566	G417	-8055	149	1618	G313	-8835	149	1670	G209	-9615	149
1567	G415	-8070	273	1619	G311	-8850	273	1671	G207	-9630	273
1568	G413	-8085	149	1620	G309	-8865	149	1672	G205	-9645	149
1569	G411	-8100	273	1621	G307	-8880	273	1673	G203	-9660	273
1570	G409	-8115	149	1622	G305	-8895	149	1674	G201	-9675	149
1571	G407	-8130	273	1623	G303	-8910	273	1675	G199	-9690	273
1572	G405	-8145	149	1624	G301	-8925	149	1676	G197	-9705	149
1573	G403	-8160	273	1625	G299	-8940	273	1677	G195	-9720	273
1574	G401	-8175	149	1626	G297	-8955	149	1678	G193	-9735	149
1575	G399	-8190	273	1627	G295	-8970	273	1679	G191	-9750	273
1576	G397	-8205	149	1628	G293	-8985	149	1680	G189	-9765	149
1577	G395	-8220	273	1629	G291	-9000	273	1681	G187	-9780	273
1578	G393	-8235	149	1630	G289	-9015	149	1682	G185	-9795	149
1579	G391	-8250	273	1631	G287	-9030	273	1683	G183	-9810	273
1580	G389	-8265	149	1632	G285	-9045	149	1684	G181	-9825	149
1581	G387	-8280	273	1633	G283	-9060	273	1685	G179	-9840	273
1582	G385	-8295	149	1634	G281	-9075	149	1686	G177	-9855	149
1583	G383	-8310	273	1635	G279	-9090	273	1687	G175	-9870	273
1584	G381	-8325	149	1636	G277	-9105	149	1688	G173	-9885	149
1585	G379	-8340	273	1637	G275	-9120	273	1689	G171	-9900	273
1586	G377	-8355	149	1638	G273	-9135	149	1690	G169	-9915	149
1587	G375	-8370	273	1639	G271	-9150	273	1691	G167	-9930	273
1588	G373	-8385	149	1640	G269	-9165	149	1692	G165	-9945	149
1589	G371	-8400	273	1641	G267	-9180	273	1693	G163	-9960	273
1590	G369	-8415	149	1642	G265	-9195	149	1694	G161	-9975	149
1591	G367	-8430	273	1643	G263	-9210	273	1695	G159	-9990	273
1592	G365	-8445	149	1644	G261	-9225	149	1696	G157	-10005	149
1593	G363	-8460	273	1645	G259	-9240	273	1697	G155	-10020	273
1594	G361	-8475	149	1646	G257	-9255	149	1698	G153	-10035	149
1595	G359	-8490	273	1647	G255	-9270	273	1699	G151	-10050	273
1596	G357	-8505	149	1648	G253	-9285	149	1700	G149	-10065	149
1597	G355	-8520	273	1649	G251	-9300	273	1701	G147	-10080	273
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1599	G351	-8550	273	1651	G247	-9330	273	1703	G143	-10110	273
1600	G349	-8565	149	1652	G245	-9345	149	1704	G141	-10125	149
1601	G347	-8580	273	1653	G243	-9360	273	1705	G139	-10140	273
1602	G345	-8595	149	1654	G241	-9375	149	1706	G137	-10155	149
1603	G343	-8610	273	1655	G239	-9390	273	1707	G135	-10170	273
1604	G341	-8625	149	1656	G237	-9405	149	1708	G133	-10185	149
1605	G339	-8640	273	1657	G235	-9420	273	1709	G131	-10200	273
1606	G337	-8655	149	1658	G233	-9435	149	1710	G129	-10215	149
1607	G335	-8670	273	1659	G231	-9450	273	1711	G127	-10230	273
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1609	G331	-8700	273	1661	G227	-9480	273	1713	G123	-10260	273
1610	G329	-8715	149	1662	G225	-9495	149	1714	G121	-10275	149
1611	G327	-8730	273	1663	G223	-9510	273	1715	G119	-10290	273
1612	G325	-8745	149	1664	G221	-9525	149	1716	G117	-10305	149

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
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1718	G113	-10335	149	1770	G9	-11115	149				
1719	G111	-10350	273	1771	G7	-11130	273				
1720	G109	-10365	149	1772	G5	-11145	149				
1721	G107	-10380	273	1773	G3	-11160	273				
1722	G105	-10395	149	1774	G1	-11175	149				
1723	G103	-10410	273	1775	VCOM	-11190	273				
1724	G101	-10425	149	1776	VCOM	-11205	149				
1725	G99	-10440	273		ALK_L	-11300	-285.5				
1726	G97	-10455	149		ALK_R	11300	-285.5				
1727	G95	-10470	273								
1728	G93	-10485	149								
1729	G91	-10500	273								
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1742	G65	-10695	149								
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1766	G17	-11055	149								
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1768	G13	-11085	149								

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