HDMI-to-eDP Converter w/ scaler

1 Features

Embedded-DisplayPort (eDP) Output

1/2/**4-lane** eDP @ 1.62/2.7Gbps per lane
HD to WQXGA **(2560*1600)** supported
Up to 6dB pre-emphasis

HDMI Input

HDMI 1.4a supported
RGB444/YCbCr444/YCbCr422 supported
Pixel clock up to 340MHz
2-channel audio supported
Support Hot-Plug Detect
Adaptive equalization

Reference Clock

Any freq. between 19MHz and 100MHz
Crystal or single-ended clock input
Built-in 5000ppm SSC generator

Misc

I²C for chip configuration
Built-in eDP handshake protocol
I²C-AUX channel for TCON/DPCD/EDID control
Built-in video test pattern

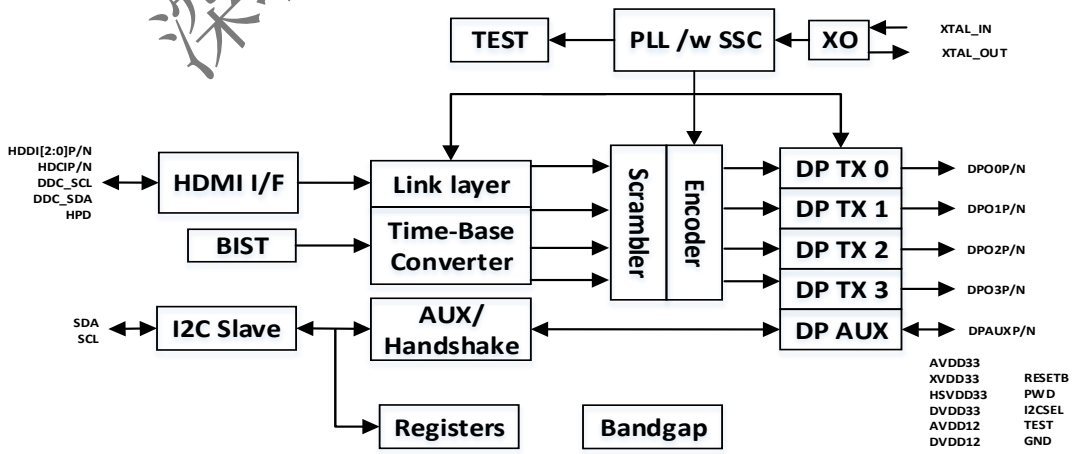
Power

1.2V core supply
2.5V or 3.3V IO supply
Power consumption ~ **150mW**
@ 2560*1600*24bit*60Hz
Deep-sleep mode power <1mW

Package

QFN-56 (7mm x 7mm) package
RoHS Compliant
Sample available now

2 Block Diagram



3 General Description

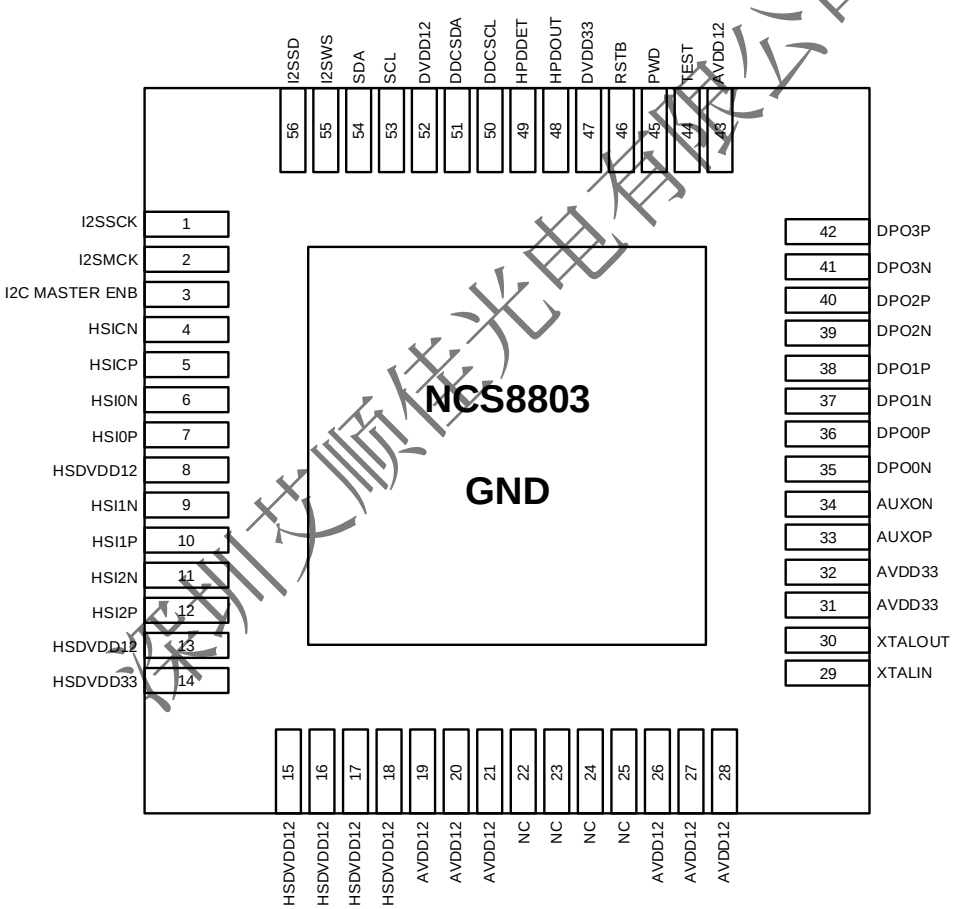
NCS8803 is a low-power HDMI-to-DisplayPort/eDP converter with advanced scaling function, fractional scaling ratio from 2:1 to 1:2, which is designed for mobile devices including tablets, laptops, monitor, etc. to support high-definition DP/eDP displays.

NCS8803 supports 4-lane DP/eDP output which is typically required to support WQXGA (2560*1600) and above at 60Hz frame rate.

Thanks to our proprietary scaling algorithm, NCS8803 provides high picture quality. All the functions pack into a small 7mm*7mmQFN56 package which saves the precious space in mobile devices.

4 Pin Diagram

(**Top View**)



5 Pin Description

No.	Pin Name	Description
1	I2SSCK	I²S serial clock
2	I2SMCK	I²S serial multiplying clock
3	I2C MASTER ENB	I²C master enable, active low
4	HSICN	HDMI clock channel negative
5	HSICP	HDMI clock channel positive
6,7	HSI0N,P	HDMI data channel 0
8,13,15~18	HSDVDD12	1.2V power supply for high-speed analog
9,10	HSI1N,P	HDMI data channel 1
11,12	HSI2N,P	HDMI data channel 2
14	HSDVDD33	3.3V power supply for high-speed analog
19~21,26~28	AVDD12	1.2V power supply for analog
22~25	NC	Not connected
29	XTALIN	Crystal or clock input
30	XTALOUT	Crystal
31	XVDD33	2.5/3.3V power supply for crystal oscillator
32	AVDD33	2.5/3.3V power supply for analog
33	AUXOP	eDP AUX channel negative
34	AUXON	eDP AUX channel positive
35	DPO0N	eDP data channel 0 negative
36	DPO0P	eDP data channel 0 positive
37,38	DPO1N,P	eDP data channel 1
39,40	DPO2N,P	eDP data channel 2
41,42	DPO3N,P	eDP data channel 3
43	AVDD12	1.2V power supply for analog
44	TEST	Not connected
45	PWD	Power down, active high
46	RSTB	Reset, active low
47	DVDD33	2.5/3.3V power supply for digital IOs
48	HPDOUT	Hot-Plug Detect output
49	HPDDET	Hot-Plug Detect input
50	DDCSCL	DDC clock
51	DDCSDA	DDC data
52	DVDD12	1.2V power supply for digital
53	SCL	I²C clock
54	SDA	I²C data
55	I2SWS	I²S left/right clock
56	I2SSD	I²S serial data
Thermal	GND	Ground

6 Electrical Specifications

6.1 Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD33	2.5/3.3V power supply for analog	2.38	3.3	3.46	V
DVDD33	2.5/3.3V power supply for digital	2.38	3.3	3.46	V
XVDD33	2.5/3.3V power supply for crystal oscillator	2.38	3.3	3.46	V
HSVDD33	2.5/3.3V power supply for RGB mode	1.71	3.3	3.46	V
	2.5/3.3V power supply for LVDS mode	2.38	3.3	3.46	V
AVDD12	1.2V power supply for analog	1.14	1.2	1.26	V
DVDD12	1.2V power supply for digital core	1.14	1.2	1.26	V
$f_{CLK-XTAL}$	crystal or single-ended clock input freq.	19	24	100	MHz
Temp	Ambient temperature	-20	25	85	℃
ESD	HBM			4	kV
	CDM			500	V
	MM			200	V

6.2 Power Consumption

Mode	Power		
	VDD33	VDD12	Power
2048*1536 @ 60Hz	5mA	110mA	148.5mW[1]
Deep-sleep	-	0.24mA	0.29mW

Note: 1. VDD33=2.5V, VDD12=1.2V, LVDS input, 4-lane*1.6Gbps eDP output, TX diff p-p voltage 200mV.

6.3 eDP Main Channel Electrical Specification

Symbol	Description	Min	Typ	Max	Units
UI_HBR	Unit interval for high bit rate(2.7 Gbps/ lane)		370		ps
UI_LBR	Unit interval for low bit rate(1.62 Gbps/ lane)		617		ps
Down-spread amp.	Link clock down spreading	0		5000	ppm
Down-spread freq.	Link clock down spreading frequency	30		33	kHz
V_{TXpp}	Differential peak-to-peak	0.1	0.6	1.2	V
T_{TX-EYE}	TX eDP output minimum eye width	0.726			UI
	No pre-emphasis		0		dB
	3.5 dB pre-emphasis Level		3.5		dB
	6.0 dB pre-emphasis Level		6		dB
$V_{TX-DC-CM}$	TX DC common mode voltage	0		1.2	V
C_{TX}	AC coupling capacitor	75	100	200	nF

6.4 eDP AUX channel Electrical Specifications

Symbol	Description	Min	Typ	Max	Units

UI	AUX unit interval	0.4	0.5	0.6	us
Pre-charge pulses	Number of pre-charge pulses	10		16	
$T_{AUX-BUS-PARK}$	AUX CH bus park time	10			ns
$V_{AUX-DIFFpp}$	AUX peak-to-peak voltage	0.4		1.2	V
$V_{AUX-DC-CM}$	AUX DC common mode voltage	0		1.2	V
C_{AUX}	AUX AC coupling capacitor	75	100	200	nF

6.5 HDMI Electrical Specification

Symbol	Description	Min	Typ	Max	Units
$Rate_{HDMI}$	HDMI data rate per pair			3000	Mbps
$f_{CLK-HDMI}$	HDMI input TMDS clock frequency			300	MHz
$V_{TH-HDMI}$	Differential input high threshold			0.1	V
$V_{TL-HDMI}$	Differential input low threshold	-0.1			V
C_{RX}	AC coupling capacitor	75	100	200	nF
T_{jitter}	HDMI input TMDS clock jitter			0.3	T_{bit}
$T_{skew-intra-pair}$	Skew between differential pair, TMDS clock below 222.75MHz			0.4	T_{bit}
$T_{skew-intra-pair}$	Skew between differential pair, TMDS clock above 222.75MHz			$0.15T_{bit}$+ 112ps	-
$T_{skew-inter-pair}$	Skew between differential channel			$0.2T_{character}$+ 1.78ns	-

7 Register Table

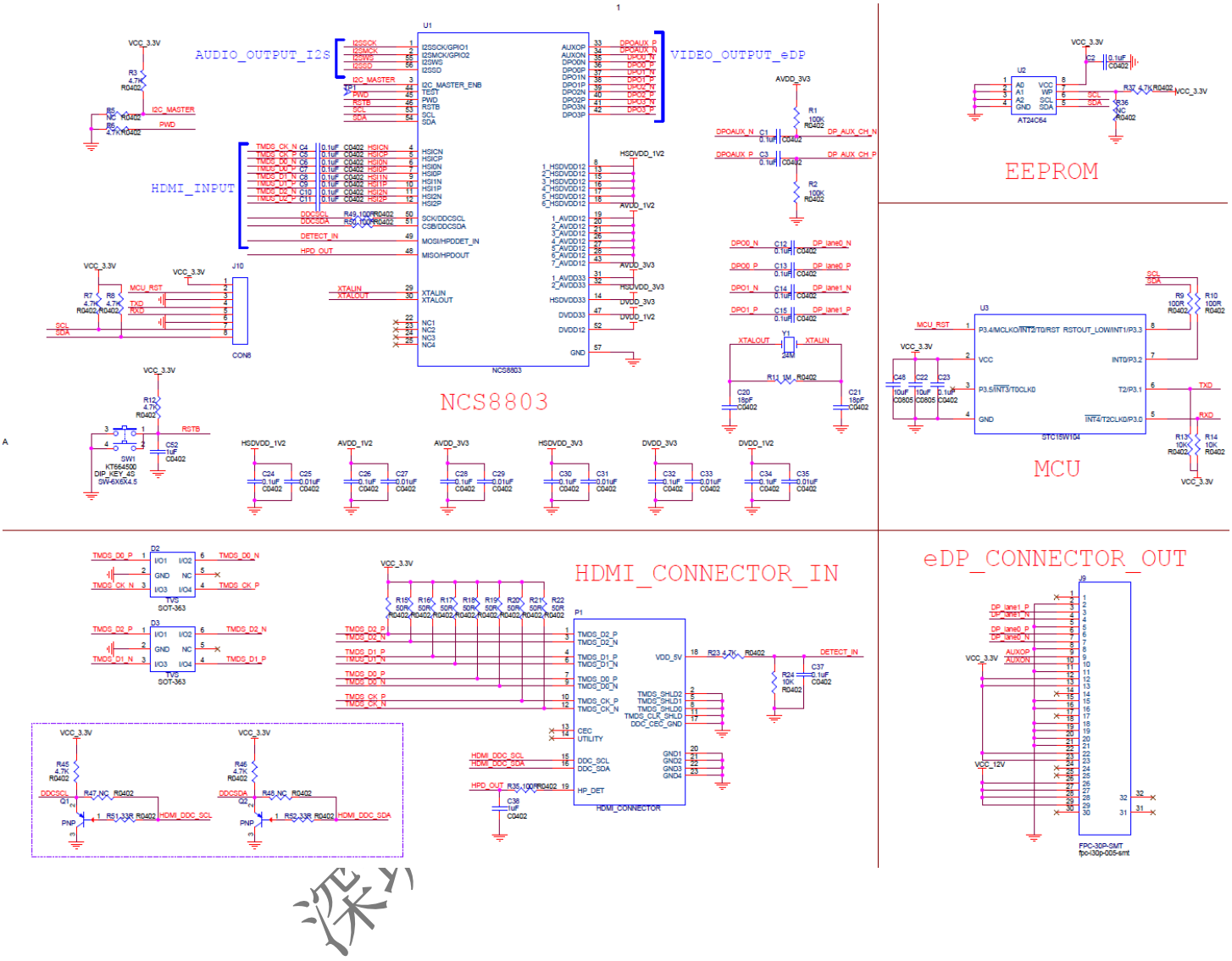
Device ID=0x70			
Addr.	R/W	Description	Default (HEX)
0x00	R/W	Bit[2:0] 000: LVDS 2-channel input 001: LVDS 1-channel input 100: RGB input	0x00
0x02	R/W	Bit0: 0: Hi-Fi scaler bypass enable 1: Hi-Fi scaler bypass disable Bit1: 0: RX panel parameter adaptive enable 1: TX panel parameter adaptive enable	0x00
0x03	R/W	Bit[1:0] LVDS a/b channel swap 00: a->a, b->b 11: a->b, b->a Bit2: LVDS mode 0: VESA mode 1: JEDIA mode Bit3: LVDS polarity 0: normal 1: polarity swap	0x00
0x07	R/W	Bit[2:0] eDP TX lane mode 001: 1 lane 010: 2 lane 100: 4 lane Bit4: data rate 0: HBR 1: RBR Bit5: pixel bit width 0: 24bit 1: 18bit Bit6: hardware training 0: disable 1: enable Bit7: data pattern 0: eDP TX data disable 1: eDP TX data enable	0x14
0x0B	R/W	Bit0: BIST enable 0: bist disable 1: bist enable Bit[7:4] bist pattern	0x00
0x0C	R/W	R component in BIST mode	0xFF
0x0D	R/W	G component in BIST mode	0xFF
0x0E	R/W	B component in BIST mode	0xFF
0x0F	R/W	Bit0: internal logic reset 0: reset enable 1: reset disable	0x01
0x10	R/W	Input Htotal (Hsync + HBP + Hactive + HFP) upper-byte	0x08
0x11	R/W	Input Htotal (Hsync + HBP + Hactive + HFP) lower-byte	0xA0
0x12	R/W	Input Hstart (Hsync + HBP) upper-byte	0x00
0x13	R/W	Input Hstart (Hsync + HBP) lower-byte	0x0A

0x14	R/W	Input Hactive (Hactive) upper-byte	0x08
0x15	R/W	Input Hactive (Hactive) lower-byte	0x00
0x16	R/W	Input Vtotal (Vsync + VBP + Vactive + VFP) upper-byte	0x06
0x17	R/W	Input Vtotal (Vsync + VBP + Vactive + VFP) lower-byte	0x0D
0x18	R/W	Input Vstart (Vsync + VBP) upper-byte	0x00
0x19	R/W	Input Vstart (Vsync + VBP) lower-byte	0x0A
0x1A	R/W	Input Vactive upper-byte	0x06
0x1B	R/W	Input Vactive lower-byte	0x00
0x1C	R/W	Input Hsync polarity control MSB: H_polarity 0: Hsync active high, 1: Hsync active low	0x80
0x1D	R/W	Input Hsync width (Hsync)	0x05
0x1E	R/W	Input Vsync polarity control MSB: V_polarity 0: Vsync active high, 1: Vsync active low	0x80
0x1F	R/W	Output Vsync width (Vsync)	0x01
0x20	R/W	Output Htotal (Hsync + HBP + Hactive + HFP) upper-byte	0x08
0x21	R/W	Output Htotal (Hsync + HBP + Hactive + HFP) lower-byte	0xA0
0x22	R/W	Output Hstart (Hsync + HBP) upper-byte	0x00
0x23	R/W	Output Hstart (Hsync + HBP) lower-byte	0x0A
0x24	R/W	Output Hactive (Hactive) upper-byte	0x08
0x25	R/W	Output Hactive (Hactive) lower-byte	0x00
0x26	R/W	Output Vtotal (Vsync + VBP + Vactive + VFP) upper-byte	0x06
0x27	R/W	Output Vtotal (Vsync + VBP + Vactive + VFP) lower-byte	0x0D
0x28	R/W	Output Vstart (Vsync + VBP) upper-byte	0x00
0x29	R/W	Output Vstart (Vsync + VBP) lower-byte	0x0A
0x2A	R/W	Output Vactive upper-byte	0x06
0x2B	R/W	Output Vactive lower-byte	0x00
0x2C	R/W	Output Hsync polarity control MSB: H_polarity 0: Hsync active high, 1: Hsync active low	0x80
0x2D	R/W	Output Hsync width (Hsync)	0x05
0x2E	R/W	Input Vsync polarity control MSB: V_polarity 0: Vsync active high, 1: Vsync active low	0x80
0x2F	R/W	Output Vsync width (Vsync)	0x01
0xc1	R/W	Output P/N swap control Bit0: lane0 P/N swap Bit1: lane1 P/N swap Bit2: lane2 P/N swap Bit3: lane3 P/N swap	0x00
0x80	RO	Bit[1:0] eDP training result 00: handshake is not valid 01: handshake is fail 10: handshake is successful	
0x81	RO	Bit 0 = LANE0_CR_DONE Bit 1 = LANE0_CHANNEL_EQ_DONE Bit 2 = LANE0_SYMBOL_LOCKED Bit 3 = RESERVED. Read 0. Bit 4 = LANE1_CR_DONE Bit 5 = LANE1_CHANNEL_EQ_DONE Bit 6 = LANE1_SYMBOL_LOCKED Bit 7 = RESERVED. Read 0.	

0x82	RO	Bit 0 = LANE2_CR_DONE Bit 1 = LANE2_CHANNEL_EQ_DONE Bit 2 = LANE2_SYMBOL_LOCKED Bit 3 = RESERVED. Read 0. Bit 4 = LANE3_CR_DONE Bit 5 = LANE3_CHANNEL_EQ_DONE Bit 6 = LANE3_SYMBOL_LOCKED Bit 7 = RESERVED. Read 0.	
Device ID=0x75			
Addr.	R/W	Description	Default (HEX)
0x00	R/W	Bit7: eDP lane speed 0: RBR (1.6Gbps) 1: HBR (2.7Gbps) Bit0: internal analog reset 0: reset enable 1: reset disable	0xB1
0x05	R/W	Bit0: reserved Bit6: eDP lane speed 0: RBR (1.62Gbps) 1: HBR (2.7Gbps)	0xC1
0x0E	R/W	TX amplitude	0x08
0x0F	R/W	TX amplitude	0x05
0x11	R/W	TX termination	0x00
0x13	R/W	TX lane enable Bit0: 1: lane0 enable Bit1: 1: lane1 enable Bit2: 1: lane2 enable Bit3: 1: lane3 enable	0x0F
0x2D	R/W	Bit[3:0] 0000: HDMI disable 1111: HDMI enable	0xDF
0x84	R/W	TX lane swap control Bit[1:0]: lane0 swap control 00: lane0->lane0 01: lane0->lane1 10: lane0->lane2 11: lane0->lane3 Bit[5:4]: lane1 swap control 00: lane1->lane0 01: lane1->lane1 10: lane1->lane2 11: lane1->lane3	0x10
0x85	R/W	TX lane swap control Bit[1:0]: lane2 swap control 00: lane2->lane0 01: lane2->lane1 10: lane2->lane2 11: lane2->lane3 Bit[5:4]: lane3 swap control 00: lane3->lane0 01: lane3->lane1 10: lane3->lane2 11: lane3->lane3	0x32

8 Applications

8.1 Typical Application Schematics



8.2 PCB Layout Rules

a. Due to the high data rate of the eDP signal, characteristic impedance throughout the signal path needs to be well controlled. It is highly suggested to control the differential characteristic impedance of the PCB trace to be within 100ohm±10%. Low speed connectors are highly suggested to be avoided in the eDP signal path, especially in the 2.7Gbps mode.

b. The requirement on the LVDS side is less stringent but impedance discontinuities including Y-branching are highly suggested to be minimized.

c. The crosstalk and length of the RGB traces needs to be minimized.

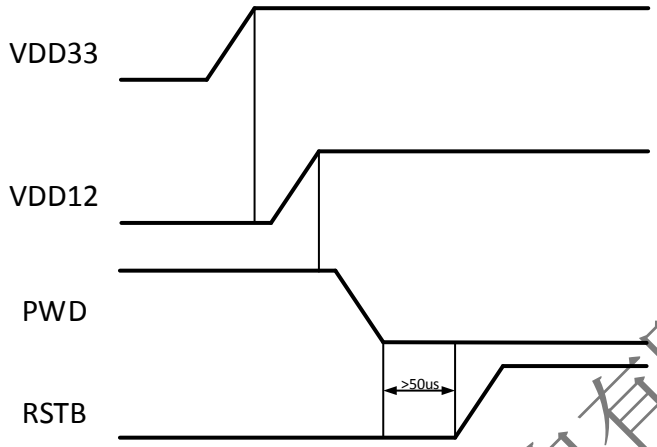
d. The intra-pair mismatch in all differential pairs needs to be avoided.

e. eDP inter-lane skew is suggested to be controlled under 50mil.

f. LVDS inter-lane skew is suggested to be controlled under 100mil.

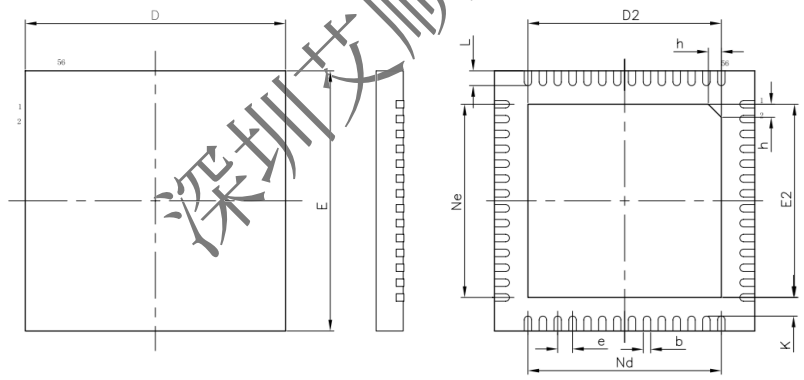
g. RGB inter-line skew is suggested to be controlled under 300mil.

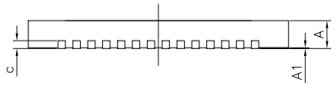
8.3 Power-on Sequence



9 Package

NCS8803 is packaged in 7mm*7mm 56-pin QFN, QFN56L (0707*0.75-0.40). The package dimensions are shown below. (Unit: mm)





SYMBOL	MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	—	0.05
b	0.15	0.25
c	0.18	0.25
D	6.90	7.10
D2	5.10	5.30
e	0.40BSC	
Nd	5.20BSC	
Ne	5.20BSC	
E	6.90	7.10
E2	5.10	5.30
K	0.20	—
L	0.35	0.45
h	0.30	0.40

10 Revision History

Rev. #	Date	Author	Comments
0.92	12/15/2016	Xin Zhang	First beta release
0.93	02/20/2017	Chenxi Liu	Update typical application schematics

This document contains information on a new product. Specifications and information herein are subject to change without notice.