DATA SHEET

NVIDIA Jetson TX2 NX System-on-Module

Pascal GPU + ARMv8 CPU + 4GB LPDDR4 + 16GB eMMC 5.1

AI Performance

Up to 1.33 TFLOPS

Pascal GPU

256 NVIDIA® CUDA® cores

End-to-end lossless compression | Tile Caching | OpenGL® 4.6 | OpenGL ES 3.2 | Vulkan™ 1.1◊ | CUDA | Maximum Operating Frequency: 1.3 GHz

Denver 2 CPU and Cortex A57

ARMv8 (64-bit) heterogeneous multi-processing (HMP) CPU architecture | Two CPU clusters (six processor cores) connected by a high-performance coherent interconnect fabric.

NVIDIA Denver 2 (Dual-Core) Processor: L1 Cache: 128KB L1 instruction cache (I-cache) per core; 64KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB

ARM® Cortex® A57 MPCore (Quad-Core) Processor: L1 Cache: 48KB L1 instruction cache (I-cache) per core; 32KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB | Cortex-A57 maximum frequency: 2 GHz

Audio

Industry-standard High-Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI interface | 4 x I2S | I and Q baseband data channels | PDM in/out

Memory

4GB | 128-bit LPDDR4 DRAM | Secure External Memory Access Using TrustZone® Technology | System MMU | Maximum Operating Frequency: 1600 MHz | Maximum Memory BW 51.2GB/s

Storage

16GB eMMC 5.1 Flash Storage | Bus Width: 8-bit | Maximum Bus Frequency: 200 MHz (HS400)

Networking

10/100/1000 BASE-T

CSI Camera

12 lanes (3x4 or 5x2) | MIPI CSI-2 D-PHY 1.2 (2.5Gb/s per lane, total up to 30Gbps)

Display Controller

Two multi-mode eDP 1.4 | DP 1.2a | HDMI 2.0a/b | 1 x2 DSI (1.5Gbps/lane)

Maximum Resolution (eDP/DP/HDMI): (up to) 3840x2160 at 60 Hz (up to 36 bpp)

Multi-Stream HD Video and JPEG

Video Decode 2x 4K60 | Video Encode 1x 4K60

Peripheral Interfaces

xHCI host controller with integrated PHY (up to) 1x USB 3.0 (Gen1), 3x USB 2.0 | PCIe 1 x2 + 1 x1 (Gen2), Root Port Only | SD/MMC controller (supporting eMMC 5.1, SD 4.0, SDHOST 4.0 and SDIO 3.0) | 3x UART | 2x SPI | 4x I^2C | 1x CAN | 4x I^2S | GPIOs | 1x SD Card/SDIO

Mechanical

Module Size: 69.6 mm x 45 mm | 260 pin edge Connector

Operating Requirements

Temperature (T_J)*: -25°C ~90°C (typical) | Supported Power 15W | Power Input: 5V

Note: Refer to the Software Features section of the latest L4T Development Guide for a list of supported features; all features may not be available.

◊ Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.

* See the *Jetson TX2 NX Thermal Design Guide* for details

Revision History

Version	Date	Description
v1.0	February 23, 2021	Initial release
v1.1	April 24, 2021	Added Environmental and Mechanical Screening section and moved Reliability Report to this section. Updated Reliability Report: added Random Vibration – 5G Non-Op
v1.2	October 27, 2021	Updates to Table 20: Power and System Control Pin Descriptions and Table 21: PMIC_BBAT Pin Descriptions.
v1.3	November 29, 2021	Removed Realtek reference
v1.4	March 18, 2022	Removed diagrams from Power Sequence section

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1.0 Functional Overview

The NVIDIA® Jetson TX2 NX series module can be used in a wide variety of applications requiring varying performance metrics. To accommodate these varying conditions, frequencies and voltages are actively managed by power and thermal management software and influenced by workload.

1.1 Pascal GPU

NVIDIA introduced major improvements to performance and power efficiency with the new Pascal GPU architecture. The Jetson TX2 NX series module incorporates these same GPU architectural enhancements to further increase performance and reduce power consumption for computationally intensive workloads. The previous (Maxwell) GPU architecture introduced an all-new design for the Streaming Multiprocessor (SM); the Pascal GPU architecture continues to improve upon this SM design with the following enhancements:

- Simplified data path
- New SM scheduler architecture
- Improvements in scheduling and overlapped load/store instructions
- New arithmetic operations
- Improved support for large address spaces and page faulting capability

The Graphics Processing Cluster (GPC) is a dedicated hardware block for compute, rasterization, shading, and texturing; most of the GPU's core graphics functions are performed inside the GPC. It is comprised of multiple SM units and a Raster Engine. The SM unit creates, manages, schedules, and executes instructions from many threads in parallel. Raster operators (ROPs) continue to be aligned with L2 cache slices and memory controllers. The SM geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces and complex gaming applications; the power efficiency of the Pascal GPU enables this performance on devices with power-limited environments.

Each SM is partitioned into four separate processing blocks (referred to as SMPs), each SMP contains its own instruction buffer, scheduler and 32 CUDA cores. Inside each SMP, CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output.

Features:

- End-to-end lossless compression
- Tile Caching
- Support for OpenGL 4.6, OpenGL ES 3.2, Vulkan 1.0
- Adaptive Scalable Texture Compression (ASTC) LDR profile supported
- DirectX 12 support
- CUDA support
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power of 2D and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute instancing

- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

1.2 CPU Complex

The CPU complex is comprised of two CPU clusters (six processor cores total) in a coherent multi-processor configuration – MCPU cluster: Denver 2 (Dual-Core) Processor; BCPU cluster: ARM Cortex-A57 MPCore (Quad-Core) Processor. Both the Denver 2 and Cortex-A57 CPU clusters support ARMv8 executing both 64-bit Aarch64 code and 32-bit Aarch32 code, including legacy ARMv7 applications.

The two CPU clusters are connected by a high-performance coherent interconnect fabric designed by NVIDIA; this enables simultaneous operation of both CPU clusters (all six cores if required) for a true heterogeneous multi-processing (HMP) environment. The coherency mechanism allows tasks to be freely migrated, according to their performance needs, between the CPU cores with no overhead for manual cache flushing. The Denver 2 processor delivers significantly higher single-thread performance; achieved with dynamic code optimizations from NVIDIA that result in considerably more out-of-order operations and associated outstanding memory reads. The Cortex-A57 is better suited for multi-threaded applications and lighter loads.

Both CPU clusters interface to the MSelect FIFO via an AXI interface to decouple I/O traffic. MSelect allows an AXI master device to send traffic to the peripheral buses based on transaction address. The AXI/Xbar bridge enables early response on write transfers and full hardware hazard resolution to permit the maximum transaction throughput to MMIO.

1.2.1 NVIDIA Denver 2 (Dual-Core) Processor

Both cores in the Denver 2 processor are identical implementations of the ARMv8 architecture with NVIDIA optimizations. Each core includes 128KB Instruction (I-cache) and 64KB Data (D-cache) Level 1 caches. A 2MB L2 cache is shared by both cores. Denver 2 processor features include:

- Full implementation of the ARMv8 architecture
- NVIDIA Dynamic Code Optimization
- 7-wide Superscalar architecture
- Dynamic branch prediction with a Branch Target Buffer and Global History Buffer RAMs, a return stack buffer, and an indirect predictor.
- 128-entry 4-way-associative L1 instruction TLB with native support for 4KB page sizes.
- 256-entry 8-way-associative L1 data TLB with native support for 4KB, and 64KB pages sizes.
- 2048-entry 8-way set-associative accelerator TLB cache in each processor
- 128KB 4-way-associative parity protected L1 instruction cache
- 64KB 4-way-associative parity protected L1 data cache
- 2MB 16-way-associative ECC protected L2 cache shared by both Denver cores
- Embedded Trace Microcell (ETM) based on the ETMv4 architecture
- Performance Monitor Unit (PMU) based on the PMUv3 architecture
- Cross Trigger Interface (CTI) for multiprocessor debugging
- Cryptographic Engine for crypto function support
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains

1.2.2 ARM Cortex-A57 MPCore (Quad-Core) Processor

All four cores in the ARM Cortex-A57 are identical implementations of the ARMv8 architecture. Each core includes 48KB Instruction (I-cache) and 32KB Data (D-cache) Level 1 caches. A 2MB L2 cache is shared by all cores. Cortex-A57 processor features include:

- Full implementation of the ARMv8 architecture
- Superscalar, variable-length, out-of-order pipeline
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer RAMs, a return stack, and an indirect predictor
- 48-entry fully associative L1 instruction TLB with native support for 4KB, 64KB, and 1MB page sizes.
- 32-entry fully associative L1 data TLB with native support for 4KB, 64KB and 1MB pages sizes.
- 4-way set-associative unified 1024-entry Level 2 (L2) TLB in each processor
- Fixed 48KB parity protected L1 instruction cache and 32KB ECC protected L1 data cache
- A 2MB ECC protected L2 cache shared by all the Cortex-A57 cores
- Embedded Trace Microcell (ETM) based on the ETMv4 architecture
- Performance Monitor Unit (PMU) based on the PMUv3 architecture
- Cross Trigger Interface (CTI) for multiprocessor debugging
- Cryptographic Engine for crypto function support
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains
- Cortex-A57 Revision r1p3

1.3 Memory Controller

The Memory Controller (MC) maximizes memory utilization while providing minimum latency access for critical CPU requests. An arbiter is used to prioritize requests, optimizing memory access efficiency and utilization, and minimizing system power consumption. The MC provides access to main memory for all internal devices. It provides an abstract view of memory to its clients via standardized interfaces, allowing the clients to ignore details of the memory hierarchy. It optimizes access to shared memory resources, balancing latency, and efficiency to provide best system performance, based on programmable parameters. Structurally, the memory subsystem (MSS) consists of four major components:

- MSS backbone: routes requests from clients to the MC Hub and responses from MC Hub to the clients.
- MC Hub: receives client requests, performs SMMU translation, performs various security checks, and sends requests to the four MC Channels.
- MC Channels: row sorter/arbiter and DRAM controller.
- DRAMIO: channel-to-pad fabric, DRAM I/O pads, and PLLs.

Features:

- 128-bit memory interface supporting: LPDDR4 up to 3200 MT/s for Jetson TX2 NX; delivering a peak bandwidth up to 51.2GB/s for Jetson TX2 NX; implemented as four 32-bit channels with x16 sub-partitions
- Integrated ARM SMMU v2 (SMMU-500) IP with two stage translation to support virtualization
- Enhanced arbiter design for higher memory efficiency
- Support for encryption of traffic to/from DRAM to comply with SCSA security requirements
- 40-bit virtual addressing
- Generalized security apertures

- Variable transaction sizes based on the requests from the clients (e.g., one 64-byte transaction with variable dimensions, two 32-byte transactions with variable dimensions, etc.)
- Encryption
    - Uses AES-XTS with 128-bit key
    - Encrypts carveout regions (Microcode, TrustZone®, GSC, VPR)
- Dual CKE signals for dynamic power down per device
- Support for two DRAM ranks of unequal device densities
- Dynamic Entry/Exit from Self -Refresh and Power Down states

The MC can sustain high utilization over a very diverse mix of requests. For example, the MC is prioritized for bandwidth (BW) over latency for all multimedia blocks (the multimedia blocks have been architected to prefetch and pipeline their operations to increase latency tolerance); this enables the MC to optimize performance by coalescing, reordering, and grouping requests to minimize memory power. DRAM also has modes for saving power when it is either not being used, or during periods of specific types of use.

1.4 Video Input Interfaces

NVCSI is the host for the fourth-generation camera solution (NVCSI 1.0, VI 4.0, and ISP 4.0). It is based on the MIPI CSI-2 v1.3 protocol stack; supports D-PHY v1.2; and is paired with the 4th generation NVIDIA video input (VI) unit. The NVCSI combination host enables three 4-lane, five 2-lane, or five 1-lane configurations. Each lane can support up to four virtual channels and supports data type interleaving.

Features:

- Virtual Channel Interleaving
- Data Type Interleaving
- Parallel pixel processing for higher throughput and lower clock speeds

1.4.1 MIPI Camera Serial Interface (CSI)

Standard
MIPI CSI 2.0 Receiver specification
MIPI D-PHY® v1.2 Physical Layer specification

The Jetson TX2 NX series module supports three MIPI CSI x4 bricks allowing for a variety of device types and camera configurations. Data aggregated from physical lanes enters an asynchronous FIFO which interfaces to the NVCSI block. Each data channel has peak bandwidth of up to 2.5 Gbps.

Features:

- Up to three quad lane stereo cameras or five dual lane camera streams
- Supported per-brick camera configurations: 1x 4 lanes, 2x 2 lanes, 2x 1 lane, 1x 1 lane, 1x 2 lanes, 1x 1 lane + 1x 2 lanes
- Supports single-shot mode
- Supported input data formats:
    - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
    - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b
    - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
    - DPCM (predictor 1): 14-10-14, 14-8-14, 12-8-12, 12-7-12, 12-6-12, 10-8-10, 10-7-10, 10-6-10

- Embedded control information
- MIPI D-PHY Modes of Operation
    - High Speed Mode – High speed differential signaling up to 2.5Gbps; burst transmission for low power
    - Low Power Control – Single-ended 1.2V CMOS level. Low speed signaling for handshaking.
    - Low Power Escape – Low speed signaling for data, used for escape command entry only.

Table 1: CSI Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
10	CSI0_CLK_N	Camera, CSI 0 Clock–	Input	MIPI D-PHY
12	CSI0_CLK_P	Camera, CSI 0 Clock+	Input	MIPI D-PHY
4	CSI0_D0_N	Camera, CSI 0 Data 0–	Input	MIPI D-PHY
6	CSI0_D0_P	Camera, CSI 0 Data 0+	Input	MIPI D-PHY
16	CSI0_D1_N	Camera, CSI 0 Data 1–	Input	MIPI D-PHY
18	CSI0_D1_P	Camera, CSI 0 Data 1+	Input	MIPI D-PHY
9	CSI1_CLK_N	Camera, CSI 1 Clock–	Input	MIPI D-PHY
11	CSI1_CLK_P	Camera, CSI 1 Clock+	Input	MIPI D-PHY
3	CSI1_D0_N	Camera, CSI 1 Data 0–	Input	MIPI D-PHY
5	CSI1_D0_P	Camera, CSI 1 Data 0+	Input	MIPI D-PHY
15	CSI1_D1_N	Camera, CSI 1 Data 1–	Input	MIPI D-PHY
17	CSI1_D1_P	Camera, CSI 1 Data 1+	Input	MIPI D-PHY
28	CSI2_CLK_N	Camera, CSI 2 Clock–	Input	MIPI D-PHY
30	CSI2_CLK_P	Camera, CSI 2 Clock+	Input	MIPI D-PHY
22	CSI2_D0_N	Camera, CSI 2 Data 0–	Input	MIPI D-PHY
24	CSI2_D0_P	Camera, CSI 2 Data 0+	Input	MIPI D-PHY
34	CSI2_D1_N	Camera, CSI 2 Data 1–	Input	MIPI D-PHY
36	CSI2_D1_P	Camera, CSI 2 Data 1+	Input	MIPI D-PHY
27	CSI3_CLK_N	Camera, CSI 3 Clock–	Input	MIPI D-PHY
29	CSI3_CLK_P	Camera, CSI 3 Clock+	Input	MIPI D-PHY
21	CSI3_D0_N	Camera, CSI 3 Data 0–	Input	MIPI D-PHY
23	CSI3_D0_P	Camera, CSI 3 Data 0+	Input	MIPI D-PHY
33	CSI3_D1_N	Camera, CSI 3 Data 1–	Input	MIPI D-PHY
35	CSI3_D1_P	Camera, CSI 3 Data 1+	Input	MIPI D-PHY
52	CSI4_CLK_N	Camera, CSI 4 Clock–	Input	MIPI D-PHY
54	CSI4_CLK_P	Camera, CSI 4 Clock+	Input	MIPI D-PHY
46	CSI4_D0_N	Camera, CSI 4 Data 0–	Input	MIPI D-PHY
48	CSI4_D0_P	Camera, CSI 4 Data 0+	Input	MIPI D-PHY
58	CSI4_D1_N	Camera, CSI 4 Data 1–	Input	MIPI D-PHY
60	CSI4_D1_P	Camera, CSI 4 Data 1+	Input	MIPI D-PHY

Pin #	Signal Name	Description	Direction	Pin Type
40	CSI4_D2_N	Camera, CSI 4 Data 2–	Input	MIPI D-PHY
42	CSI4_D2_P	Camera, CSI 4 Data 2+	Input	MIPI D-PHY
64	CSI4_D3_N	Camera, CSI 4 Data 3–	Input	MIPI D-PHY
66	CSI4_D3_P	Camera, CSI 4 Data 3+	Input	MIPI D-PHY

Table 2: Camera Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
213	CAM_I2C_SCL	Camera I^2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	Camera I^2C Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
116	CAM0_MCLK	Camera 0 Reference Clock	Output	CMOS – 1.8V
114	CAM0_PWDN	Camera 0 Powerdown or GPIO	Output	CMOS – 1.8V
122	CAM1_MCLK	Camera 1 Reference Clock	Output	CMOS – 1.8V
120	CAM1_PWDN	Camera 1 Powerdown or GPIO	Output	CMOS – 1.8V

1.4.2 Video Input (VI)

The VI block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor execution resources. The VI block provides formatting for RGB, YCbCr, and raw Bayer data in support of several camera user models. These models include single and multi-camera systems, which may have up to six active streams. The input streams are obtained from MIPI compliant CMOS sensor camera modules.

1.4.3 Image Signal Processor (ISP)

The ISP takes data from the VI or CSI block in raw Bayer format and processes it to YUV output. Advanced image processing is used to convert input to YUV data, and remove artifacts introduced by high-megapixel CMOS sensors, camera lens and color-space conversion.

Features:

- CSI Virtual Channel (VC) supports four VCs per CSI x4 brick
- SMMU ID support for guest OS virtualization
- Local Tone Map
- Bayer Histogram statistics for auto-exposure
- Bayer average map for auto white balance and auto-exposure
- Sharpness map for auto focus

1.5 Display Controller

The display controller complex contains two Serial Output Resources (SOR) which collects pixels from the output of a display pipeline, format/encode them to desired format and then streams to various output devices. The SOR consists of several individual resources which can be used to interface with different display devices such as HDMI or DP. A SOR can drive only a single device at any given time. In addition to SORs, 1 x2 MIPI-DSI interface is available.

Features:

- 1/2/4 lane DP (DP 1.2a) and eDP (eDP 1.4)
- 1 x2 DSI
- HDMI 2.0a/b
    - Support 8/12 bpc RGB and YUV444
    - Support 8/10/12 bpc YUV422
- Up to 36bpp* pixel depth on HDMI and DP; up to 24bpp* on DSI and eDP.

Note: * (Resolution + Refresh Rate + Pixel Depth + Format) must be within specification limits to achieve support for desired pixel depth.

- ASSR scrambling for eDP panels
- On HDMI, multichannel audio from HDA controller, up to eight channels 192 kHz 24-bit.
- Support frame-packed 3D stereo mode (not frame-sequential mode like dGPU)
- Support generic info-frame transmission
- Support HDMI Vendor Specific Info-frame (VSI) packet transmission
- Supported eDP 1.4 features:
    - Additional link rates (2.16, 2.43, 3.24, 4.32 Gbps)
    - Enhanced framing
    - Power sequencing
    - Reduced main voltage swing

Table 3: DSI Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
76	DSI_CLK_N	DSI Clock–	Output	MIPI D-PHY
78	DSI_CLK_P	DSI Clock+	Output	MIPI D-PHY
70	DSI_D0_N	DSI Data 0–	Bidir	MIPI D-PHY
72	DSI_D0_P	DSI Data 0+	Bidir	MIPI D-PHY
82	DSI_D1_N	DSI Data 1–	Output	MIPI D-PHY
84	DSI_D1_P	DSI Data 1+	Output	MIPI D-PHY

1.6 High Definition (HD) Audio/Video Subsystem

The High-Definition Audio-Video Subsystem uses a collection of functional blocks to off-load audio and video processing activities from the CPU subsystem, resulting in fast, fully concurrent, highly efficient operation.

This Subsystem is comprised of the following:

- Multi-Standard Video Decoder
- Multi-Standard Video Encoder
- JPG Processing Block
- Video Image Compositor (VIC)
- Audio Processing Engine (APE)

1.6.1 HDMI and DisplayPort Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0a/b	Scrambling support Clock/4 support (1/40 bit-rate clock) HDMI 1.4 (up to 340 MHz pixel clock rate) HDMI 2.0 (up to 594 MHz pixel clock rate)
VESA DisplayPort Standard Version 1.4	

A standard DP 1.4 or High-Definition Multimedia Interface (HDMI) 2.0a/b interface is supported. These share the same set of interface pins, so either DisplayPort (DP) or HDMI can be supported natively. Each output collects the output of a display pipeline from the display controller, formats/encodes that output (to a desired format), and then streams it to an output device. Each output can provide an interface to an external device; each output can drive only a single output device at any given time. HDMI support provides a method of transferring both audio and video data; the SOR receives video from the display controller and audio from a separate high-definition audio (HDA) controller, it combines and transmits them as appropriate.

Note: A single CEC controller is shared between the two HDMI/DP interfaces. Both DP0 and DP1 support either DP or HDMI.

Features:

- DisplayPort
  - Multichannel audio from HDA controller, up to eight channels, 96 kHz, 24-bit
  - (up to) 540 MHz pixel clock rate (i.e., 1.62 GHz for RBR, 2.7 GHz for HBR, and 5.4 GHz for HBR2.
  - 8b/10b encoding support
  - External dual-mode standard support
  - Audio streaming support
- HDMI
  - (up to) 594 MHz pixel clock
    - 8/12 bpc RGB and YUV444
    - 8/10/12 bpc YUV422
    - 8 bpc YUV420 (10/12 bpc YUV frame buffers should be output as YUV422)
  - HDMI Vendor-Specific Info frame (VSI) packet transmission
  - On HDMI, multichannel audio from HDA controller, up to eight channels, 192 kHz, 24-bit.
  - Fuse calibration information for HDMI analog parameter(s)
  - 1080i output on HDMI
- DP or HDMI connectors via appropriate external level shifting
- HDCP 2.2 and 1.4 over either DP or HDMI
  Note: refer to NVIDIA software release notes for detailed specifications.
- Generic info frame transmission
- Frame-packed 3D stereo mode

Table 4: HDMI/DisplayPort/eDP Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
39	DP0_TXD0_N	DisplayPort 0 Lane 0 or HDMI Lane 2–	Output	DP/HDMI
41	DP0_TXD0_P	DisplayPort 0 Lane 0 or HDMI Lane 2+	Output	DP/HDMI

Pin #	Signal Name	Description	Direction	Pin Type
45	DP0_TXD1_N	DisplayPort 0 or HDMI Lane 1–	Output	DP/HDMI
47	DP0_TXD1_P	DisplayPort 0 or HDMI Lane 1+	Output	DP/HDMI
51	DP0_TXD2_N	DisplayPort 0 Lane 2– or HDMI Lane 0–	Output	DP/HDMI
53	DP0_TXD2_P	DisplayPort 0 Lane 2+ or HDMI Lane 0+	Output	DP/HDMI
57	DP0_TXD3_N	DisplayPort 0 Lane 3– or HDMI Clk Lane–	Output	DP/HDMI
59	DP0_TXD3_P	DisplayPort 0 Lane 3+ or HDMI Clk Lane+	Output	DP/HDMI
90	DP0_AUX_N	Display Port 0 Aux– or HDMI DDC SDA	Bidir	DP/HDMI
92	DP0_AUX_P	Display Port 0 Aux+ or HDMI DDC SCL	Bidir	DP/HDMI
88	DP0_HPD	Display Port 0 or HDMI Hot Plug Detect	Input	Open Drain – 1.8V
63	DP1_TXD0_N	DisplayPort 1 Lane 0 or HDMI Lane 2–	Output	DP/HDMI
65	DP1_TXD0_P	DisplayPort 1 Lane 0 or HDMI Lane 2+	Output	DP/HDMI
69	DP1_TXD1_N	DisplayPort 1 or HDMI Lane 1–	Output	DP/HDMI
71	DP1_TXD1_P	DisplayPort 1 or HDMI Lane 1+	Output	DP/HDMI
75	DP1_TXD2_N	DisplayPort 1 Lane 2– or HDMI Lane 0–	Output	DP/HDMI
77	DP1_TXD2_P	DisplayPort 1 Lane 2+ or HDMI Lane 0+	Output	DP/HDMI
81	DP1_TXD3_N	DisplayPort 1 Lane 3– or HDMI Clk Lane–	Output	DP/HDMI
83	DP1_TXD3_P	DisplayPort 1 Lane 3+ or HDMI Clk Lane+	Output	DP/HDMI
98	DP1_AUX_N	Display Port 1 Aux– or HDMI DDC SDA	Bidir	Open-Drain, 1.8V (3.3V tolerant - DDC)
100	DP1_AUX_P	Display Port 1 Aux+ or HDMI DDC SCL	Bidir	Open-Drain, 1.8V (3.3V tolerant – DDC)
96	DP1_HPD	Display Port 1 or HDMI Hot Plug Detect	Input	Open Drain – 1.8V
94	HDMI_CEC	HDMI CEC	Bidir	Open Drain – 3.3V

Note: (Resolution + Refresh Rate + Pixel Depth + Format) must be within specification limits to achieve support for desired pixel depth.

1.6.2 Embedded DisplayPort (eDP)

Standard
VESA Embedded DisplayPort Standard Version 1.4a

Embedded DisplayPort (eDP) is a mixed-signal interface consisting of four differential serial output lanes and one PLL. This PLL is used to generate a high-frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. eDP modes consist of 1.6 GHz for RBR; 2.16 GHz, 2.43 GHz, and 2.7 GHz for HBR; 3.24 GHz, 4.32 GHz, and 5.4 GHz for HBR2.

Note:	eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

The eDP block collects pixels from the output of the display pipeline, formats/encodes them to the eDP format, and then streams them to various output devices. It drives local panels only (does not support an external DP port), and it includes a small test pattern generator and CRC generator.

Features:

- 1/2/4/ lane, single link
- Additional link rates (2.16, 2.43, 3.24, 4.32 Gbps)
- Enhanced framing
- Power sequencing
- Reduced auxiliary timing
- Reduced main voltage swing
- Alternate Seed Scrambler Reset (ASSR) for internal eDP panels

1.7 High-Definition Audio-Video Subsystem

Standard
High-Definition Audio Specification Version 1.0a

The HD Audio-Video Subsystem uses a collection of functional blocks to off-load audio and video processing activities from the CPU complex, resulting in fast, fully concurrent, and highly efficient operation. This subsystem is comprised of the following:

- Multi-standard video decoder
- Multi-standard video encoder
- JPEG processing block
- Video Image Compositor (VIC)
- Audio Processing Engine (APE)

1.7.1 Multi-Standard Video Decoder

The video decoder accelerates video decode, supporting low resolution mobile content, Standard Definition (SD), High Definition (HD) and UltraHD (2160p, or “4k” video) profiles. The video decoder is designed to be extremely power efficient without sacrificing performance.

The video decoder communicates with the memory controller through the video DMA which supports a variety of memory format output options. For low power operations, the video decoder can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques.

- Control and assist hardware audio decoding blocks
- Control and synchronize the video decode processor (NVDEC)

The following video standards are supported:

- H.265: Main10, Main, Main444
- WEBM VP9 and VP8
- H.264: Baseline, Main, High, Stereo SEI (half-res)

- VC-1: Advanced
- MPEG-4: Simple
- H.263: Profile 0
- DiVX: 4/5/6
- XviD Home Theater
- MPEG-2: MP

Note:	A/V codec, post-processing and containers support are subject to software support: refer to NVIDIA software documentation for current support.

1.7.2 Multi-Standard Video Encoder

The multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high quality video encoding operations for mobile applications such as video recording and video conferencing. The encode processor is designed to be extremely power efficient without sacrificing performance.

The following video standards are supported:

- H.265 Main Profile: I-frames and P-frames (No B-frames)
- H.264 Baseline/Main/High Profiles: IDR/I/P/B-frame support
- MVC
- WEBM: VP8, VP9
- MPEG4 (ME only)
- MPEG2 (ME only)
- VC1 (ME only): No B frame, no interlaced

1.7.3 JPEG Processing Block

The JPEG processing block is responsible for JPEG (de)compression calculations (based on JPEG still image standard), image scaling, decoding (YUV420, YUV422H/V, YUV444, YUV400), and color space conversion (RGB to YUV; decode only).

Input (encode) formats:

- Pixel width: 8 bpc
- Subsample format: YUV420
- Resolution up to 16K x 16K
- Pixel pack format
    - Semi-planar/planar for 420

Output (decode) formats:

- Pixel width 8 bpc
- Resolution up to 16K x 16K
- Pixel pack format
    - Semi-planar/planar for YUV420
    - YUY2/planar for 422H/422V
    - Planar for YUV444
    - Interleave for RGBA

1.7.4 Video Image Compositor (VIC)

VIC implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending, and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features:

- Color Decompression
- High-quality Deinterlacing
- Inverse Teleciné
- Temporal Noise Reduction
    - High quality video playback
    - Reduces camera sensor noise
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation

1.7.5 High-Definition Audio (HDA)

Standard
Intel High-Definition Audio Specification Revision 1.0a

The Jetson TX2 NX implements an industry-standard High-Definition Audio (HDA) controller. This controller provides a multi-channel audio path to the HDMI interface. The HDA block also provides an HDA-compliant serial interface to an audio codec. Multiple input and output streams are supported.

Features:

- Supports HDMI 2.0 and DP1.4
- Support up to two audio streams for use with HDMI/DP
- Supports striping of audio out across 1,2,4[a] SDO lines
- Supports DVFS with maximum latency up to 208 µs for eight channels
- Supports two internal audio codecs
- Audio Format Support
    - Uncompressed Audio (LPCM): 16/20/24 bits at 32/44.1/48/88.2/96/176.4/192[b] kHz
    - Compressed Audio format: AC3, DTS5.1, MPEG1, MPEG2, MP3, DD+, MPEG2/4 AAC, TrueHD, DTS-HD

[a] Four SDO lines: cannot support one stream, 48 kHz, 16-bits, two channels; for this case, use a one or two SDO line configuration.
[b] DP protocol sample frequency limitation: cannot support >96 kHz, i.e., does not support 176.4 kHz and 196 kHz.

1.7.6 Audio Processing Engine (APE)

The Audio Processing Engine (APE) is a self-contained unit with dedicated audio clocking that enables Ultra Low Power (ULP) audio processing. Software based post processing effects enable the ability to implement custom audio algorithms.

Features:

- 96 KB Audio RAM
- Low latency voice processing
- Audio Hub (AHUB) I/O Modules
    - 4 x I^2S Stereo/TDM I/O
- Multi-Channel IN/OUT
    - Digital Audio Mixer: 10-in/5-out
        - Up to eight channels per stream
        - Simultaneous Multi-streams
        - Flexible stream routing
    - Parametric equalizer: up to 12 bands
    - Low latency sample rate conversion (SRC) and high-quality asynchronous sample rate conversion (ASRC)

1.7.7 Security Controller (TSEC)

TSEC heavy-secure (HS) hardware can authenticate its own code autonomously using its Secure Boot ROM and signature verification keys. The on-chip secure memory enables tamper resistant secure storage and transaction verification. TSEC implements a random number generator (RNG) and has a Falcon engine that supports AES-128b; no other cryptographic primitives or key sizes are supported. Two independent instruction queues (capable of holding up to 16 instructions) are used to provide encryption support for DRM schemes, including protected content encryption/ decryption.

Two instances of the TSEC controller (i.e., TSECA and TSECB) balance the performance requirements of increasingly demanding use cases.

Features:

- TSECA – performs GSC blob signing for NVDEC
- TSECA/B
    - Communicates with SE for any crypto acceleration, if required.
    - Side channel countermeasures for AES.
    - Dedicated video protection region in memory
        - Programmable in the memory controller
        - Extends security controller i-cache and d-cache
        - Only accessible by the Security Controller
        - Minimum size requirements avoid security exposure

1.8 Security Engine

A dedicated platform security engine supports secure boot, incorporates a NIST SP800-90 complaint random number generator (RNG) including built in ring oscillator-based entropy source used to seed a deterministic random bit generator (DRBG), and a protected memory aperture for video use cases.

Features:

- Side channel attack prevention
- Encryption of memory traffic
- RSA PKC 2048-bit CMAC based boot support
- Support for multiple security domains throughout the control plane and peripheral bridges

- AES-128/192/256 encryption and decryption support
- SHA-1, SHA-224, SHA-256, SHA-384, and SHA-512 support
- RSA: 512, 768, 1024, 1536, 2048, 3072, and 4096-bit support
- ECC: 160, 192, 224, 256, 384, 512, and 521-bit support

1.9 Interface Descriptions

The following sections outline the interfaces available on the Jetson TX2 NX module and details the module pins used to interact with and control each interface. See the *Jetson TX2 NX Product Design Guide* for complete functional descriptions, programming guidelines, and register listings for each of these blocks.

1.9.1 SD/eMMC

Standard	Notes
SD Specifications, Part A2, SD Host Controller Standard Specification, Version 4.1	
SD Specifications, Part 1, Physical Layer Specification, Version 4.2	
SD Specifications, Part 1, eSD (Embedded SD) Addendum, Version 2.10	
SD Specifications, Part E1, SDIO Specification Version, 4.1	Support for SD 4.0 Spec without UHS-II
JEDEC Standard, Embedded Multimedia Card (eMMC) Electrical Standard 5.1	JESD84-B51

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to an external SD card or SDIO device and provides the interface for the on module eMMC. It has a direct memory controller interface and is capable of initiating data transfers between system memory and an external card or device. It also has an AMBA Peripheral Bus (APB) slave interface to access its configuration registers. To access the on-system RAM for MicroBoot, the SD/MMC controller relies on the path to System RAM in the memory controller.

Features:

- 8-bit data interface to on-module eMMC
- 4-bit data interface for SD cards/SDIO
- Supports card interrupts for SD cards (1/4/8-bit SD modes) and SDIO devices
- Supports read wait control and suspend/resume operation for SD cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB

Table 5: SD/SDIO Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
229	SDMMC_CLK	SD Card or SDIO Clock	Output	CMOS – 1.8V/3.3V
227	SDMMC_CMD	SD Card or SDIO Command	Bidir	CMOS – 1.8V/3.3V
219	SDMMC_DAT0	SD Card or SDIO Data 0	Bidir	CMOS – 1.8V/3.3V
221	SDMMC_DAT1	SD Card or SDIO Data 1	Bidir	CMOS – 1.8V/3.3V
223	SDMMC_DAT2	SD Card or SDIO Data 2	Bidir	CMOS – 1.8V/3.3V
225	SDMMC_DAT3	SD Card or SDIO Data 3	Bidir	CMOS – 1.8V/3.3V

1.9.2 Universal Serial Bus (USB)

Standard	Notes
Universal Serial Bus Specification Revision 3.0	Refer to specification for related interface timing details.
Universal Serial Bus Specification Revision 2.0	USB Battery Charging Specification, version 1.2; including Data Contact Detect protocol Modes: Host and Device Speeds: Low, Full, and High
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	

An xHCI/Device controller (named XUSB) supports the xHCI programming model for scheduling transactions and interface managements as a host that natively supports USB 3.0, USB 2.0, and USB 1.1 transactions with its USB 3.0 and USB 2.0 interfaces. The XUSB controller supports USB 2.0 L1 and L2 (suspend) link power management and USB 3.0 U1, U2, and U3 (suspend) link power managements. The XUSB controller supports remote wakeup, wake on connect, wake on disconnect, and wake on overcurrent in all power states, including sleep mode.

1.9.2.1 USB 2.0 Operation

USB 2.0 ports operate in USB 2.0 High Speed mode (up to 480Mb/s) when connecting directly to a USB 2.0 peripheral and USB 1.1 Full and Low Speed modes (up to 12Mb/s) when connecting directly to a USB 1.1 peripheral. Supports software-initiated link power management.

Table 6: USB 2.0 Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
109	USB0_D_N	USB 2.0 Port 0 Data–	Bidir	USB PHY
111	USB0_D_P	USB 2.0 Port 0 Data+	Bidir	USB PHY
115	USB1_D_N	USB 2.0 Port 1 Data–	Bidir	USB PHY
117	USB1_D_P	USB 2.0 Port 1 Data+	Bidir	USB PHY
121	USB2_D_N	USB 2.0 Port 2 Data–	Bidir	USB PHY
123	USB2_D_P	USB 2.0 Port 2 Data+	Bidir	USB PHY

1.9.2.2 USB 3.0 Operation

USB 3.0 port only operates in USB 3.0 (Gen1) Super Speed mode (up to 5Gb/s). Supports hardware and software-initiated link power management.

Table 7: USB 3.0 Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
161	USBSS_RX_N	USB SS Receive– (USB 3.0 Ctrl #0)	Input	USB SS PHY
163	USBSS_RX_P	USB SS Receive+ (USB 3.0 Ctrl #0)	Input	USB SS PHY
166	USBSS_TX_N	USB SS Transmit– (USB 3.0 Ctrl #0)	Output	USB SS PHY
168	USBSS_TX_P	USB SS Transmit+ (USB 3.0 Ctrl #0)	Output	USB SS PHY

1.9.3 PCI Express (PCIe)

Standard	Notes
PCI Express Base Specification Revision 2.0	The Jetson TX2 NX series module meets the timing requirements for the Gen2 (5.0 GT/s) data rates. Refer to specification for complete interface timing details. Although NVIDIA validates that the module design complies with the PCIe specification, PCIe software support may be limited.

The Jetson TX2 NX series module integrates a x3 lane PCIe® bridge to enable a control path from the module to external PCIe devices with support for up to three lanes, and two separate interfaces. Both interfaces support upstream and downstream AXI that serves as the control path from the Jetson TX2 NX series module to the external PCIe device.

Features:

- Configurations and Link Speed
  - x2 lane configurations
    - Supports x2 and x1 configurations with conventional PCIe interface
    - Supports lane reversal and lane flipping for x2 and x1
    - Supports polarity inversion
    - Supports Gen1 and Gen2 link speed
    - Supports dynamic link speed and lane width change
  - x1 lane configurations
    - Supports polarity inversion
    - Supports Gen1 and Gen2 link speed for conventional PCIe
  - Possible configurations
  - 1 x2 + 1 x1
- Dedicated PEX_RST#, PEX_CLK and PEX_CLKREQ# signals for each PCIe interface
- One PEX_WAKE# signal
- PCIe Transactions
  - Supports 128-byte maximum payload size
  - Supports 64-bit address
  - Supports completion timeout with configurable timeout range
  - Does not support TLP prefixes or ECRC
  - Message Signaled Interrupts
    - Transaction ordering and coherency
    - Supports PCIe transaction ordering rules
    - Supports relaxed ordering
    - Supports No Snoop bit forwarding for upstream/DMA requests
    - Does not support ID-based ordering

Table 8: PCIe Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
131	PCIE0_RX0_N	PCIe #0 Receive 0– (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
133	PCIE0_RX0_P	PCIe #0 Receive 0+ (PCIe Ctrl #0 Lane 0)	Input	PCIe PHY
137	PCIE0_RX1_N	PCIe #0 Receive 1– (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
139	PCIE0_RX1_P	PCIe #0 Receive 1+ (PCIe Ctrl #0 Lane 1)	Input	PCIe PHY
134	PCIE0_TX0_N	PCIe #0 Transmit 0– (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
136	PCIE0_TX0_P	PCIe #0 Transmit 0+ (PCIe Ctrl #0 Lane 0)	Output	PCIe PHY
140	PCIE0_TX1_N	PCIe #0 Transmit 1– PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
142	PCIE0_TX1_P	PCIe #0 Transmit 1+ (PCIe Ctrl #0 Lane 1)	Output	PCIe PHY
181	PCIE0_RST*	PCIe #0 Reset (PCIe Ctrl #0). 4.7kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
180	PCIE0_CLKREQ*	PCIe #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
160	PCIE0_CLK_N	PCIe #0 Reference Clock–	Bidir	PCIe PHY
162	PCIE0_CLK_P	PCIe #0 Reference Clock+	Output	PCIe PHY
167	PCIE1_RX0_N	PCIe #1 Receive 0– (PCIe Ctrl #2 Lane 0)	Input	PCIe PHY.
169	PCIE1_RX0_P	PCIe #1 Receive 0+ (PCIe Ctrl #2 Lane 0)	Input	PCIe PHY
172	PCIE1_TX0_N	PCIe #1 Transmit 0– (PCIe Ctrl #2 Lane 0)	Output	PCIe PHY
174	PCIE1_TX0_P	PCIe #1 Transmit 0+ (PCIe Ctrl #2 Lane 0)	Output	PCIe PHY
183	PCIE1_RST*	PCIe #1 Reset (PCIe Ctrl #2). 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain – 3.3V
182	PCIE1_CLKREQ*	PCIe #1 Clock Request (PCIe Ctrl #2). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
173	PCIE1_CLK_N	PCIe #1 Reference Clock– (PCIe Ctrl #2)	Output	PCIe PHY
175	PCIE1_CLK_P	PCIe #1 Reference Clock+ (PCIe Ctrl #2)	Output	PCIe PHY
179	PCIE_WAKE*	PCIe Wake. 47kΩ pull-up to 3.3V on the module.	Input	Open Drain – 3.3V

See the *Jetson TX2 NX Product Design Guide* for supported PCIe configuration and connection examples.

1.9.4 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) controller allows a duplex, synchronous, serial communication between the controller and external peripheral devices; it supports both Master and Slave modes of operation on the SPI bus. See the *Jetson TX2 NX Product Design Guide* for more information.

Features:

- Independent Rx FIFO and Tx FIFO.
- Software controlled bit-length supports packet sizes of 1 to 32 bits.

- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size).
- SS_N can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries.
- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO).
- Simultaneous receive and transmit supported.

Table 9: SPI Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
91	SPI0_SCK	SPI 0 Clock	Bidir	CMOS – 1.8V
89	SPI0_MOSI	SPI 0 Master Out / Slave In	Bidir	CMOS – 1.8V
93	SPI0_MISO	SPI 0 Master In / Slave Out	Bidir	CMOS – 1.8V
95	SPI0_CS0*	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V
97	SPI0_CS1*	SPI 0 Chip Select 1	Bidir	CMOS – 1.8V
106	SPI1_SCK	SPI 1 Clock	Bidir	CMOS – 1.8V
104	SPI1_MOSI	SPI 1 Master Out / Slave In	Bidir	CMOS – 1.8V
108	SPI1_MISO	SPI 1 Master In / Slave Out	Bidir	CMOS – 1.8V
110	SPI1_CS0*	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V

Figure 1: SPI Master Timing Diagram

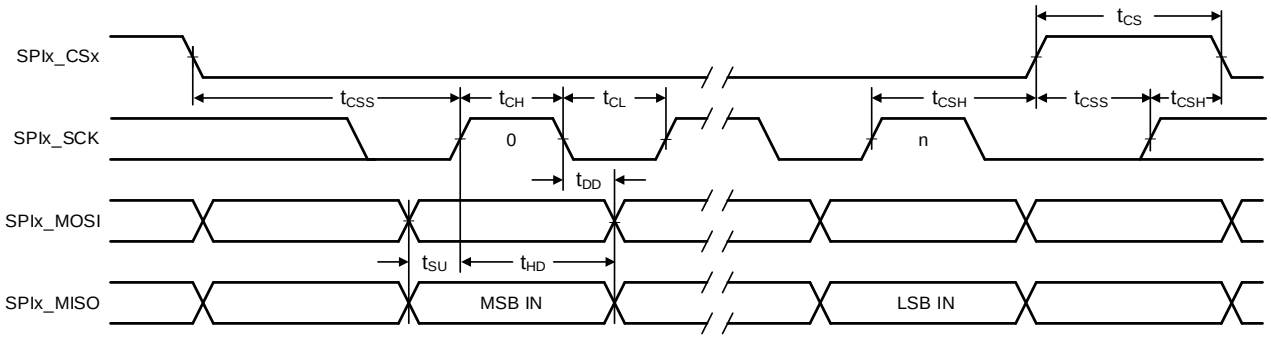


Table 10: SPI Master Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Fsck	SPIx_SCK clock frequency	–	65	MHz
Psck	SPIx_SCK period	1/Fsck	–	ns
t_{CH}	SPIx_SCK high time	50%Psck -10%	50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%	50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1	–	V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1	–	V/ns
t_{SU}	SPIx_MISO setup to SPIx_SCK rising edge	2	–	ns
t_{HD}	SPIx_MISO hold from SPIx_SCK rising edge	3	–	ns

Symbol	Parameter	Minimum	Maximum	Unit
t_{DD}	Active Clock edge to MOSI data output valid	–	6	
t_{CSS}	SPIx_CSx setup time	2	–	ns
t_{CSH}	SPIx_CSx hold time	3	–	ns
t_{CS}	SPIx_CSx high time	10	–	ns

Figure 2: SPI Slave Timing Diagram

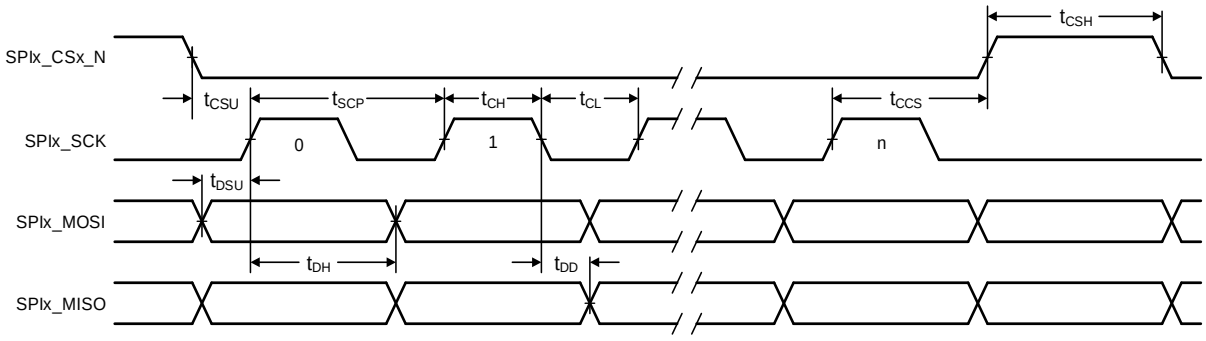


Table 11: SPI Slave Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{SDD}+ t_{MSU}$[1]$)$		ns
t_{SCH}	SPIx_SCK high time	$t_{SDD} + t_{MSU}$[1]		ns
t_{SCL}	SPIx_SCK low time	$t_{SDD} + t_{MSU}$[1]		ns
t_{SCSU}	SPIx_CSx_n setup time	1		t_{SCP}
t_{SCSH}	SPIx_CSx_n high time	1		t_{SCP}
t_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1	1	t_{SCP}
t_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1	1	ns
t_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2	11	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT1[2])	3.5	16	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT2[2])	3	13	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT3[2])	4	17	ns

1. t_{MSU} is the setup time required by the external master
2. ALT1/2/3 refers to the position of the SPI pins in the Signal Pinout Multiplexing tables in Section 3.1, *Signal List and Multiplexing Functions*.

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

1.9.5 Universal Asynchronous Receiver/Transmitter (UART)

The UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Note:	The UART receiver input has low baud rate tolerance in 1-stop bit mode. External devices must use two stop bits. In 1-stop bit mode, the UART receiver can lose sync between the receiver and the external transmitter resulting in data errors/corruption. In 2-stop bit mode, the extra stop bit allows the UART receiver logic to align properly with the UART transmitter.

Features:

- 3x UART Interfaces
- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200 MHz, baud rate of 12.5 Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both Tx and Rx
- 8-bit x 36 deep Tx FIFO
- 11-bit x 36 deep Rx FIFO. 3 bits of 11 bits per entry will log the Rx errors in FIFO mode (break, framing and parity errors as bits 10, 9, 8 of FIFO entry)
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 12: UART Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
99	UART0_TXD	UART #0 Transmit	Output	CMOS – 1.8V
101	UART0_RXD	UART #0 Receive	Input	CMOS – 1.8V
103	UART0_RTS*	UART #0 Request to Send	Output	CMOS – 1.8V
105	UART0_CTS*	UART #0 Clear to Send	Input	CMOS – 1.8V
203	UART1_TXD	UART #1 Transmit	Output	CMOS – 1.8V
205	UART1_RXD	UART #1 Receive	Input	CMOS – 1.8V
207	UART1_RTS*	UART #1 Request to Send	Output	CMOS – 1.8V
209	UART1_CTS*	UART #1 Clear to Send	Input	CMOS – 1.8V
236	UART2_TXD	UART #2 Transmit	Output	CMOS – 1.8V
238	UART2_RXD	UART #2 Receive	Input	CMOS – 1.8V

1.9.6 Controller Area Network (CAN)

Standard	Notes
ISO/DIS 16845-2	CAN conformance test
ISO 11898-1:2015	Data link layer and physical signaling; CAN FD Frame formats
ISO 11898-4:2004	Time-triggered communication

The Jetson TX2 NX series module supports connectivity to two CAN networks.

Features:

- CAN protocol version 2.0A, version 2.0B and ISO 11898-1:2006/11898-1:2015
  - Support ISO11898-1:2006 FD format and Bosch FD format
  - Dual clock source, enabling FM-PLL designs
  - 16, 32, 64, or 128 Message Objects (configurable)
  - Each Message Object has its own Identifier Mask
  - Programmable FIFO mode
  - Programmable loop-back mode for self-test
- Parity check for Message RAM (optional)
  - Maskable interrupt, two interrupt lines
  - MA support, automatic Message Object increment
  - Power-down support
- Supports TT CAN
  - TTCAN Level 0, 1, and 2
  - Time Mark Interrupts
  - Stop Watch
  - Watchdog Timer
  - Synchronization to external events

Table 13: CAN Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
145	CAN_TX	CAN PHY	Output	CMOS – 3.3V
143	CAN_RX	CAN PHY	Input	CMOS – 3.3V

1.9.7 Inter-Chip Communication (I^2C)

Standard	Notes
NXP inter-IC-bus (I^2C) specification	https://i2c.info/i2c-bus-specification

This general purpose I^2C controller allows system expansion for I^2C-based devices as defined in the NXP inter-IC-bus (I^2C) specification. The I^2C bus supports serial device communications to multiple devices. (4x I^2C) The I^2C controller handles clock source negotiation, speed negotiation for standard and fast devices, 7-bit slave address support according to the I^2C protocol and supports master and slave modes of operation.

The I^2C controller supports the following operating modes:

- Master – Standard-mode (up to 100 Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1 Mbit/s).
- Slave – Standard-mode (up to 100 Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1 Mbit/s).

Table 14: I2C Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
185	I2C0_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	Bidir	Open Drain – 3.3V
187	I2C0_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
189	I2C1_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
191	I2C1_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
232	I2C2_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
234	I2C2_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
213	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V

1.9.8 Inter-IC Sound (I^2S)

Standard
Inter-IC Sound (I^2S) specification

The Inter-IC Sound (I^2S) controller implements full-duplex, bidirectional and single direction point-to-point serial interfaces. It can interface with I^2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, modems, Bluetooth chips, etc. The Jetson TX2 NX series module supports four I^2S audio outputs with I^2S/PCM interfaces supporting clock rates up to 24.576 MHz.

Features:

- Basic I^2S modes to be supported (I^2S, RJM, LJM, and DSP) in both master and slave modes
- PCM mode with short (one bit-clock wide) and long-fsync (two bit-clock wide) in both master and slave modes
- NW-mode with independent slot-selection for both transmit and receive
- TDM mode with flexibility in number of slots and slot(s) selection
- Capability to drive-out a high-z outside the prescribed slot for transmission
- Flow control for the external input/output stream

Table 15: I2S Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
199	I2S0_SCLK	I2S Audio Port 0 Clock	Bidir	CMOS – 1.8V
197	I2S0_FS	I2S Audio Port 0 Left/Right Clock	Bidir	CMOS – 1.8V
193	I2S0_DOUT	I2S Audio Port 0 Data Out	Output	CMOS – 1.8V
195	I2S0_DIN	I2S Audio Port 0 Data In	Input	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V

Pin #	Signal Name	Description	Direction	Pin Type
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V
124	I2S2_DOUT	I2S Audio Port 2 Data Out	Bidir	CMOS – 1.8V
126	I2S2_DIN	I2S Audio Port 2 Data In	Bidir	CMOS – 1.8V
127	I2S2_FS	I2S Audio Port 2 Left/Right Clock	Input	CMOS – 1.8V
128	I2S2_SCLK	I2S Audio Port 2 Clock	Bidir	CMOS – 1.8V
112	I2S3_DIN	I2S Audio Port 3 Data In	Bidir	CMOS – 1.8V
218	I2S3_DOUT	I2S Audio Port 3 Data Out	Bidir	CMOS – 1.8V
130	I2S3_FS	I2S Audio Port 3 Left/Right Clock	Bidir	CMOS – 1.8V
212	I2S3_SCLK	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V

Table 16: TDM Timing Parameters (Slave Mode)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
F_{SCK}	Frequency	–	24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$	–	ns	
T_{FDLY}	I2Sx_LRCK delay	0	4.5	ns	
t_{DDLY}	I2Sx_SDOUT delay	0	4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	ns	
t_{DH}	I2Sx_SDIN hold time	2	–	ns	
t_{RT}	I2Sx_SCLK rise time	–	5% * T_{CYL}	ns	
t_{FT}	I2Sx_SCLK fall time	–	5% * T_{CYL}	ns	
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}	–	ns	
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}	–	ns	

Table 17: TDM Timing Parameters (Master Mode)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
F_{SCK}	Frequency	–	24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$	–	ns	
t_{DDLY}	I2Sx_SDOUT delay	0	4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	ns	
t_{DH}	I2Sx_SDIN hold time	2	–	ns	
t_{FSU}	I2Sx_LRCK setup	2	45% * T_{CYL} - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	55% T_{CYL} + 2	–	ns	2
t_{RT}	I2Sx_SCLK rise time	–	5% * T_{CYL}	ns	
t_{FT}	I2Sx_SCLK fall time	–	5% * T_{CYL}	ns	

Symbol	Parameter	Minimum	Maximum	Unit	Notes
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}	–	ns	
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}	–	ns	

1. Maximum t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Minimum t_{FSH} (55% TCYL + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Minimum t_{FSH} is 2ns.

1.9.9 Gigabit Ethernet

Standard	Notes
Gigabit Ethernet (GbE)	IEEE 802.3ab

The on-module Ethernet controller supports:

- 10/100/1000 Gigabit Ethernet
- IEEE 802.3u Media Access Controller (MAC)

Table 18: Gigabit Ethernet Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
184	GBE_MDI0_N	GbE Transformer Data 0–	Bidir	MDI
186	GBE_MDI0_P	GbE Transformer Data 0+	Bidir	MDI
190	GBE_MDI1_N	GbE Transformer Data 1–	Bidir	MDI
192	GBE_MDI1_P	GbE Transformer Data 1+	Bidir	MDI
196	GBE_MDI2_N	GbE Transformer Data 2–	Bidir	MDI
198	GBE_MDI2_P	GbE Transformer Data 2+	Bidir	MDI
202	GBE_MDI3_N	GbE Transformer Data 3–	Bidir	MDI
204	GBE_MDI3_P	GbE Transformer Data 3+	Bidir	MDI
188	GBE_LED_LINK	Ethernet Link LED (Green)	Output	
194	GBE_LED_ACT	Ethernet Activity LED (Yellow)	Output	

1.9.10 Fan

The Jetson TX2 NX includes a Pulse Width Modulator (PWM) and Tachometer functionality to enable fan control as part of a thermal solution. The PWM controller is a frequency divider with a varying pulse width. The PWM runs off a device clock programmed in the Clock and Reset controller and can be any frequency up to the device clock maximum speed of 48 MHz. The PWM gets divided by 256 before being subdivided based on a programmable value.

1.9.11 Pulse Width Modulator (PWM)

Jetson TX2 NX has three Pulse Width Modulator (PWM) outputs. Each PWM output is based on a frequency divider whose pulse width varies. Each has a programmable frequency divider and a programmable pulse width generator. The PWM controller supports one PWM output for each of its four instances. Each instance is allocated a 64 KB independent address space.

Frequency division is a 13-bit programmable value, and pulse division is an 8-bit value. The PWM can run at a maximum frequency of up to 408 MHz. The PWM controller can source its clock from either CLK_M or PLLP. CLK_M (19.2 MHz) is derived from the OSC clock (38.4 MHz). PLLP operates at 408 MHz.

The PWM clock frequency is divided by 256 before subdividing it based on the programmable frequency division value to generate the required frequency for the PWM output. The maximum output frequency that can be achieved from this configuration is 408 MHz/256 = 1.6 MHz. This 1.6 MHz frequency can be further divided using the frequency divisor in PWM.

The OSC clock is the primary/default source for the PWM IP clock. For higher PWM output frequency requirements, PLLP is the clock source (up to 408 MHz).

Table 19: PWM Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
206	GPIO07	Pulse Width Modulator or GPIO #7	Bidir	CMOS – 1.8V
228	GPIO13	Pulse Width Modulator or GPIO #13	Bidir	CMOS – 1.8V
230	GPIO14	Pulse Width Modulator or GPIO #14	Bidir	CMOS – 1.8V

2.0 Power and System Management

VIN must be supplied by the carrier board that the module is designed to connect to. All interfaces are referenced to on-module voltage rails, additional I/O voltage is not required to be supplied to the module. See the *Jetson TX2 NX Product Design Guide* for details on connecting to each of the interfaces.

Table 20: Power and System Control Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
251 252 253 254 255 256 257 258 259 260	VDD_IN	Main power – Supplies PMIC and other registers	Input	5.0V
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	1.65V-5.5V
233	SHUTDOWN_REQ*	Used by the module to request a shutdown from the carrier board. Pull up to VDD_IN with ~5kΩ (4.02k + 1k) on the module.	Output	Analog – 5.0V
237	POWER_EN	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 100kΩ pulldown is also on the module.	Input	CMOS – 5.0V
239	SYS_RESET*	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. Pull up to 1.8V with 10kΩ resistor on the module.	Bidir	Open Drain – 1.8V
178	MOD_SLEEP*	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	Output	CMOS – 1.8V
210	CLK_32K_OUT	Sleep/Suspend clock	Output	CMOS – 1.8V
214	FORCE_RECOVERY*	Force Recovery strap pin	Input	CMOS – 1.8V
240	SLEEP/WAKE*	Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	Input	CMOS – 5.0V

2.1 Power Rails

VDD_IN must be supplied by the carrier board that the Jetson TX2 NX is designed to connect to. All Jetson TX2 NX interfaces are referenced to on-module voltage rails and no I/O voltage is required to be supplied to the module. See the *Jetson TX2 NX Product Design Guide* for details of connecting to each of the interfaces.

2.2 Power Domains/Islands

Jetson TX2 NX has a single three-channel INA that can measure power of CPU_GPU_SRAM combined rail, Core (SoC), and module input power (VDD_IN).

2.3 Power Management Controller (PMC)

The PMC power management features enable both high speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC, USB) which can wake the system from deep sleep state. The PMC enables aggressive power-gating capabilities on idle modules and integrates specific logic to maintain defined states and control power domains during sleep and deep sleep modes.

2.4 Resets

If you assert reset, then the Jetson TX2 NX and onboard storage will be reset. This signal is also used for baseboard power sequencing.

2.5 PMIC_BBAT

An optional back up battery can be attached to the VCC_RTC module input to maintain the module real-time clock (RTC) when VIN is not present. This pin is connected directly to the onboard PMIC. Details of the types of backup cells that optionally can be connected are found in the PMIC manufacturer's data sheet. When a backup cell is connected to the PMIC, the RTC retains its contents and can be configured to charge the backup cell as well. RTC accuracy is 2 seconds/day in typical room temperature only.

The following backup cells may be attached to this pin:

- Super capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells

The backup cells must provide a voltage in the range 2.5V to 3.5V. These are charged with a constant current, and a constant voltage charger that can be configured between 2.5V and 3.5V (constant voltage) output and 50 µA to 800 µA (constant current).

Table 21: PMIC_BBAT Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power. Constant current of 2.0µA for 2.45V; 2.2µA for 3.0V typical; 4.2µA maximum.	Bidir	1.65V-5.5V

2.6 Power Sequencing

The Jetson TX2 NX is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the SYS_RESET* signal (when deasserted) is used to indicate when the carrier board can power on. The following sections provide an overview of the power sequencing steps between the carrier board and Jetson TX2 NX. Refer to the *Jetson TX2 NX Product Design Guide* for system level details on the application of power, power sequencing, and

monitoring. The Jetson TX2 NX and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

2.6.1 Power Up

During power up, the carrier board must wait until the signal SYS_RESET* is deasserted from the Jetson module before enabling its power; the Jetson module will deassert the SYS_RESET* signal to enable the complete system to boot.

Note:	I/O pins cannot be high (>0.5V) before SYS_RESET* goes high. When SYS_RESET* is low, the maximum voltage applied to any I/O pin is 0.5V.

2.6.2 Power Down

Shutdown events can be triggered by either the module or the baseboard, but the shutdown event will always be serviced by the baseboard. To do so, the baseboard deasserts POWER_EN, which begins the shutdown power sequence on the module. If the module needs to request a shutdown event in the case of thermal, software, or under-voltage events, it will assert SHUTDOWN_REQ*. When the baseboard sees low SHUTDOWN_REQ*, it should deassert POWER_EN as soon as possible.

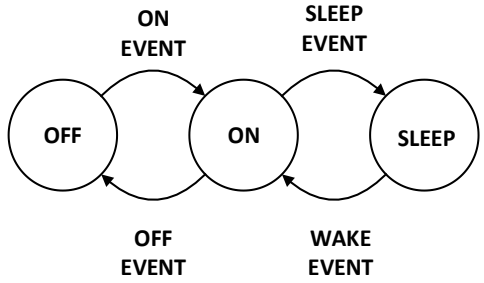
Once POWER_EN is deasserted, the module will assert SYS_RESET*, and the baseboard may shut down. SoC 3.3V I/O must reach 0.5V or lower at most 1.5ms after SYS_RESET* is asserted. SoC 1.8V I/O must reach 0.5V or lower at most 4ms after SYS_RESET* is asserted.

Note:	Refer to the *Jetson TX2 NX Product Design Guide* for additional Power Sequence information.

2.7 Power States

The Jetson TX2 NX operates in three main power modes: OFF, ON, and SLEEP. The module transitions between these states are based on various events from hardware or software. Figure 3 shows the transitions between these three states.

Figure 3: Power State Transition Diagram



2.7.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state, the Jetson TX2 NX module is fully functional and operates normally. An ON event must occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_EN pin. This must occur with VDD_IN connected to a power rail and POWER_EN is asserted (at a logic1). The POWER_EN control is the carrier board indication to the Jetson module that the VDD_IN power is good. The carrier board should assert this high only when VDD_IN has reached its required voltage level and is stable. This prevents the Jetson TX2 NX Module from powering up until the VDD_IN power is stable.

When in the ON power state, the Jetson TX2 NX series module includes various design features to minimize the power when possible. These include such items as:

- Advanced Power Management IC (PMIC)
- On system Power Gating
- Advanced on chip Clock Gating
- Dynamic Voltage and Frequency Scaling (DVFS)
- Always on logic used to wake the system based on either a timer event or an external trigger (e.g., key press).
- Low power DRAM (LPDDR4)

2.7.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state, through an OFF event. OFF events are listed in the table below.

Table 22: OFF State Events

Event	Details	Preconditions
HW Shutdown	Set POWER_EN pin to zero for at least 100 µs, the internal PMIC starts the shutdown sequence.	In ON State
SW Shutdown	Software initiated shutdown	ON state, software operational
Thermal Shutdown	If the internal temperature of the Jetson TX2 NX module reaches an unsafe temperature, the hardware is designed to initiate a shutdown.	Any power state

Note: Hardware shutdown, Software shutdown, and Thermal shutdown will all assert SHUTDOWN_REQ* low. System on Module will not initiate power supply shutdown sequence until POWER_EN is deasserted. POWER_EN debounce is 1ms on Jetson TX2 NX.

2.7.3 SLEEP State

The SLEEP state can only be entered from the ON state. This state allows the module to quickly resume to an operational state without performing a full boot sequence. The SLEEP state also includes a low power mode SC7 (deep sleep) where the module operates only with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state, the output signals from the module are maintained at their logic level prior to entering the state (i.e., they do not change to a 0V level). To exit the SLEEP state a WAKE event must occur; WAKE events can occur from within the module or from external devices through various pins on the module connector.

Table 23: SLEEP and WAKE Events

Event	Details
RTC WAKE Up	Timers within the module can be programmed, on SLEEP entry. When these expire, they create a WAKE event to exit the SLEEP state.
Thermal Condition	If the module internal temperature exceeds programmed hot and cold limits the system is forced to wake up, so it can report and take appropriate action (shut down for example).
USB VBUS Detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate.
Module Connector Interface WAKE Signal	Programmable signals on the module connector.

2.8 Thermal and Power Monitoring

The Jetson TX2 NX is designed to operate under various workloads and environmental conditions. It has been designed so that an active or passive heat sink solution can be attached. The module contains various methods through hardware and software to limit the internal temperature to within operating limits. See the *Jetson TX2 NX Thermal Design Guide* for more details.

2.9 Overcurrent Throttling

The power monitor triggers CPU/GPU hardware throttling to keep power within budget.

- INA warning signals lite GPU throttling (50%) when VDD_IN average power (512 samples) exceeds 15W
- INA critical signal triggers lite CPU+GPU throttling (50%) when VDD_IN instantaneous power exceeds 18W

3.0 Pin Definitions

The function(s) for each pin on the module is fixed to a single Special-Function I/O (SFIO) or software-controlled General Purpose I/O (GPIO). The Jetson TX2 NX has multiple dedicated GPIOs and each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls. SFIO and GPIO functionality is configured using Multi-Purpose I/O (MPIO) pads with each MPIO pad consisting of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either Schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pads are partitioned into multiple pad control groups with controls being configured for the group. During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the *Jetson TX2 NX Product Design Guide* for more information.

3.1 Power-on Reset Behavior

Each MPIO pad has a deterministic power-on reset (PoR) state. The reset state for each pad is chosen to minimize the need of additional on-board components; for example, on-chip weak pull-ups are enabled during PoR for pads which are usually used to drive active-low chip selects eliminating the need for additional pull-up resistors.

The following list is a simplified description of the Jetson TX2 NX boot process focusing on those aspects which relate to the MPIO pins:

- System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET*.
- The boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device (eMMC).
- The boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
- If the BCT and boot loader are fetched successfully, the boot ROM transfers control to the boot loader.
- Otherwise, the boot ROM enters USB recovery mode.

3.2 Sleep Behavior

Sleep is an ultra-low-power standby state in which the module maintains much of its I/O state while most of the chip is powered off. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering DPD is same across pads.

MPIO pads can vary during deep sleep. They differ regarding:

- Input buffer behavior during deep sleep
    - Forcibly disabled OR
    - Enabled for use as a GPIO wake event, OR
    - Enabled for some other purpose (e.g., a clock request pin)
- Output buffer behavior during deep sleep
    - Maintain a static programmable (0, 1, or tristate) constant value OR
    - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep

- Forcibly disabled OR
- Can be configured

- Pads that do not enter deep sleep
  - Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep at any time.

3.3 GPIO

The Jetson TX2 NX has multiple dedicated GPIOs. Each GPIO can be individually configurable as an Output, Input, or Interrupt source with level/edge controls. The pins listed in the following table are dedicated GPIOs; some with alternate SFIO functionality. Many other pins not included in this list are capable of being configured as GPIOs instead of the SFIO functionality the pin name suggests (e.g., UART, SPI, I^2S, etc.). All pins that can support GPIO functionality have this exposed in the Pinmux.

Table 24: GPIO Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
87	GPIO00	GPIO #0 or USB 0 VBUS Enable #0	Bidir	CMOS – 1.8V
118	GPIO01	GPIO #1 or Generic Clocks	Bidir	CMOS – 1.8V
124	GPIO02	GPIO #2	Bidir	CMOS – 1.8V
126	GPIO03	GPIO #3	Bidir	CMOS – 1.8V
127	GPIO04	GPIO #4	Bidir	CMOS – 1.8V
128	GPIO05	GPIO #5	Bidir	CMOS – 1.8V
130	GPIO06	GPIO #6	Bidir	CMOS – 1.8V
206	GPIO07	GPIO #7 or Pulse Width Modulator	Bidir	CMOS – 1.8V
208	GPIO08	GPIO #8 or Fan Tach	Bidir	CMOS – 1.8V
211	GPIO09	GPIO #9 or Audio Codec Master Clock	Bidir	CMOS – 1.8V
212	GPIO10	GPIO #10	Bidir	CMOS – 1.8V
216	GPIO11	GPIO #11 or Generic Clocks	Bidir	CMOS – 1.8V
218	GPIO12	GPIO #12 or Pulse Width Modulator	Bidir	CMOS – 1.8V
228	GPIO13	GPIO #13 or Pulse Width Modulator	Bidir	CMOS – 1.8V
230	GPIO14	GPIO #14 or Pulse Width Modulator	Bidir	CMOS – 1.8V

3.4 Jetson TX2 NX Pin List

Jetson TX2 NX Signal Name	Jetson TX2 NX Function	Pin # Top Odd		Pin # Bottom Even	Jetson TX2 NX Signal Name	Jetson TX2 NX Function
GND	GND	1		2	GND	GND
CSI1_D0_N	CSI1_D0_N	3		4	CSI0_D0_N	CSI0_D0_N
CSI1_D0_P	CSI1_D0_P	5		6	CSI0_D0_P	CSI0_D0_P
GND	GND	7		8	GND	GND
CSI1_CLK_N	CSI1_CLK_N	9		10	CSI0_CLK_N	CSI0_CLK_N
CSI1_CLK_P	CSI1_CLK_P	11		12	CSI0_CLK_P	CSI0_CLK_P
GND	GND	13		14	GND	GND
CSI1_D1_N	CSI1_D1_N	15		16	CSI0_D1_N	CSI0_D1_N
CSI1_D1_P	CSI1_D1_P	17		18	CSI0_D1_P	CSI0_D1_P
GND	GND	19		20	GND	GND
CSI3_D0_N	CSI3_D0_N	21		22	CSI2_D0_N	CSI2_D0_N
CSI3_D0_P	CSI3_D0_P	23		24	CSI2_D0_P	CSI2_D0_P
GND	GND	25		26	GND	GND
CSI3_CLK_N	CSI3_CLK_N	27		28	CSI2_CLK_N	CSI2_CLK_N
CSI3_CLK_P	CSI3_CLK_P	29		30	CSI2_CLK_P	CSI2_CLK_P
GND	GND	31		32	GND	GND
CSI3_D1_N	CSI3_D1_N	33		34	CSI2_D1_N	CSI2_D1_N
CSI3_D1_P	CSI3_D1_P	35		36	CSI2_D1_P	CSI2_D1_P
GND	GND	37		38	GND	GND
DP0_TXD0_N	DP0_TXD0_N	39		40	CSI4_D2_N	CSI4_D2_N
DP0_TXD0_P	DP0_TXD0_P	41		42	CSI4_D2_P	CSI4_D2_P
GND	GND	43		44	GND	GND
DP0_TXD1_N	DP0_TXD1_N	45		46	CSI4_D0_N	CSI4_D0_N
DP0_TXD1_P	DP0_TXD1_P	47		48	CSI4_D0_P	CSI4_D0_P
GND	GND	49		50	GND	GND
DP0_TXD2_N	DP0_TXD2_N	51		52	CSI4_CLK_N	CSI4_CLK_N
DP0_TXD2_P	DP0_TXD2_P	53		54	CSI4_CLK_P	CSI4_CLK_P
GND	GND	55		56	GND	GND
DP0_TXD3_N	DP0_TXD3_N	57		58	CSI4_D1_N	CSI4_D1_N
DP0_TXD3_P	DP0_TXD3_P	59		60	CSI4_D1_P	CSI4_D1_P
GND	GND	61		62	GND	GND
DP1_TXD0_N	DP1_TXD0_N	63		64	CSI4_D3_N	CSI4_D3_N
DP1_TXD0_P	DP1_TXD0_P	65		66	CSI4_D3_P	CSI4_D3_P
GND	GND	67		68	GND	GND
DP1_TXD1_N	DP1_TXD1_N	69		70	DSI_D0_N	DSI_D0_N
DP1_TXD1_P	DP1_TXD1_P	71		72	DSI_D0_P	DSI_D0_P
GND	GND	73		74	GND	GND
DP1_TXD2_N	DP1_TXD2_N	75		76	DSI_CLK_N	DSI_CLK_N
DP1_TXD2_P	DP1_TXD2_P	77		78	DSI_CLK_P	DSI_CLK_P
GND	GND	79		80	GND	GND
DP1_TXD3_N	DP1_TXD3_N	81		82	DSI_D1_N	DSI_D1_N
DP1_TXD3_P	DP1_TXD3_P	83		84	DSI_D1_P	DSI_D1_P
GND	GND	85		86	GND	GND
GPIO00	GPIO00	87		88	DP0_HPD	DP0_HPD
SPI0_MOSI	SPI0_MOSI	89		90	DP0_AUX_N	DP0_AUX_N
SPI0_SCK	SPI0_SCK	91		92	DP0_AUX_P	DP0_AUX_P
SPI0_MISO	SPI0_MISO	93		94	HDMI_CEC	HDMI_CEC
SPI0_CS0*	SPI0_CS0*	95		96	DP1_HPD	DP1_HPD
SPI0_CS1*	SPI0_CS1*	97		98	DP1_AUX_N	DP1_AUX_N
UART0_TXD	UART0_TXD	99		100	DP1_AUX_P	DP1_AUX_P
UART0_RXD	UART0_RXD	101		102	GND	GND
UART0_RTS*	UART0_RTS*	103		104	SPI1_MOSI	SPI1_MOSI
UART0_CTS*	UART0_CTS*	105		106	SPI1_SCK	SPI1_SCK
GND	GND	107		108	SPI1_MISO	SPI1_MISO
USB0_D_N	USB0_D_N	109		110	SPI1_CS0*	SPI1_CS0*
USB0_D_P	USB0_D_P	111		112	SPI1_CS1*	I2S3_DIN
GND	GND	113		114	CAM0_PWDN	CAM0_PWDN
USB1_D_N	USB1_D_N	115		116	CAM0_MCLK	CAM0_MCLK
USB1_D_P	USB1_D_P	117		118	GPIO01	GPIO01
GND	GND	119		120	CAM1_PWDN	CAM1_PWDN
USB2_D_N	USB2_D_N	121		122	CAM1_MCLK	CAM1_MCLK
USB2_D_P	USB2_D_P	123		124	GPIO02	I2S2_DOUT
GND	GND	125		126	GPIO03	I2S2_DIN

Jetson TX2 NX Signal Name	Jetson TX2 NX Function	Pin # Top Odd		Pin # Bottom Even	Jetson TX2 NX Signal Name	Jetson TX2 NX Function
GPIO04	I2S2_FS	127		128	GPIO05	I2S2_SCLK
GND	GND	129		130	GPIO06	I2S3_FS
PCIE0_RX0_N	PCIE0_RX0_N	131		132	GND	GND
PCIE0_RX0_P	PCIE0_RX0_P	133		134	PCIE0_TX0_N	PCIE0_TX0_N
GND	GND	135		136	PCIE0_TX0_P	PCIE0_TX0_P
PCIE0_RX1_N	PCIE0_RX1_N	137		138	GND	GND
PCIE0_RX1_P	PCIE0_RX1_P	139		140	PCIE0_TX1_N	PCIE0_TX1_N
GND	GND	141		142	PCIE0_TX1_P	PCIE0_TX1_P
CAN_RX	CAN_RX	143		144	GND	GND
CAN_TX	CAN_TX	145		146	GND	GND
GND	GND	147		148	PCIE0_TX2_N	RSVD
PCIE0_RX2_N	RSVD	149		150	PCIE0_TX2_P	RSVD
PCIE0_RX2_P	RSVD	151		152	GND	GND
GND	GND	153		154	PCIE0_TX3_N	RSVD
RSVD	RSVD	155		156	PCIE0_TX3_P	RSVD
RSVD	RSVD	157		158	GND	GND
GND	GND	159		160	PCIE0_CLK_N	PCIE0_CLK_N
USBSS_RX_N	USBSS_RX_N	161		162	PCIE0_CLK_P	PCIE0_CLK_P
USBSS_RX_P	USBSS_RX_P	163		164	GND	GND
GND	GND	165		166	USBSS_TX_N	USBSS_TX_N
PCIE1_RX0_N	PCIE1_RX0_N	167		168	USBSS_TX_P	USBSS_TX_P
PCIE1_RX0_P	PCIE1_RX0_P	169		170	GND	GND
GND	GND	171		172	PCIE1_TX0_N	PCIE1_TX0_N
PCIE1_CLK_N	PCIE1_CLK_N	173		174	PCIE1_TX0_P	PCIE1_TX0_P
PCIE1_CLK_P	PCIE1_CLK_P	175		176	GND	GND
GND	GND	177		178	MOD_SLEEP*	MOD_SLEEP*
PCIE_WAKE*	PCIE_WAKE*	179		180	PCIE0_CLKREQ*	PCIE0_CLKREQ*
PCIE0_RST*	PCIE0_RST*	181		182	PCIE1_CLKREQ*	PCIE1_CLKREQ*
PCIE1_RST*	PCIE1_RST*	183		184	GBE_MDI0_N	GBE_MDI0_N
I2C0_SCL	I2C0_SCL	185		186	GBE_MDI0_P	GBE_MDI0_P
I2C0_SDA	I2C0_SDA	187		188	GBE_LED_LINK	GBE_LED_LINK
I2C1_SCL	I2C1_SCL	189		190	GBE_MDI1_N	GBE_MDI1_N
I2C1_SDA	I2C1_SDA	191		192	GBE_MDI1_P	GBE_MDI1_P
I2S0_DOUT	I2S0_DOUT	193		194	GBE_LED_ACT	GBE_LED_ACT
I2S0_DIN	I2S0_DIN	195		196	GBE_MDI2_N	GBE_MDI2_N
I2S0_FS	I2S0_FS	197		198	GBE_MDI2_P	GBE_MDI2_P
I2S0_SCLK	I2S0_SCLK	199		200	GND	GND
GND	GND	201		202	GBE_MDI3_N	GBE_MDI3_N
UART1_TXD	UART1_TXD	203		204	GBE_MDI3_P	GBE_MDI3_P
UART1_RXD	UART1_RXD	205		206	GPIO07	GPIO07
UART1_RTS*	UART1_RTS*	207		208	GPIO08	GPIO08
UART1_CTS*	UART1_CTS*	209		210	CLK_32K_OUT	CLK_32K_OUT
GPIO09	GPIO09	211		212	GPIO10	I2S3_SCLK
CAM_I2C_SCL	CAM_I2C_SCL	213		214	FORCE_RECOVERY*	FORCE_RECOVERY*
CAM_I2C_SDA	CAM_I2C_SDA	215		216	GPIO11	GPIO11
GND	GND	217		218	GPIO12	I2S3_DOUT
SDMMC_DAT0	SDMMC_DAT0	219		220	I2S1_DOUT	I2S1_DOUT
SDMMC_DAT1	SDMMC_DAT1	221		222	I2S1_DIN	I2S1_DIN
SDMMC_DAT2	SDMMC_DAT2	223		224	I2S1_FS	I2S1_FS
SDMMC_DAT3	SDMMC_DAT3	225		226	I2S1_SCLK	I2S1_SCLK
SDMMC_CMD	SDMMC_CMD	227		228	GPIO13	GPIO13
SDMMC_CLK	SDMMC_CLK	229		230	GPIO14	GPIO14
GND	GND	231		232	I2C2_SCL	I2C2_SCL
SHUTDOWN_REQ*	SHUTDOWN_REQ*	233		234	I2C2_SDA	I2C2_SDA
PMIC_BBAT	PMIC_BBAT	235		236	UART2_TXD	UART2_TXD
POWER_EN	POWER_EN	237		238	UART2_RXD	UART2_RXD
SYS_RESET*	SYS_RESET*	239		240	SLEEP/WAKE*	SLEEP/WAKE*
GND	GND	241		242	GND	GND
GND	GND	243		244	GND	GND
GND	GND	245		246	GND	GND
GND	GND	247		248	GND	GND
GND	GND	249		250	GND	GND
VDD_IN	VDD_IN	251		252	VDD_IN	VDD_IN
VDD_IN	VDD_IN	253		254	VDD_IN	VDD_IN
VDD_IN	VDD_IN	255		256	VDD_IN	VDD_IN

Jetson TX2 NX Signal Name	Jetson TX2 NX Function	Pin # Top Odd		Pin # Bottom Even	Jetson TX2 NX Signal Name	Jetson TX2 NX Function
VDD_IN	VDD_IN	257		258	VDD_IN	VDD_IN
VDD_IN	VDD_IN	259		260	VDD_IN	VDD_IN

Note: For cell shading, light green indicates ground; light blue indicates Jetson TX2 NX specific functionality.

4.0 DC Characteristics

4.1 Operating and Absolute Maximum Ratings

The parameters listed in following table are specific to a temperature range and operating voltage. Operating the Jetson TX2 NX beyond these parameters is not recommended.

WARNING: Exceeding the listed conditions may damage and/or affect long-term reliability of the part.
The Jetson TX2 NX module should never be subjected to conditions extending beyond the ratings listed below.

Table 25: Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_{DC}	VDD_IN	4.75	5.0	5.25	V
	PMIC_BBAT	1.65	-	5.5	V

Absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, performance is not guaranteed, and device reliability may be affected. It is not recommended to operate the Jetson TX2 NX module under these conditions.

Table 26: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VDD_{MAX}	VDD_IN	-0.5	5.5	V	
	PMIC_BBAT	-0.3	6.0	V	
IDD_{MAX}	VDD_IN I_{max}	-	5	A	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	VDD + 0.5V when CARRIER_PWR_ON high and associated I/O rail powered. I/O pins cannot be high (>0.5V) before CARRIER_PWR_ON goes high. When CARRIER_PWR_ON is low, the maximum voltage applied to any I/O pin is 0.5V
	DD pins configured as open drain	-0.5	3.63	V	The pin's output-driver must be set to open-drain mode
T_{OP}	Operating Temperature	-25	See Note	°C	See the *Jetson TX2 NX Thermal Design Guide* for details.
T_{STG}	Storage Temperature (ambient)	-40	80	°C	
M_{MAX}	Mounting Force	-	See Note	kgf	Maximum force: 3.63 kgf (8.0 lbs.) Pressure: 241 kPa (35 psi). Pressure must be applied on the die. See the *Jetson TX2 NX Thermal Design Guide* for additional details on mounting a thermal solution.

4.2 Environmental and Mechanical Screening

Module performance was assessed against a series of industry standard tests designed to evaluate robustness and estimate the failure rate of an electronic assembly in the environment in which it will be used. Mean Time Between Failures (MTBF) calculations are produced in the design phase to predict a product's future reliability in the field.

Table 27: Jetson TX2 NX Reliability Report

Test	Test Conditions	Reference Standard	Results
Temperature Humidity Biased	85°C / 85% RH, 168 hours, Power ON	JESD22-A101	PASS
Temperature Cycling	-40°C to 105°C, 500 cycles, non-operational	JESD22-A104, IPC9701	PASS
Board-level Power Cycling	40°C to 130°C, with a heater attached on top of SoC, 15 min/cycle, 2000 cycles,	NV Standard	PASS
Mechanical Shock – 140G Non-Op	140G, half sine, one shock/orientation, six orientations total, non-operational	JESD22-B110	PASS
Mechanical Shock – 50G Op	50G, half sine, 6 msec, three shocks/orientation, six orientations total, operational	IEC 600068 2-27	PASS
Sine Vibration – 3G	3G, 10-500 Hz, two sweep/axis, three axes total, non-operational	IEC60068-2-6	PASS
Random Vibration – 2G Non-Op	10-500 Hz, 2 Grms, 1 hour/axis, non-operational	IEC60068-2-64	PASS
Random Vibration – 5G Non-Op	10-500 Hz, 5 Grms, 8 hours/axis, non-operational	IEC60068-2-64	PASS
Random Vibration – 1G Op	10-500 Hz, 1 Grms, 30 min/axis, operational	IEC60068-2-64	PASS
Hard Boot	Power ON/OFF, ON for 150 sec OFF for 30 sec: 2000 cycles at 25°C 1000 cycles at -5°C 1000 cycles at 45°C	NV Standard	PASS
Operational Low Temp	-20°C, 24 hours, operational	NV Standard	PASS
Operational High Temp	45°C, 90%RH, 500 hours, operational	NV Standard	PASS
MTBF (mean time between failures)	Controlled Environment (GB), T = 35°C, CL = 90%	Telcordia SR-332, ISSUE 3 Parts Count (Method I)	2,197K Hrs
MTBF (mean time between failures)	Uncontrolled Environment (GF), T = 35°C, CL = 90%	Telcordia SR-332, ISSUE 3 Parts Count (Method I)	1,511K Hrs

4.3 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 28: CMOS Pin Type DC Characteristics

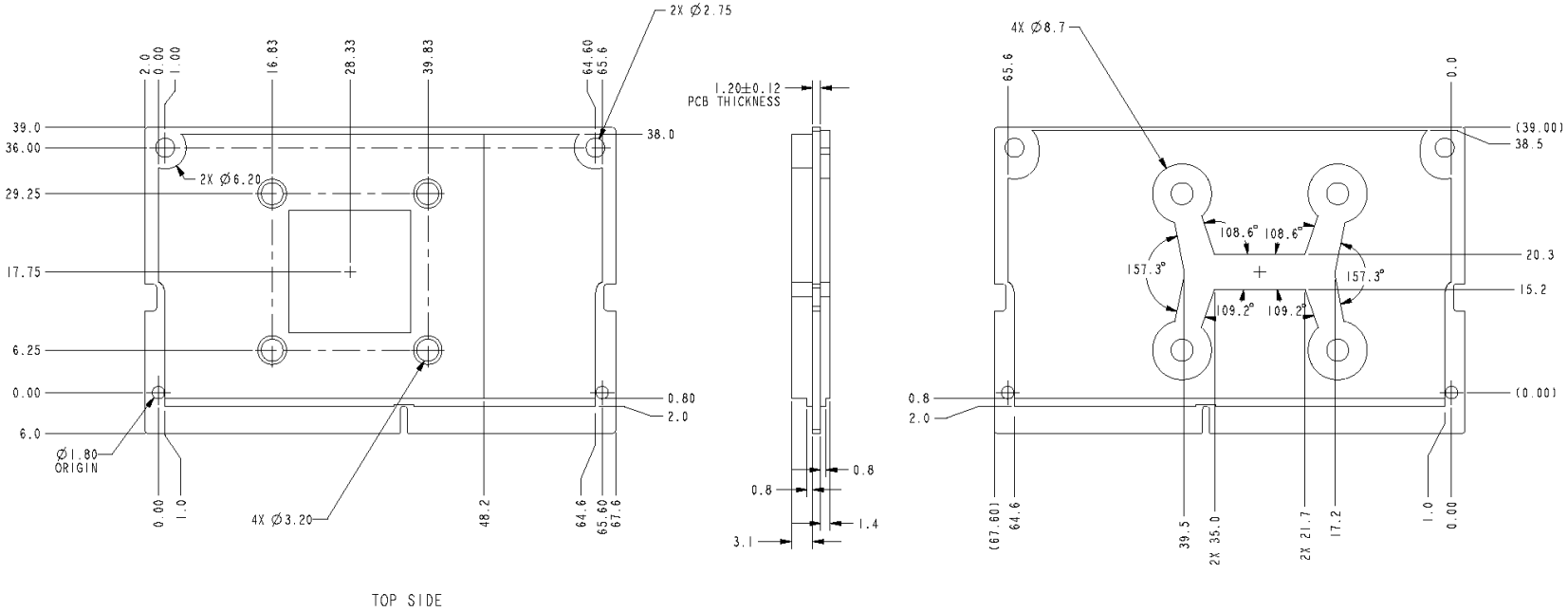
Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	-	V

Table 29: Open Drain Pin Type DC Characteristics

Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
	I^2C [1,0] Output Low Voltage (I_{OL} = 2mA) (see note)	-	0.3 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	-	V

Note: I2C[1,0]_[SCL, SDA] pins pull-up to 3.3V through on module 2.2kΩ resistor. I2C2_[SCL, SDA] pins pull-up to 1.8V through on module 2.2kΩ resistor.

5.0 Package Drawing and Dimensions



Note:

- All dimensions are in millimeters unless otherwise specified.
- Tolerances are: .X ± 0.25, .XX ± is 0.1, Angle ± is 1°
- SoC height information: Minimum is 1.10 mm, Nominal is 1.20 mm, Maximum is 1.30 mm

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