FE2.1

USB 2.0 HIGH SPEED 7-PORT HUB CONTROLLER

Data Sheet

INTRODUCTION

The FE2.1 is a highly integrated, high quality, high performance, low power consumption, yet low overall cost solution for USB 2.0 High Speed 7-Port Hub.

It adopts *Multiple Transaction Translator* (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – include even the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special *Build-In-Self-Test* mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components in the packaging and testing stages as well.

Low power consumption is achieved by using 0.18μ m technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

FEATURES

- Low power consumption
    - □ 155 mA when seven downstream facing ports enabled in High-Speed mode;
    - □ 66 mA when one downstream facing port enabled in High-Speed mode;
- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
    - □ Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
    - □ 7 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister and crystal load capacitor;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Multiple Transaction Translator* (MTT) –
    - □ One TT for each downstream port;

- □ Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
- □ Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- ■ Support Self-Powered Mode only;
- ■ Board configured options –
  - □ *Ganged* or *Individual Power Control Mode* select;
  - □ *Global*, *Multiple Ganges*, or *Individual Over-Current Protection Mode* select;
  - □ *Removable* or *Non-Removable Downstream Devices* configuration;
  - □ *Number of Downstream Ports*;
- ■ EEPROM configured options –
  - □ *Vendor ID*, *Product ID*, & *Device Release Number*;
  - □ *Removable* or *Non-Removable Downstream Devices* configuration;
  - □ *Serial Number*; and
  - □ *Number of Downstream Ports*;
- ■ Comprehensive status indicators support:
  - □ Standard downstream port status indicators (Green and Amber LED control for each downstream port);
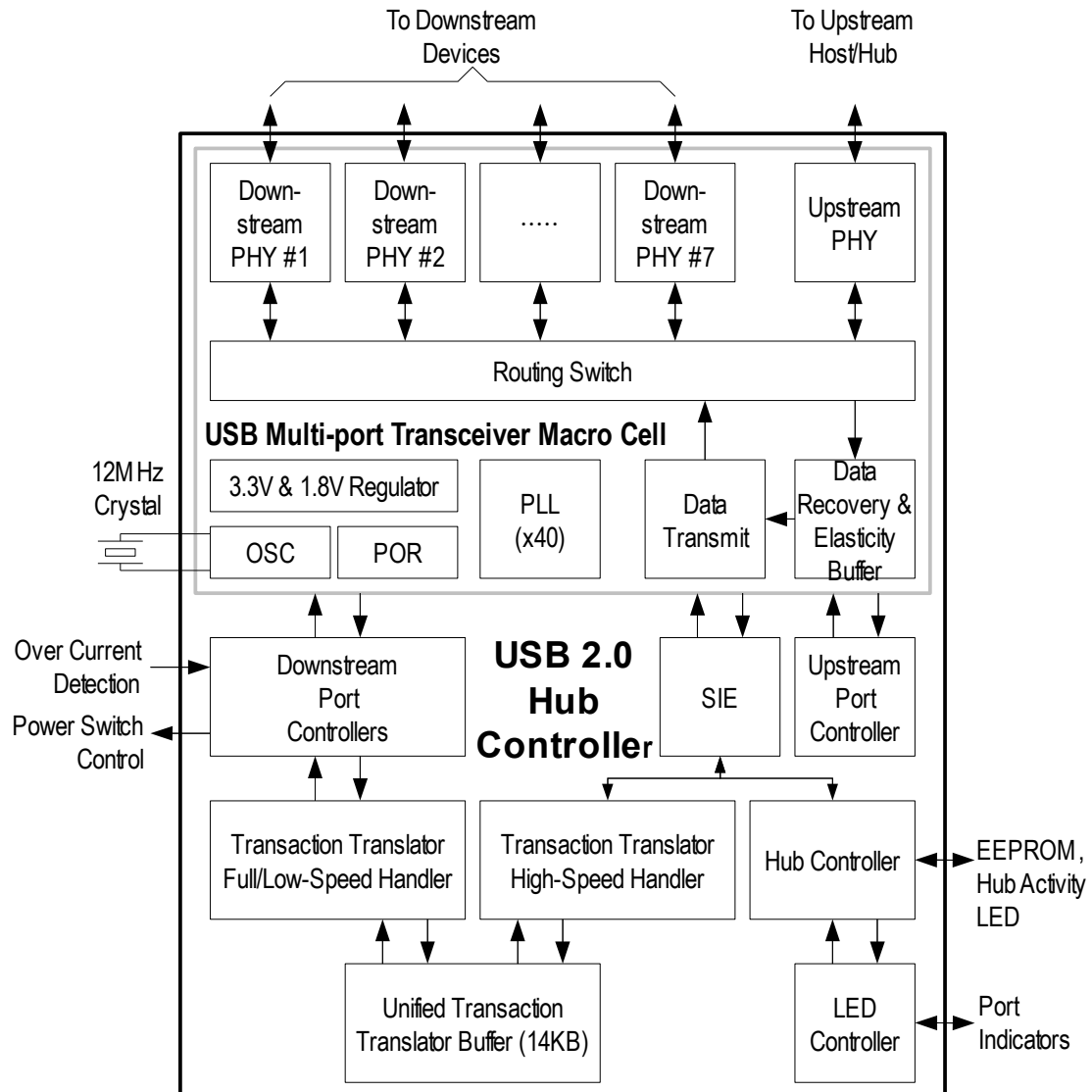 - □ *Hub Active/Suspend* indicator LED.

BLOCK DIAGRAM

To Downstream
Devices

To Upstream
Host/Hub

| Down-stream PHY #1 | Down-stream PHY #2 | ..... | Down-stream PHY #7 | Upstream PHY |

Routing Switch

USB Multi-port Transceiver Macro Cell

12MHz
Crystal

| 3.3V & 1.8V Regulator | PLL (x40) | Data Transmit | Data Recovery & Elasticity Buffer |
| OSC | POR | | | |

USB 2.0 Hub Controller

Over Current
Detection

Power Switch
Control

| Downstream Port Controllers | SIE | Upstream Port Controller |

| Transaction Translator Full/Low-Speed Handler | Transaction Translator High-Speed Handler | Hub Controller |

EEPROM,
Hub Activity
LED

| Unified Transaction Translator Buffer (14KB) | LED Controller |

Port
Indicators

Fig. 1: Block Diagram

PACKAGE I – 64-PIN LQFP
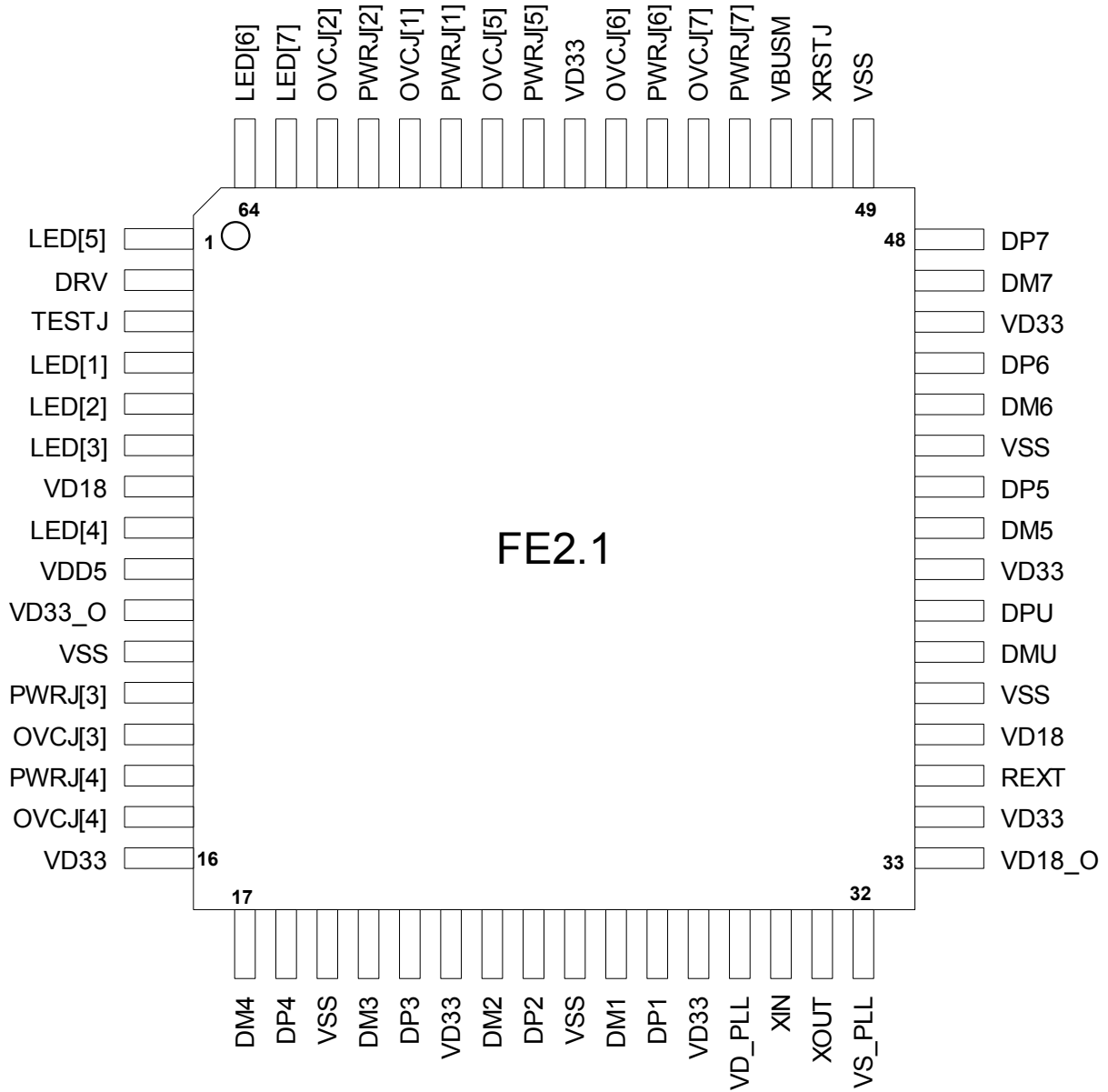
(Body Size: 10x10 mm)

PIN ASSIGNMENT

Fig. 2: 64-pin LQFP Pin Assignment

PACKAGE II – 48-PIN LQFP
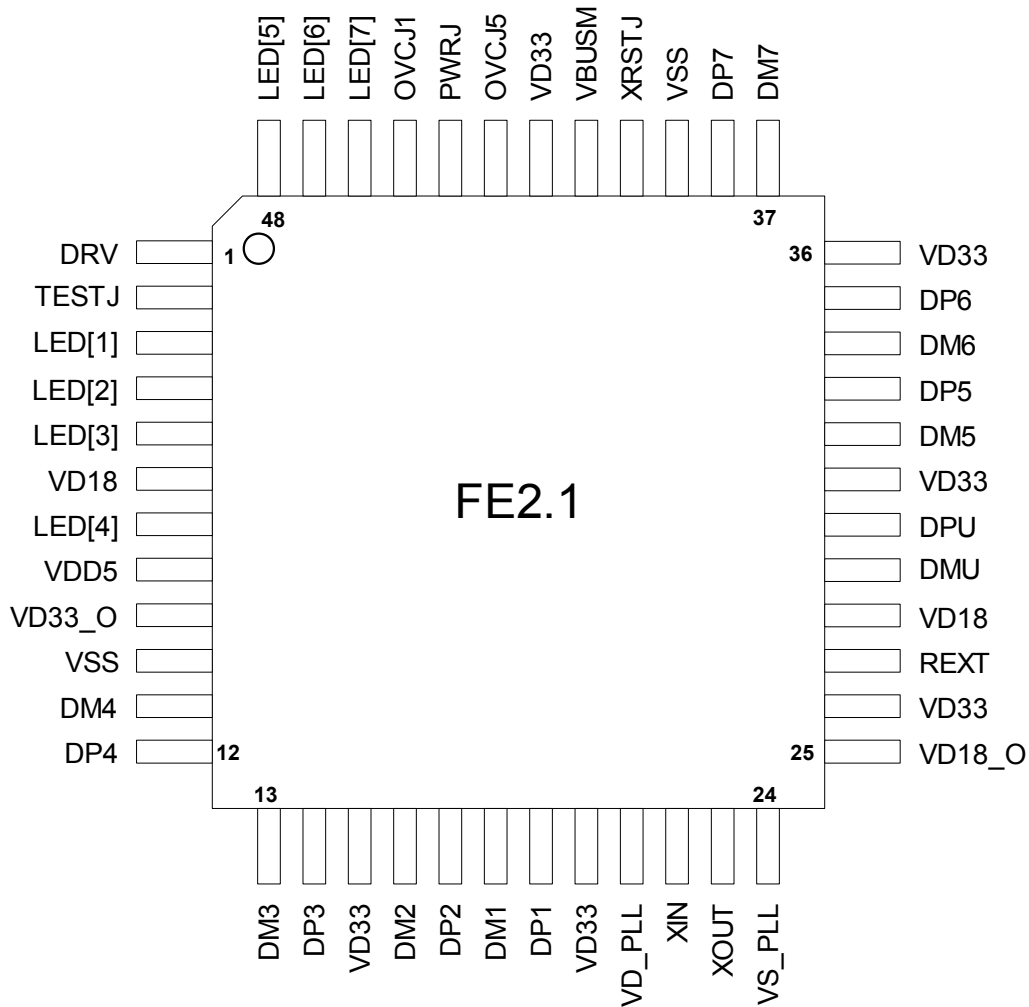
(Body Size: 7x7 mm)

PIN ASSIGNMENT

Fig. 3: 48-pin LQFP Pin Assignment

TERMINUS

PIN DESCRIPTION TABLE

Pin Name	64-pin LQFP Pin#	48-pin LQFP Pin#	Type	Function	Note
LED[5]	1	48	O	LED Control for the 5th Downstream Facing Port Status.	
DRV	2	1	O	Driving Control for all LED.	
TESTJ	3	2	IO-PU	Test Mode Enable during hardware reset, active low. Otherwise, SDA, Serial Data/Address pin for external Serial EEPROM.	
LED[1]	4	3	O/ IO-PU	LED Control for the 1st Downstream Facing Port Status, and SCL, Serial Clock pin for external Serial EEPROM.	4
LED[2]	5	4	O/ I-PU	LED Control for the 2nd Downstream Facing Port Status, and Non-Removable Device Configuration bit 0.	3
LED[3]	6	5	O/ I-PU	LED Control for the 3rd Downstream Facing Port Status, and Non-Removable Device Configuration bit 1.	3
VD18	7, 36	6, 28	P	1.8V power input.	
LED[4]	8	7	O/ I-PU	LED Control for the 4th Downstream Facing Port Status, and Non-Removable Device Configuration bit 2.	3
VDD5	9	8	P	5V power input for integrated 5V→3.3V regulator.	
VD33_O	10	9	P	3.3V power output from 5V→3.3V integrated regulator – a 10μF decoupling capacitor is required.	
VSS	11, 19, 25, 37, 43, 49	10, 39	P	Ground.	
PWRJ[3]	12	—	OD	Power Enable for 3rd Downstream Facing Port, active low.	
OVCJ[3]	13	—	I-PU	Over-current Detect for 3rd Downstream Facing Port, active low.	1
PWRJ[4]	14	—	OD	Power Enable for 4th Downstream Facing Port, active low.	
OVCJ[4]	15	—	I-PU	Over-current Detect for 4th Downstream Facing Port, active low.	1
VD33	16, 22, 28, 34, 40, 46, 56	15, 20, 26, 31, 36, 42	P	3.3V Power Input.	
DM4	17	11	UTD	The D- pin of the 4th Downstream Facing Port.	
DP4	18	12	UTD	The D+ pin of the 4th Downstream Facing Port.	

DM3	20	13	UTD	The D- pin of the 3rd Downstream Facing Port.	
DP3	21	14	UTD	The D+ pin of the 3rd Downstream Facing Port.	
DM2	23	16	UTD	The D- pin of the 2nd Downstream Facing Port.	
DP2	24	17	UTD	The D+ pin of the 2nd Downstream Facing Port.	
DM1	26	18	UTD	The D- pin of the 1st Downstream Facing Port.	
DP1	27	19	UTD	The D+ pin of the 1st Downstream Facing Port.	
VD_PLL	29	21	P	1.8V Power for PLL.	
XIN	30	22	OSC	12 MHz Crystal Oscillator input	
XOUT	31	23	OSC	12 MHz Crystal Oscillator output.	
VS_PLL	32	24	P	Ground for PLL.	
VD18_O	33	25	P	1.8V power output from 3.3V→1.8V integrated regulator – a 10μF decoupling capacitor is required.	
REXT	35	27	A	A 2.7KΩ (± 1%) resister should be connected to VSS to provide internal bias reference.	
DMU	38	29	UTU	The D- pin of the Upstream Facing Port.	
DPU	39	30	UTU	The D+ pin of the Upstream Facing Port.	
DM5	41	32	UTD	The D- pin of the 5th Downstream Facing Port.	
DP5	42	33	UTD	The D+ pin of the 5th Downstream Facing Port.	
DM6	44	34	UTD	The D- pin of the 6th Downstream Facing Port.	
DP6	45	35	UTD	The D+ pin of the 6th Downstream Facing Port.	
DM7	47	37	UTD	The D- pin of the 7th Downstream Facing Port.	
DP7	48	38	UTD	The D+ pin of the 7th Downstream Facing Port.	
XRSTJ	50	40	I	External Reset, active low, is an optional source of chip reset signal. The minimum low pulse width is 10 μs.	
VBUSM	51	41	I	The V$_{BUS}$ Monitor of upstream facing port.	
PWRJ[7]	52	—	OD/ I-PU	Power Enable for 7th Downstream Facing Port, active low, and Power Control Mode Configuration bit 1.	2
OVCJ[7]	53	—	I-PU	Over-current Detect for 7th Downstream Facing Port, active low.	1
PWRJ[6]	54	—	OD/ I-PU	Power Enable for 6th Downstream Facing Port, active low, and Power Control Mode Configuration bit 1.	2
OVCJ[6]	55	—	I-PU	Over-current Detect for 6th Downstream Facing Port, active low.	1
PWRJ[5]	57	—	OD	Power Enable for 5th Downstream Facing Port, active low.	
OVCJ[5]	58	43	I-PU	Over-current Detect for 5th Downstream Facing Port, active low.	1
PWRJ[1]	59	44	OD	Power Enable for 1st Downstream Facing Port, active low.	
OVCJ[1]	60	45	I	Over-current Detect for 1st Downstream Facing Port, active low.	1, 3
PWRJ[2]	61	—	OD	Power Enable for 2nd Downstream Facing Port, active low.	

OVCJ[2]	62	—	I-PU	Over-current Detect for 2nd Downstream Facing Port, active low.	1
LED[7]	63	46	O/ I-PU	LED Control for the 7th Downstream Facing Port Status, and Number of Ports Configuration bit 0.	3
LED[6]	64	47	O/ I-PU	LED Control for the 6th Downstream Facing Port Status, and Number of Ports Configuration bit 1.	3

Note

1. Pins OVCJ[7:2] are equipped with optional internal pull-up resisters. When certain OVCJ pin is not required by currently configured over-current protection mode, its internal pull-up resister will be applied so that pin can be left as unconnected on the board. Otherwise, when certain OVCJ pin is used by currently configured over-current protection mode, its pull-up resister will be removed so that it could be used to monitor either 3.3V or 5V input from external application circuit.

2. During power up configuration stage, pins PWRJ[7:6] are used as input with internal pull-up resisters. Once passed that stage, they will be configured as open drain output.

3. During power up configuration stage, pins LED[4:2] and LED[7:6] are used as input with internal pull-up resister. Once passed that stage, they will be configured as CMOS output.

4. During power up configuration stage, pin LED[1] is used as CMOS tristate I/O to work with the external EEPROM as serial clock. Once passed that stage, it is used as CMOS output.

Type Abbreviation –

I :   Schmitt Trigger Input, 5V-Tolerant;

I-PU :   Input with Controllable Internal Pull-Up, 5V-Tolerant when pull-up resisters is disabled;

IO-PU :   CMOS 3-state Output with Input and Internal Pull-Up;

OD :   Open Drain Output;

O :   CMOS Output;

A :   Analog I/O;

P :   Power/Ground;

OSC :   Crystal Oscillator with internal bias resister and load capacitor;

UTU :   USB High Speed and Full Speed Transceiver;

UTD :   USB High Speed, Full Speed, and Low Speed Transceiver.

CONFIGURABLE OPTIONS

The FE2.1 is a highly versatile design that can be configured to meet many varieties of implementation requirement in a rather easy way. The behavior of FE2.1 can be configured by either board design selected options or through contents of external EEPROM.

LED Indicators, Number of Downstream Facing Port, and Non-Removable Devices

According to USB 2.0 Specification, the status of each downstream port is shown by two LED indicators – the Green and Amber LED. FE2.1 supports the full function as specified by DRV and LED[7:1] pins. Figure 4 shows how these port status indicators be connected, together with the external EEPROM and the *Hub Active Indicator* (the Red LED).
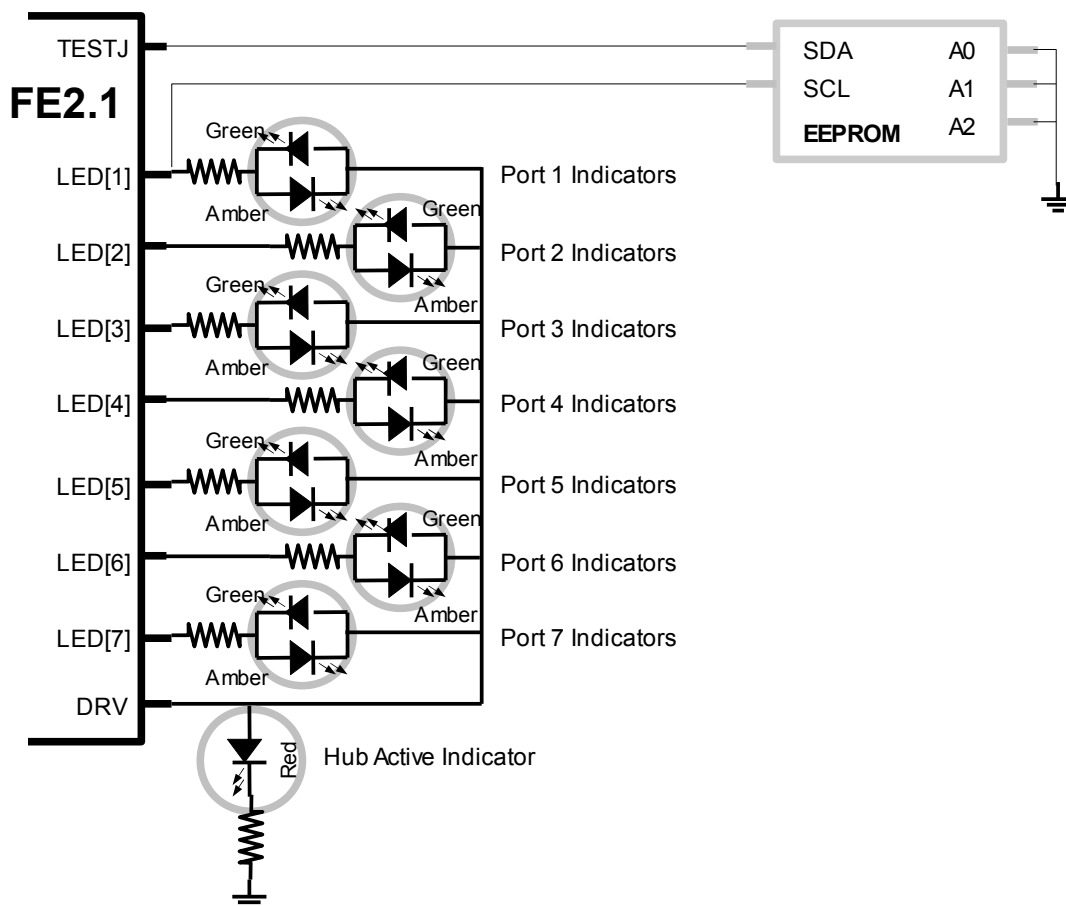

Fig. 4: LED and EEPROM Connections

The optional Hub Active Indicator is only turned on when the hub is configured by the host, and turned off when the hub is either set into suspend mode, disconnected, or powered off by the host. Any of these fifteen LED's could be removed without effecting the normal function of the hub.

The LED[7:1] pins could also be used to configure the number of downstream facing port and non-removable downstream devices. These option selections are sampled and loaded each time after chip reset. If an alternate configuration is intended, the corresponding pins should be tied to ground as shown in the following table. Otherwise, denoted as **Normal** in the following tables, they could be either left floating or connected to the LED's as shown by figure 4.

Usable Downstream Facing Port	LED[7]	LED[6]
4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground
5, 4, 3, 2, 1	Normal	Tied-to-Ground
6, 5, 4, 3, 2, 1	Tied-to-Ground	Normal
7, 6, 5, 4, 3, 2, 1	Normal	Normal

Setting the number of Downstream Facing Port by tying any of LED[7:6] to ground will change the **bNbrPorts** field (3rd byte) of *Hub Descriptor* as response to host's **GetHubDescriptor** request. Henceforth the ports beyond the specified number will not be recognized nor activated by the host.

Non-Removable Downstream Facing Ports	LED[4]	LED[3]	LED[2]
None	Normal	Normal	Normal
2	Normal	Normal	Tied-to-Ground
3, 2	Normal	Tied-to-Ground	Normal
3, 2, 1	Normal	Tied-to-Ground	Tied-to-Ground
4, 3, 2, 1	Tied-to-Ground	Normal	Normal
5, 4, 3, 2, 1	Tied-to-Ground	Normal	Tied-to-Ground
6, 5, 4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground	Normal
7, 6, 5, 4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground	Tied-to-Ground

The Non-Removable Downstream Facing Ports setting is reported in the bit-map of **DeviceRemovable** field of Hub Class Descriptor.

When a downstream facing port is configured as unusable or non-removable, its corresponding LED pin will be disabled. In other words, those LED pins should be either tied to ground based on the selected configuration, or left floating. The only exception is LED[1], which would be still used as SCL, Serial Clock pin for external EEPROM, should it exist.

Figure 5 depicts an example that enable 5 downstream facing ports only, with port 3 and 2 as non-removable device. As shown, the LED[4] is connected to the LED's, LED[2] left floating, and LED[3] tied to ground, so that the FE2.1 would recognize that port 3 and 2 are non-removable devices. The LED[6] is tied to ground and LED[7] left floating, thus the FE2.1 will report to system that only 5 ports are available in this hub.
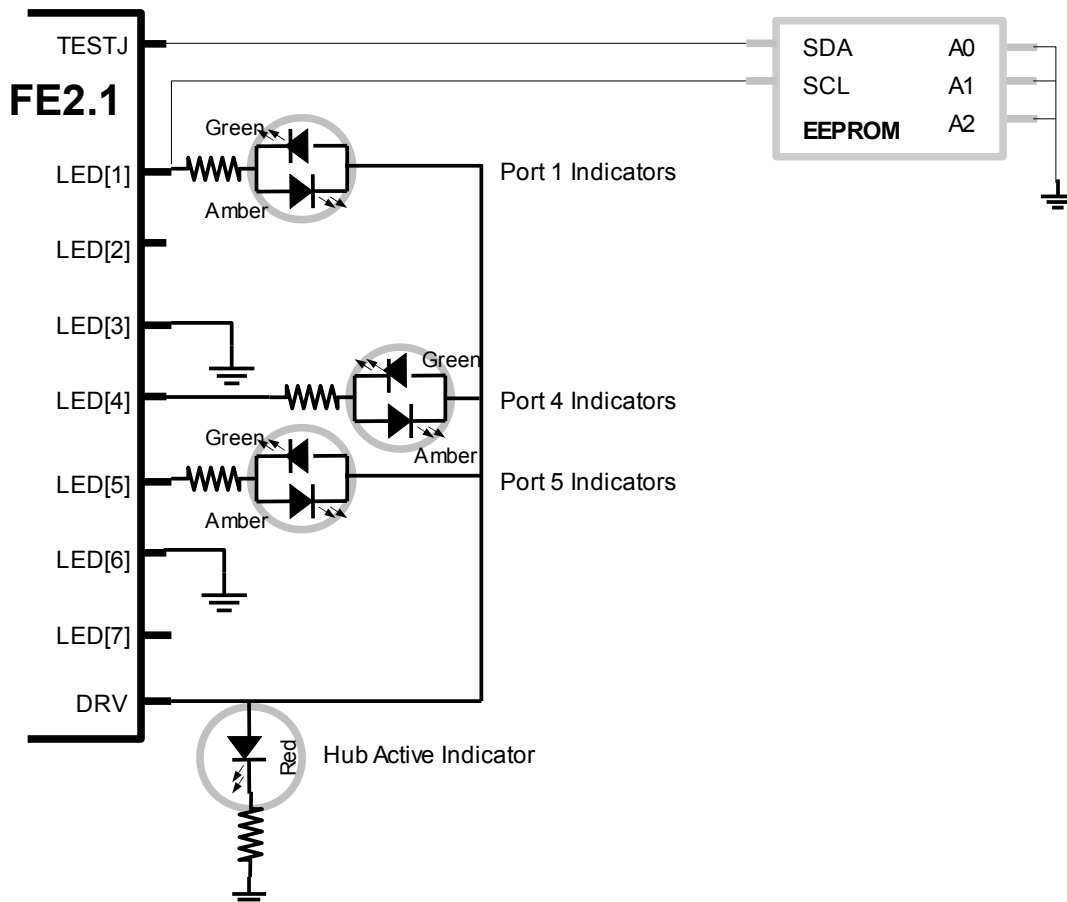

Fig. 5: LED Board Configuration Example

If the external EEPROM is not required, the TESTJ should be left floating. If the Hub Active Indicator is not required, the LED and its serial resister should be removed together. If the port status LED's are not required, LED[5:4, 1] could be all left floating with all their related Green/Amber LED's and resisters removed.

Power Control and Over-current Protection

The FE2.1 supports optional power switches that control delivery of power downstream facing ports by way of a set of active low, open drain, control pins, PWRJ[7:1]. With external pull-up resisters to either 5V or 3.3V, system designers could choice from a wide variety of circuit to implement the power switches.

As self-powered hub, over-current protection is a must for safety reasons. The FE2.1 provides a set of input pins, OVCJ[7:1], to monitor status of external over-current detection circuit. The over-current status will than be reported to the host hub driver by FE2.1. Depends on the power control mode actually selected, the unused OVCJ pins will be internally pull-up and left unconnected on board.

The FE2.1 supports three types of power control modes, namely *Individual Mode*, *Multiple Gangs Mode*, and *Ganged Mode*. These modes could be configured by tying either or both of PWRJ[7:6] to ground according to the following table.

Power Control Mode	PWRJ[7]	PWRJ[6]	wHubCharacteristics		PWRJ [$\mathcal{N}$]	OVCJ [$\mathcal{N}$]	Availability
			D1..D0	D4..D3			
Individual Mode	Normal	Normal	01	01	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	LQFP-64
Multiple Gangs Mode	Tied-to-Ground	Normal	00	01	1	1, 5	LQFP-64, LQFP-48
Ganged Mode	Tied-to-Ground	Tied-to-Ground	00	00	1	1	LQFP-64

In the *Individual Mode*, the power switch of each port is controlled individually, and the over-current status is reported on a per-port basis. That is, for each port $\mathcal{N}$, the power switch is controlled by PWRJ[$\mathcal{N}$], and the over-current status is monitored by OVCJ[$\mathcal{N}$].

In the *Ganged Mode*, the power switch to all ports are controlled by one single PWRJ[1], and the over-current is monitored by OVCJ[1]. Therefore, when host issues SetPortFeature(PORT_POWER) to any of the downstream facing port, the PWRJ[1] will go active, and only when all ports are in powered-off state that PWRJ[1] will be turned inactive. Since there is only one OVCJ input, all downstream facing ports will be marked as over-current simultaneously and set to powered-off state.

The *Multiple Gangs Mode* has one more over-current status pin, OVCJ[5], then the Ganged Mode. If

OVCJ[1] goes low, downstream facing port 1, 2, 3, and 4 would be marked as over-current. If OVCJ[5] goes low, downstream facing port 5, 6, and 7 would be marked as over-current. Since there is only one PWRJ pin, all ports will be switched to powered-off state at once. This is the only mode supported by LQFP-48 package of FE2.1.

The power control mode selection is reported to the host software through the wHubCharacteristics field, the 4th and 5th byte, of Hub Descriptor, which describes the hub's operational characteristics. Two bit-fields would be effected – "D1..D0" for *Logical Power Switching Mode*, and "D4..D3" for *Over-current Protection Mode*. In "D1..D0", 00 means ganged power switching (all ports' power at the once,) and 01 means individual port power switching. In "D4..D3", 00 represents global over-current protection, and 01 represents individual port over-current protection.

Figure 6 demonstrates a LQFP-64 implementation of Individual Mode design with dual-channel power distribution switches. In this case, 3,3V pull-up are used for PWRJ/Enable pins to meet the requirement of the specific switches used.
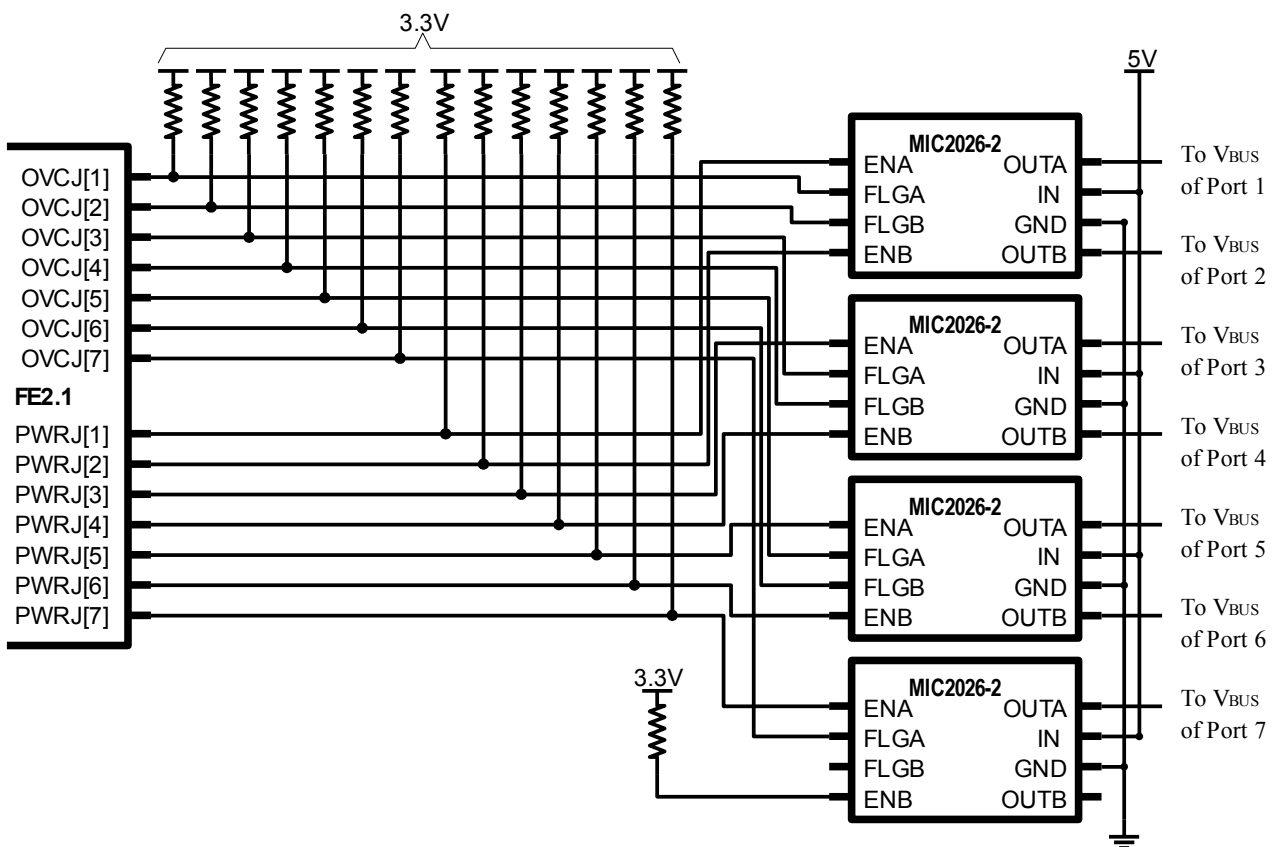

Fig. 6: LQFP-64 Individual Power Control Mode Example

Figure 7 demonstrates LQFP-64 implementations of Multiple Gangs Mode and Ganged Mode with

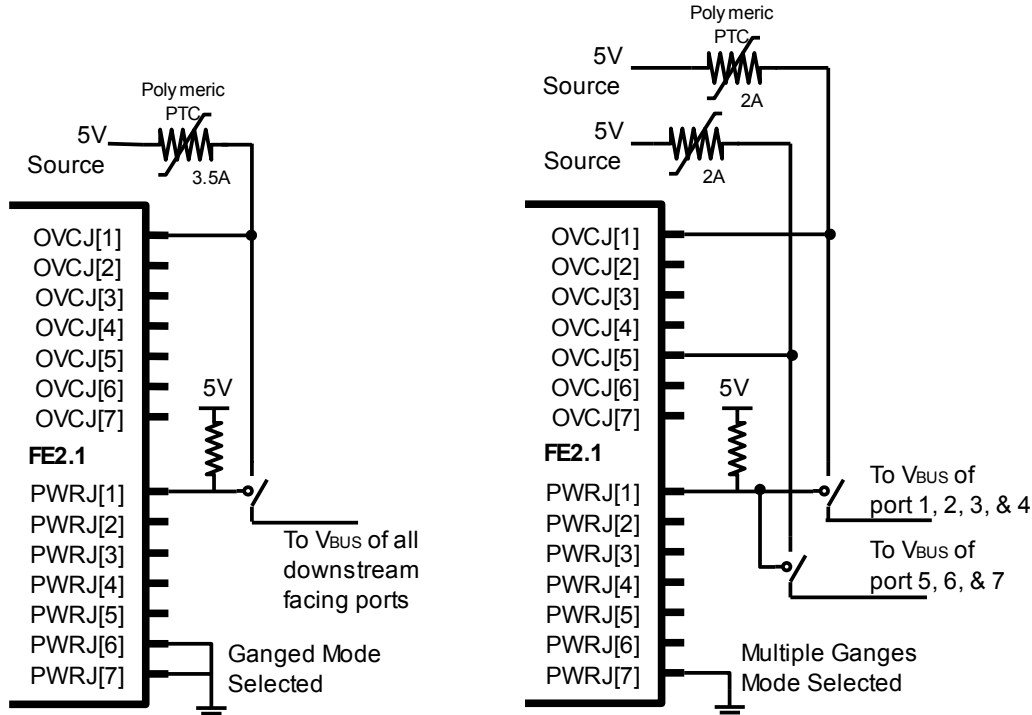polymeric PTC and MOSFET switches. In these cases, 5V pull-up are used instead.

Fig. 7: LQFP-64 Power Control Mode Examples

And Figure 8 shows LQFP-48 implementation for Multiple Gangs Mode – the only mode supported by LQFP-48 package.
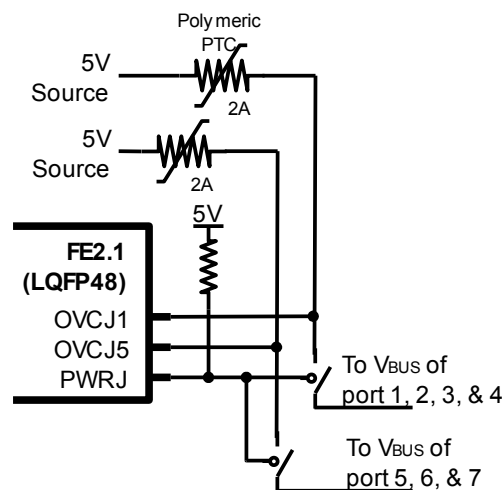

Fig. 8: LQFP-48 Power Control Example

EEPROM CONTENTS

Address	Contents	Note
0x00	0x40	Constant, low byte of check code
0x01	0x1A	Constant, high byte of check code
0x02	Vendor ID (Low)	Low byte of Vendor ID, idVendor field of *Standard Device Descriptor*
0x03	Vendor ID (High)	High byte of Vendor ID, idVendor field of *Standard Device Descriptor*
0x04	Product ID (Low)	Low byte of Product ID, idProduct field of *Standard Device Descriptor*
0x05	Product ID (High)	High Byte of Product ID, idProduct field of *Standard Device Descriptor*
0x06	Device Release (Low)	Low byte of Device Release Number, must be Binary Coded Decimal, bcdDevice field of *Standard Device Descriptor*
0x07	Device Release (High)	High byte of Device Release Number, must be Binary Coded Decimal, bcdDevice field of *Standard Device Descriptor*
0x08 ~ 0x17	Device Serial Number	Device's Serial Number – the contents of string descriptor describing the device's serial number.
0x18	Length of Serial Number	Length of effective "Device Serial Number" stored in 0x08 to 0x17.
0x19	Filling	0x00
0x1A	Port Number	Number of Downstream Ports, bNbrPorts field of *Hub Descriptor*.
0x1B	Filling	0x00
0x1C	Device Removable	*DeviceRemovable* field of Hub Descriptor – Indicates if a port has a removable device attached. If bit N is set to 1, then the device on downstream facing port N is non-removable. Otherwise, it is removable. Bit 0 is reserved and should be 0.
0x1D	Filling	0x00
0x1E	Device Attributes	Bit 0: Port Indicators Support, bit 7 of *wHubCharacteristics* field of Hub Descriptor – 0: Port Indicators are not supported on its downstream facing ports and PORT_INDICATOR request has no effect. 1: Port Indicators are supported on its downstream facing ports and PORT_INDICATOR request controls the indicators. Bit 1: Identifies a Compound Device, bit 2 of *wHubCharacteristics* field of Hub Descriptor – 0: Hub is not part of a compound device. 1: Hub is part of a compound device. Bit 2: Maximum current requirements of the Hub Controller electronics, *bHubContrCurrent* field of Hub Descriptor – 0: 200mA. 1: 500mA. Bit 3 to 7, reserved, must be 0's.
0x1F	Check Sum	The 8-bit sum of all value from 0x00 to 0x1E.

The first two bytes are the check code for the existence of EEPROM, their value must be 0x1A40. Any other value would cause the EEPROM loading mechanism of FE2.1 to conclude that the contents of this EEPROM is unusable, and use default values instead.

The string descriptor for device's serial number could be defined by *Device Serial Number* and *Length of Serial Number* fields of the EEPROM, address 0x08 to 0x18. Length of Serial Number field, address 0x18, define the number of digits, while Device Serial Number field, address 0x08 to 0x17, specify the serial number in ASCII code. The space after the specified number of digits should be filled with Null, 0x00. For example, suppose the serial number is "A090108F4", then the EEPROM should be like:

0x08	0x41 (A)	0x30 (0)	0x39 (9)	0x30 (0)	0x31 (1)	0x30 (0)	0x38 (8)	0x46 (F)
0x10	0x34 (4)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)
0x18	0x09							

The last byte, address 0x1F, is a checksum made up of the sum of all value from 0x00 to 0x1E. The numbers must match to render the contents of the EEPROM usable. Otherwise, the loading mechanism of FE2.1 would discard the value from EEPROM and use default values instead.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	℃
Power Supply Voltage	VDD5 VD33 VD18 & VD_PLL	-0.5 -0.5 -0.5	+6.0 +4.0 +2.5	V
ESD Human Body Mode		-2000	2000	V
ESD Machine Mode		-200	200	V
Latch Up		-200	200	mA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	℃
Case Temperature (LQFP-64 package)	TC_{64}	0		110	℃
Case Temperature (LQFP-48 package)	TC_{48}	0		105	℃
Operating voltage	VDD5 VD33 VD18 & VD_PLL	4.5 3.0 1.62	5.0 3.3 1.8	5.5 3.6 1.98	V
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
Threshold voltage of digital input	VTH	1.45	1.58	1.74	V
Low-to-High level of schmitt-trigger input	VT+	1.44	1.5	1.56	V
High-to-Low level of schmitt-trigger input	VT-	0.89	0.94	0.99	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V
Internal Pull-Up Resister Range	R_{PU}	39	65	116	KΩ

POWER CONSUMPTION

DC SUPPLY CURRENT

Symbol	Condition			Typ.	Unit
	Active ports	**Host**	**Device**		
I_suspend	Suspend			600	uA
Icc	7	Full-Speed	7x Full-Speed	36	mA
		High-Speed	7x High-Speed	155	mA
		High-Speed	7x Full-Speed	53	mA
	6	Full-Speed	6x Full-Speed	36	mA
		High-Speed	6x High-Speed	140	mA
		High-Speed	6x Full-Speed	53	mA
	5	Full-Speed	5x Full-Speed	36	mA
		High-Speed	5x High-Speed	125	mA
		High-Speed	5x Full-Speed	53	mA
	4	Full-Speed	4x Full-Speed	35	mA
		High-Speed	4x High-Speed	111	mA
		High-Speed	4x Full-Speed	52	mA
	3	Full-Speed	3x Full-Speed	35	mA
		High-Speed	3x High-Speed	96	mA
		High-Speed	3x Full-Speed	52	mA
	2	Full-Speed	2x Full-Speed	35	mA
		High-Speed	2x High-Speed	82	mA
		High-Speed	2x Full-Speed	52	mA
	1	Full-Speed	1x Full-Speed	35	mA
		High-Speed	1x High-Speed	66	mA
		High-Speed	1x Full-Speed	52	mA
	No active	Full-Speed		35	mA
		High-Speed		52	mA

Note: The power consumption is measured when the bus is in IDLE state – there is no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending upon the system configuration, type of operations, and over-all bus utilization.
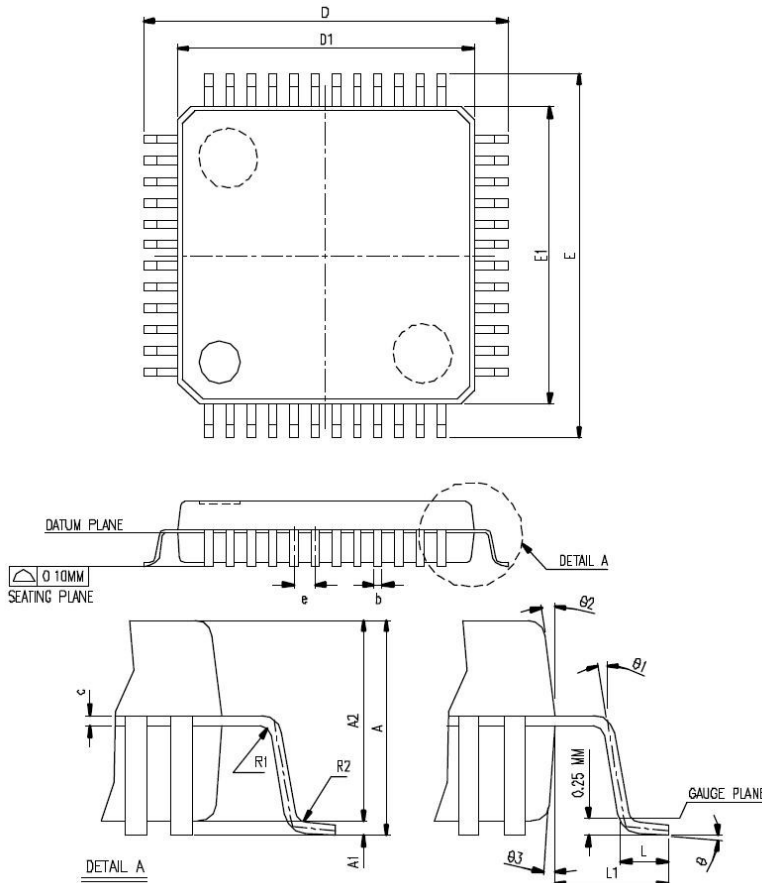
PACKAGE I

64-pin LQFP (Body Size: 10x10 mm)
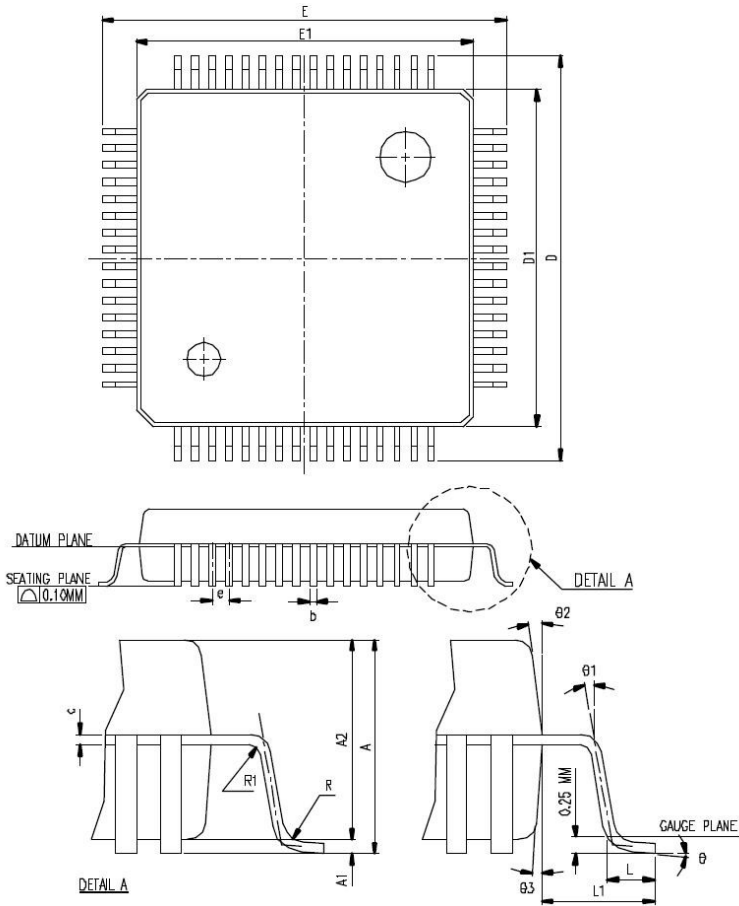
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD
PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE.
" D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
INCLUDING MOLD MISMATCH.

PACKAGE II

48-pin LQFP (Body Size: 7x7 mm)

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
e	0.50 BASIC			0.020 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R2	0.08		0.20	0.003		0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBC)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD
PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE.
" D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
INCLUDING MOLD MISMATCH.