SPECIFICATIONS

FOR

LCD MODULE

Customer: _____

Model name: HW101F-0D-0E(IVO101_40PIN)

Description: LIQUID CRYSTAL DISPLAY MODULE

Date: 2013-09-27

CUSTOMER APPROVAL

Customer Approval	☐ Accept ☐ Reject comment: Approved by: _____

SUPPLIER APPROVAL

APPROVED	CHECKED	ORGANIZED

1、OTHERS：

APPROVAL FOR SPECIFICATIONS ONLY

APPROVAL FOR SPECIFICATIONS AND SAMPLE

NOTE: VERSION OF SPECIFICATIONS: 00

2、 OTHERS:

History of revision

Revision	Contents	Date	Note
01	**New Revision**	2013-09-27	1.0

CONTENTS PAGE

1. Introduction And General Specifications

Liquid crystal Displays (LCDS) have widely used in many applications such as industrial measurements, office mechanisms, and household electronic–equipment etc. LCM (LCD Module) integrates with LCD and driving circuit that is easily to be interfaced by user. This LCM contains a standard built-in dot –matrix font set.

1.1Applications of LCM

Telephone
Facsimile mechanism
Electronic Typewriter
Word processor
Electronic memo pads
Remote controller

1.2 Features of LCM

Compact, thin and light
Wide view angle
Low power consumption
High contrast image
Wide operating temperature
High reliability

1.2 General specification

Parameter	Value	Unit
Display Mode	Normal white TN	-
Display Resolution	1024*RGB*600	pixels
Pixel Arrangement	RGB-stripe	-
Viewing Direction	6 o' clock	
Display Mode	Normally white	
IC Package Type	COG	-
MPU Interface	LVDS 6-bit	-
Power Supply Voltage	2.8~3.3	V
Back-light	White LED*21	pcs

1.3 Absolute Maximum Ratings

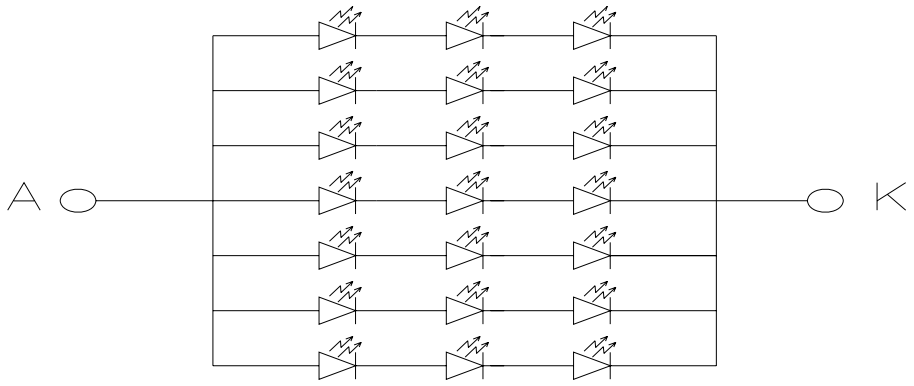
Item	Symbol	Min	Max	Unit	Remark
Backlight Forward Current	I_{LED}	-	8	mA	For each LED
Operating Temperature	T_{OPR}	-20.0	70.0	℃	
Storage Temperature	T_{STG}	-30.0	80.0	℃	

1.4 Electrical Characteristics

Item	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Digital supply voltage	DVDD	--	3.2	--	V
Analog supply Voltage	AVDD	7.2	8.2	9.2	V
Gate On Voltage	VGH	18	19	20	V
Gate Off voltage	VGL	-9	-8.0	-7	V
Common Electrode Driving Signal	VCOM	2.2	3.2	4.2	V

1.5 LCM And Backlight Driving Conditions

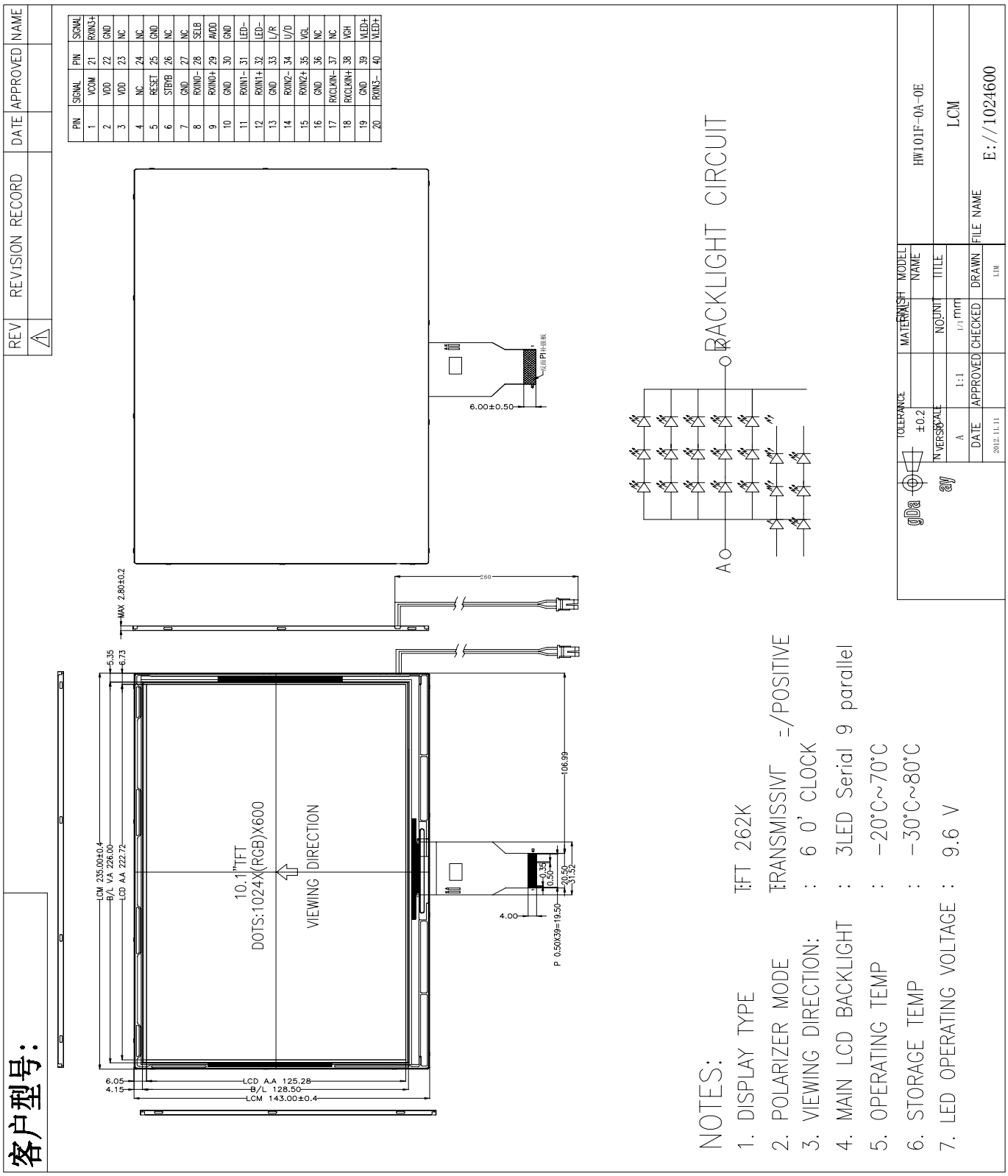
Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED forward voltage	V_L	-	9.0	9.9	V	
LED forward current	I_L	-	140	-	mA	
LCM Luminance	Lv		200		cd/㎡	



BACKLIGHT CIRCUIT

I=140mA U=9.6V

2. LCD&LCM Outline Drawing



3. 6-bit Interface pin Connections Circuit Block Diagram

PIN NO.	SYMBOL	DESCRIPTION
1	VCOM	Vcommon voltage
2-3	VDD	Power Supply
4	NC	NC
5	RESTR	Blobal reset pin
6	STBYB	Standby mode.Normally pulled high STBYB="1".normal operation STBYB="0"timing controller,source driver will turn off,all output are High-Z
7	GND	Power Ground
8	RXIN0-	-LVDS differential data input
9	RXIN0+	+LVDS differential data input(
10	GND	Power Ground
11	RXIN1-	-LVDS differential data input
12	RXIN1+	+LVDS differential data input
13	GND	Power Ground
14	RXIN2-	-LVDS differential data input
15	RXIN2+	+LVDS differential data input
16	GND	Power Ground
17	RXCLKIN-	-LVDS differential clock input
18	RXCLKIN+	+LVDS differential clock input
19	GND	Power Ground
20	RXIN3-	-LVDS differential clock input
21	RXIN3+	+LVDS differential clock input
22	GND	Power Ground
23-24	NC	NC
25	GND	Power Ground
26-27	NC	NC
28	SELB	6/8bit mode select。SELB=0 : 8BIT/ SELB=1 : 6BIT
29	AVDD	Power for analog circuit
30	GND	Power Ground
31-32	LED-	LED Cathode
33	L/R	Horixontal inversion
34	U/D	Verticalcinversionc
35	VGL	Gate off Voltage
36-37	NC	NC
38	VGH	Gate on Voltage
39-40	VLED+	LED Anode

4. Resolution:1024x600

- **DE mode**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd		600		T_H
VSD Period	tvbp	610	635	800	T_H
VSD Blanking	tvbp+ tvfp	10	35	200	T_H

Table 10.4: DE mode (1024x600)

- **HV mode**

Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp		160		DCLK
HSD Front Porch	thfp	16	160	216	DCLK

Table 10.5: HV mode horizontal timing (1024x600)

Vertical Timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		T_H
VSD Period	tv	624	635	750	T_H
VSD Pulse Width	tvpw	1	-	20	T_H
VSD Back Porch	tvbp		23		T_H
VSD Front Porch	tvfp	1	12	127	T_H

Table 10.6: HV Mode Vertical Timing (1024x600)

4.1 LVDS mode DC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Differential input high Threshold voltage	R_{XVTH}	-	-	+0.1	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-0.1	-	-	V	
Input voltage range (singled-end)	R_{XVIN}	0	-	VDD-1.2+ $\|V_{ID}\|/2$	V	-
Differential input common Mode voltage	R_{XVCM}	$\|V_{ID}\|/2$	-	VDD-1.2	V	-
Differential input voltage	$\| V_{ID} \|$	0.2	-	0.6	V	-
Differential input leakage Current	RV_{Xliz}	-10	-	+10	µA	-
LVDS Digital Operating Current	Iddlvds	-	15	30	mA	Fclk=65MHz, VDD=3.3V
LVDS Digital Stand-by Current	Istlvds	-	10	50	µA	Clock & all Functions are stopped

Table 9.3: LVDS mode DC electrical characteristics

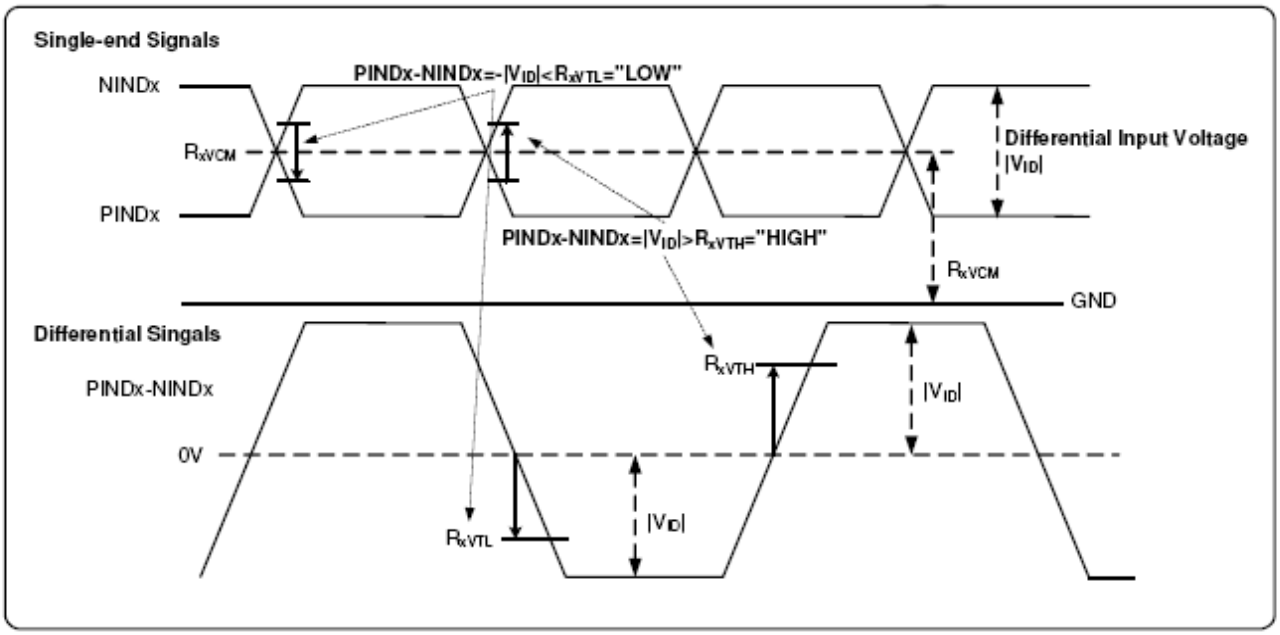


Figure 9.1: Single-end signals

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Base drive current for PWM	IDRV	-	-	60	mA	R_{XVCM} =1.2V
DRV output voltage for PWM	VDRV	0	-	VDD	V	
Feed back voltage for PWM	VFB	0.55	0.6	0.65	V	-
Duty cycle maximum	Dmax	-	-	85	%	-
VCOM buffer input voltage	VCOMI	1	-	AVDD	V	-
VCOM buffer output voltage	VCOMO	VCOMI-0.2	VCOMI	VCOMI+0.2	V	-
VCOM buffer output current	IVCOM	-	-	10	mA	Fclk=65MHz, VDD=3.3V

Table 9.4: Power table

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Condition
Clock frequency	R_{XFCLK}	20	-	71	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	pS	| V_{ID} |=400mV R_{XVCM} =1.2V R_{XFCLK} =71MHz
Clock high time	T_{LVCH}	-	4/(7* R_{XFCLK})	-	ns	-
Clock low time	T_{LVCL}	-	3/(7* R_{XFCLK})	-	ns	-
PLL wake-up time	T_{emPLL}				µs	-

Table 10.2: LVDS mode AC electrical characteristics

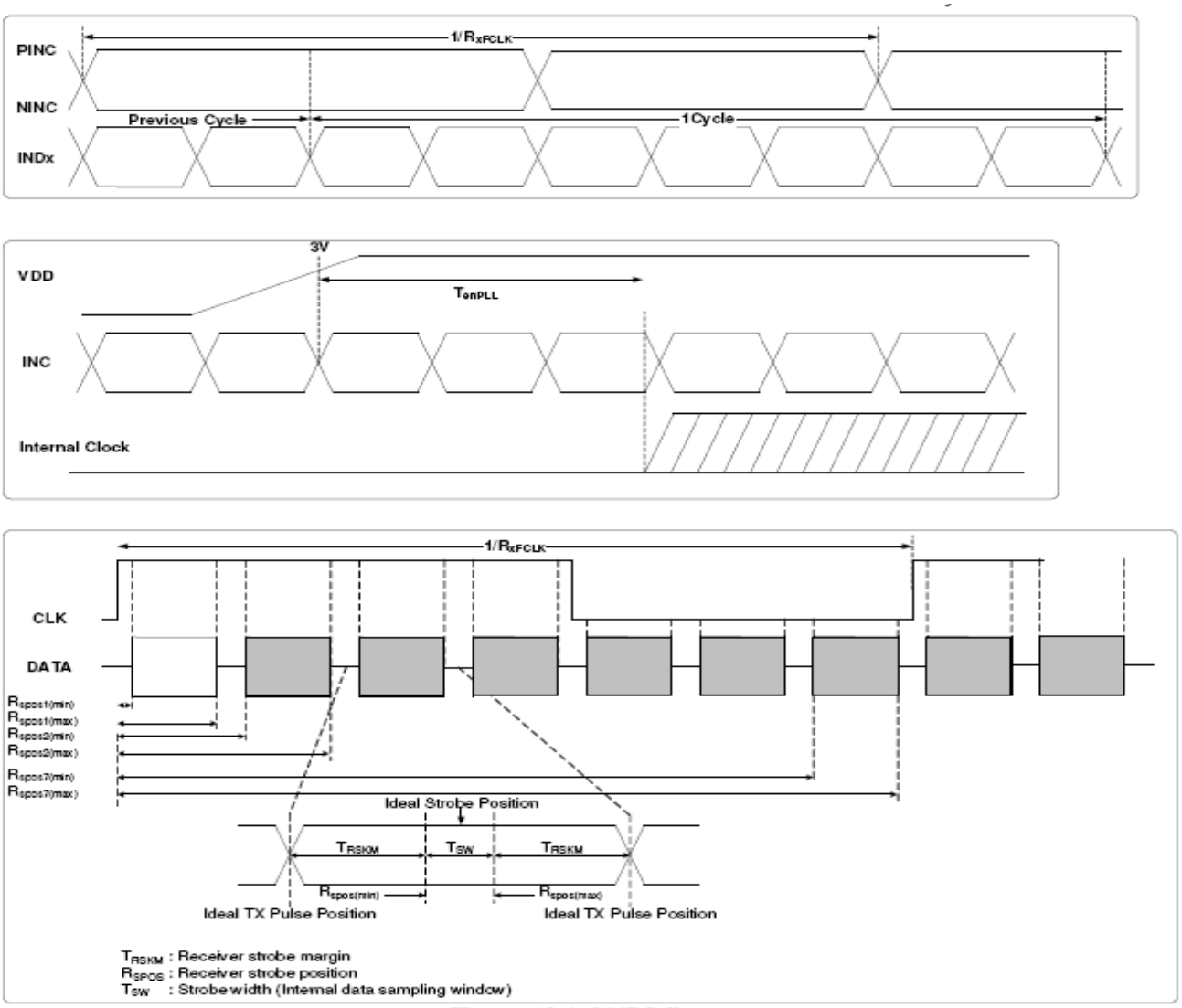


Figure 10.1: LVDS figure

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit	Condition
Modulation Frequency	SSC_{MF}	23	-	93	KHz	-
Modulation Rate	SSC_{MR}	-	-	±3	%	LVDS clock =71MHz center spread

Table 10.3: SSC table

4.2 LVDS mode data input format

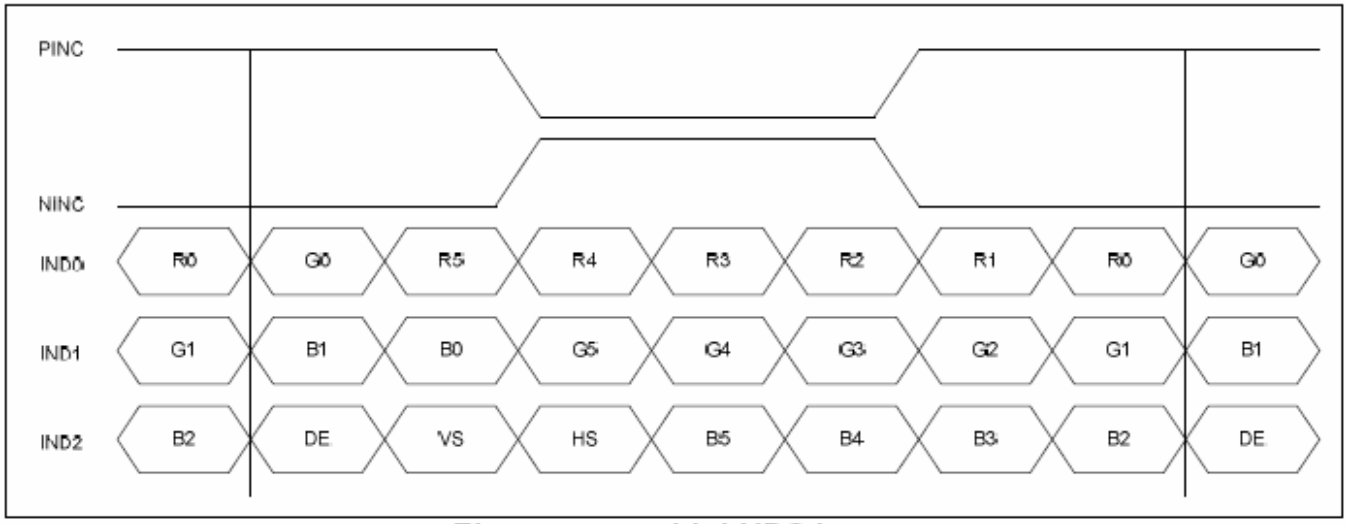


Figure 10.4: 6-bit LVDS input

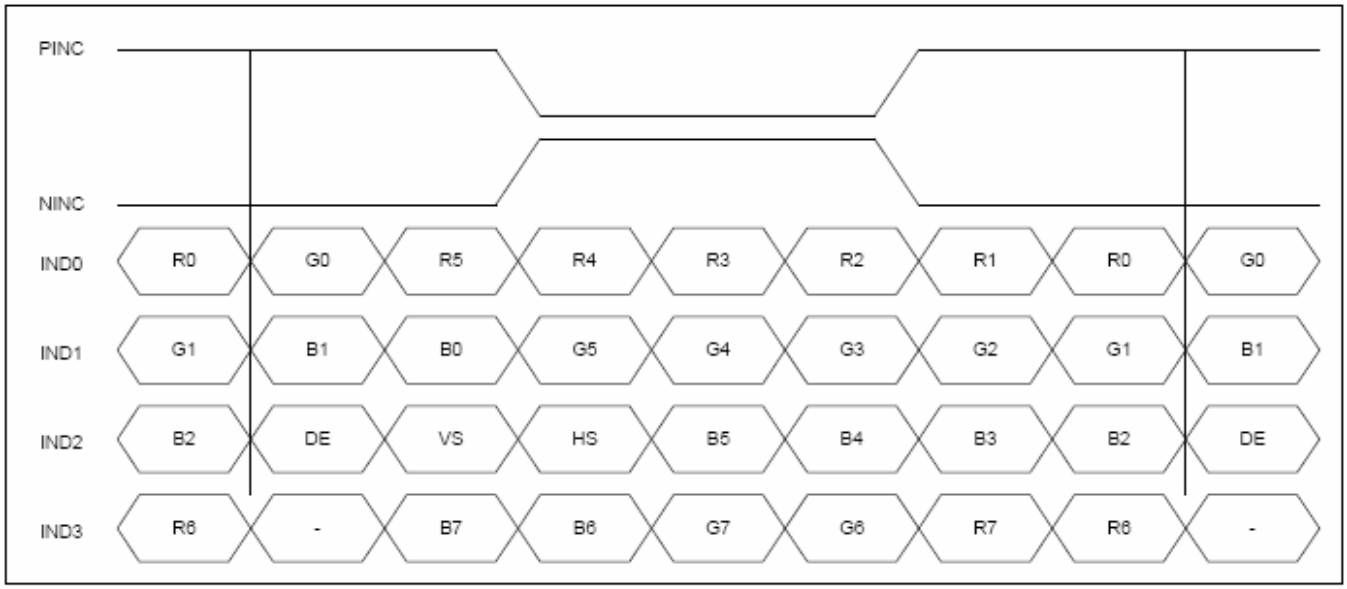
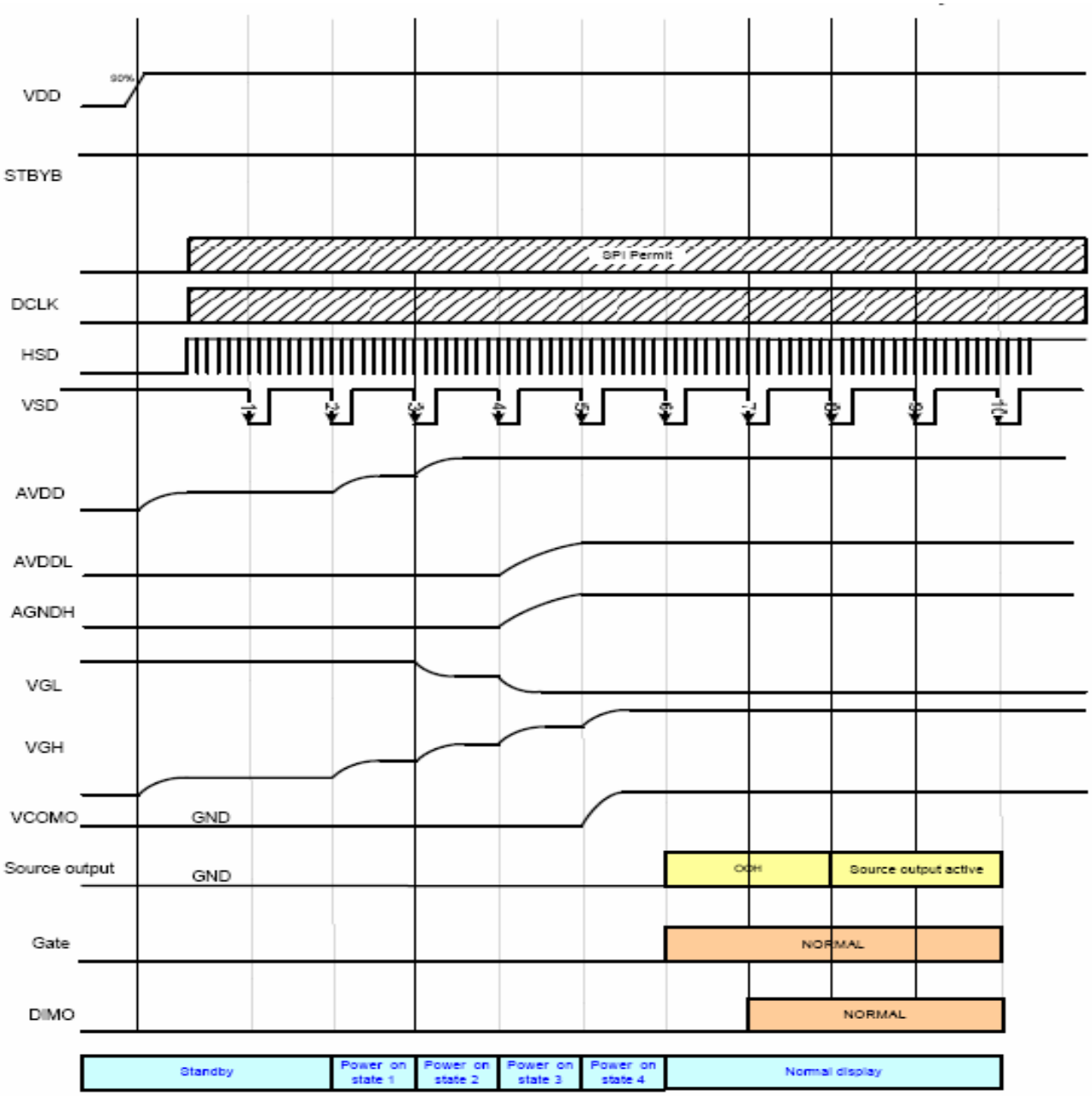


Figure 10.5: 8-bit LVDS Input

5. Power sequence

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.
Power on: VDD, GND ->AVDD, AGND -> V1 to V14
Power off: V1 to V14 -> AVDD, AGND->VDD, GND

5.1 Power on/off control



Note: Low level=3FH, when NBW=L (Normally white)
Low level=00H, when NBW=H (Normally black)

Figure 8.1: Power on/off timing sequence

5.2 Enter and exit standby mode sequence

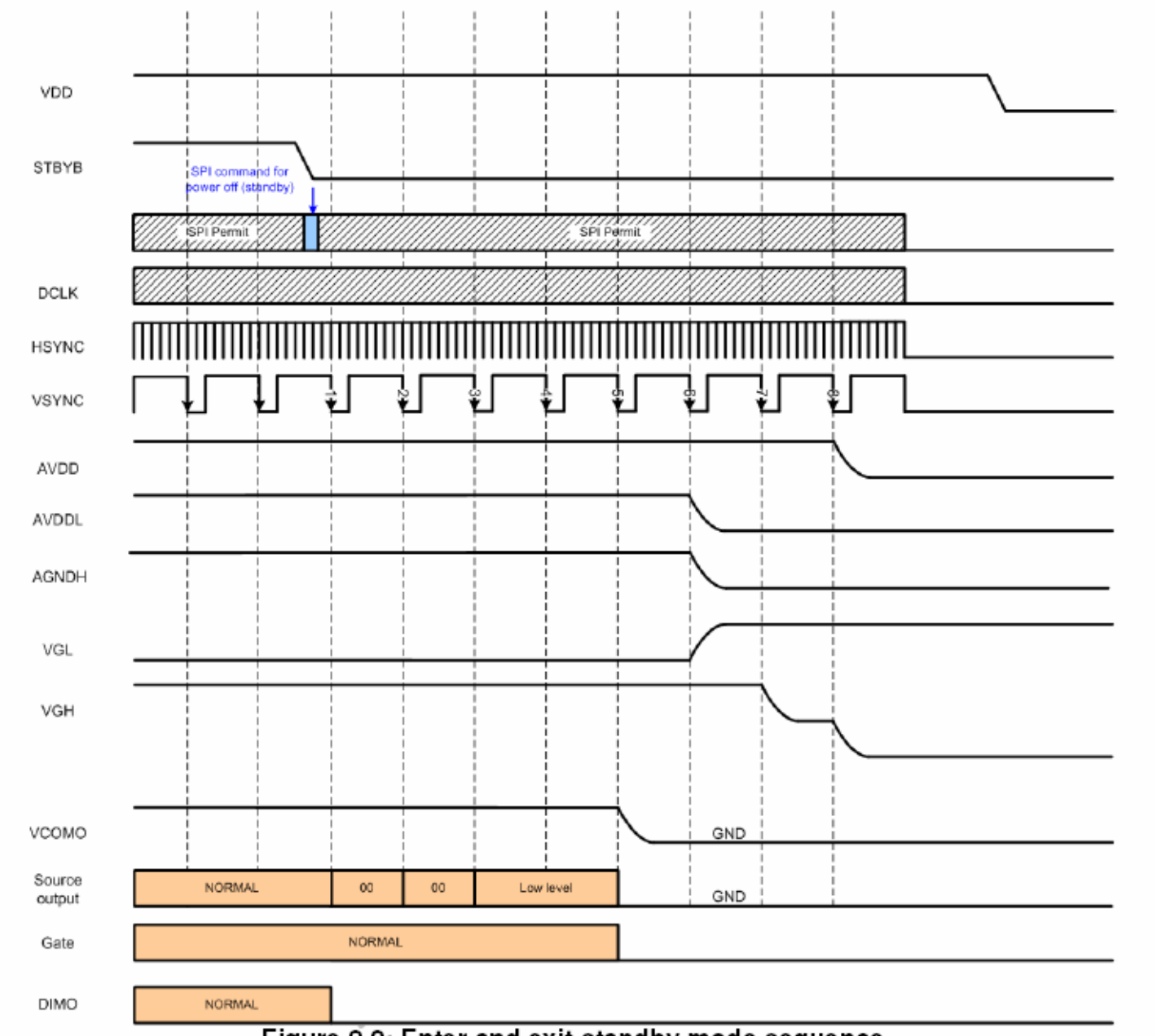


Figure 8.2: Enter and exit standby mode sequence